S6B0724

132 SEG / 65 COM DRIVER & CONTROLLER FOR STN LCD

Mar. 2002.

Ver. 1.1

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.

2. Always test and inspect products under the environment with no penetration of light.

S6B0724 Specification Revision History		
Version	**Content**	**Date**
0.0	Initial version	Mar.1999
0.1	PAD name change (VSS → TEST4)	Mar.1999
0.2	Eq2. changed (page 32)	Mar.1999
0.3	Figure 10. Figure 11. Changed	Mar.1999
0.4	Set Static Indicator Register changed (page 46)	Apr.1999
0.5	PAD location added	Apr.1999
0.6	Modify following sections Introduction, Features, Pad Configuration, Pin Description, Power Supply Circuits, Reference Circuit Examples, DC/AC Characteristics, Connection Between S6B0724 and LCD Panel	Apr.1999
0.7	Pin name changed at page 8 (FRI → FR)	May.1999
0.8	Operating VDD is changed	Oct.1999
0.9	Read timing is changed(Figure 5)	Jun.2000
1.0	Added detail information for several items	Mar.2001
1.1	VDD is changed (2.4V~3.6V -> 2.4V~5.5V)	Mar.2002

CONTENTS

INTRODUCTION

The S6B0724 is a single chip driver & controller LSI for graphic dot-matrix liquid crystal display systems. This chip can be connected directly to a microprocessor, accepts serial or 8-bit parallel display data from the microprocessor, stores the display data in an on-chip display data RAM of 65 x 132 bits and generates a liquid crystal display drive signal independent of the microprocessor. It provides a high-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. It contains 65 common driver circuits and 132 segment driver circuits, so that a single chip can drive a 65 x 132 dot display. And the capacity of the display can be increased through the use of master/slave multi-chip structures.
These chip are able to minimize power consumption because it performs display data RAM read / write operation with no external operation clock. In addition, because it contains power supply circuits necessary to drive liquid crystal, which is a display clock oscillator circuit, high performance voltage converter circuit, high-accuracy voltage regulator circuit, low power consumption voltage divider resistors and OP-Amp for liquid crystal driver power voltage, it is possible to make the lowest power consumption display system with the fewest components for high performance portable systems.

FEATURES

Display Driver Output Circuits

– 65 common outputs / 132 segment outputs

On-chip Display Data RAM

– Capacity: 65 x 132 = 8,580 bits
– RAM bit data " 1" : a dot of display is illuminated.
– RAM bit data " 0" : a dot of display is not illuminated.

Applicable Duty Ratios

Duty ratio	Applicable LCD bias	Maximum display area
1/65	1/7 or 1/9	65 × 132
1/55	1/6 or 1/8	55 × 132
1/49	1/6 or 1/8	49 × 132
1/33	1/5 or 1/6	33 × 132

Microprocessor Interface

– High-speed 8-bit parallel bi-directional interface with 6800-series or 8080-series
– Serial interface (only write operation) available

Various Function Set

– Display ON / OFF, set initial display line, set page address, set column address, read status, write / read display data, select segment driver output, reverse display ON / OFF, entire display ON / OFF, select LCD bias, set/reset modify-read, select common driver output, control display power circuit, select internal regulator resistor ratio for V0 voltage regulation, electronic volume, set static indicator state.
– H/W and S/W reset available
– Static drive circuit equipped internally for indicators with 4 flashing modes

Built-in Analog Circuit

- On-chip oscillator circuit for display clock (external clock can also be used)
- High performance voltage converter (with booster ratios of x2, x3, x4 and x5, where the step-up reference voltage can be used externally)
- High accuracy voltage regulator (temperature coefficient: -0.05%/°C or external input)
- Electronic contrast control function (64 steps)
- Vref = 2.1V ± 3% (V0 voltage adjustment voltage)
- High performance voltage follower (V1 to V4 voltage divider resistors and OP-Amp for increasing drive capacity)

Operating Voltage Range

- Supply voltage (V_{DD}): 2.4 to 3.6 V
- Supply voltage (V_{DD}): 2.4 to 5.5 V (Select by product code)
- LCD driving voltage (V_{LCD} = V0 - V_{SS}): 4.5 to 15.0 V

Low Power Consumption

- Operating power: 40µA typical. (Condition: V_{DD} = 3V, x 4 boosting (VCI is V_{DD}), V0 = 11V, internal power supply ON, display OFF and normal mode is selected)
- Standby power: 10µA maximum. (During power save [standby] mode)

Operating Temperatures

- Wide range of operating temperature: -40 to 85°C

CMOS Process

Package Type

- Gold bumped chip

Series Specifications

Product code	Temperature coefficient	Package type	Chip thickness	VDD Range
S6B0724A01-B0CZ	-0.05%/°C	COG	670 µm	2.4~3.6[V]
S6B0724A01-B0CY			470 µm	
S6B0724A05-B0CZ			670 µm	2.4~5.5[V]
S6B0724A05-B0CY			470 µm	

* xx: TCP ordering number

BLOCK DIAGRAM

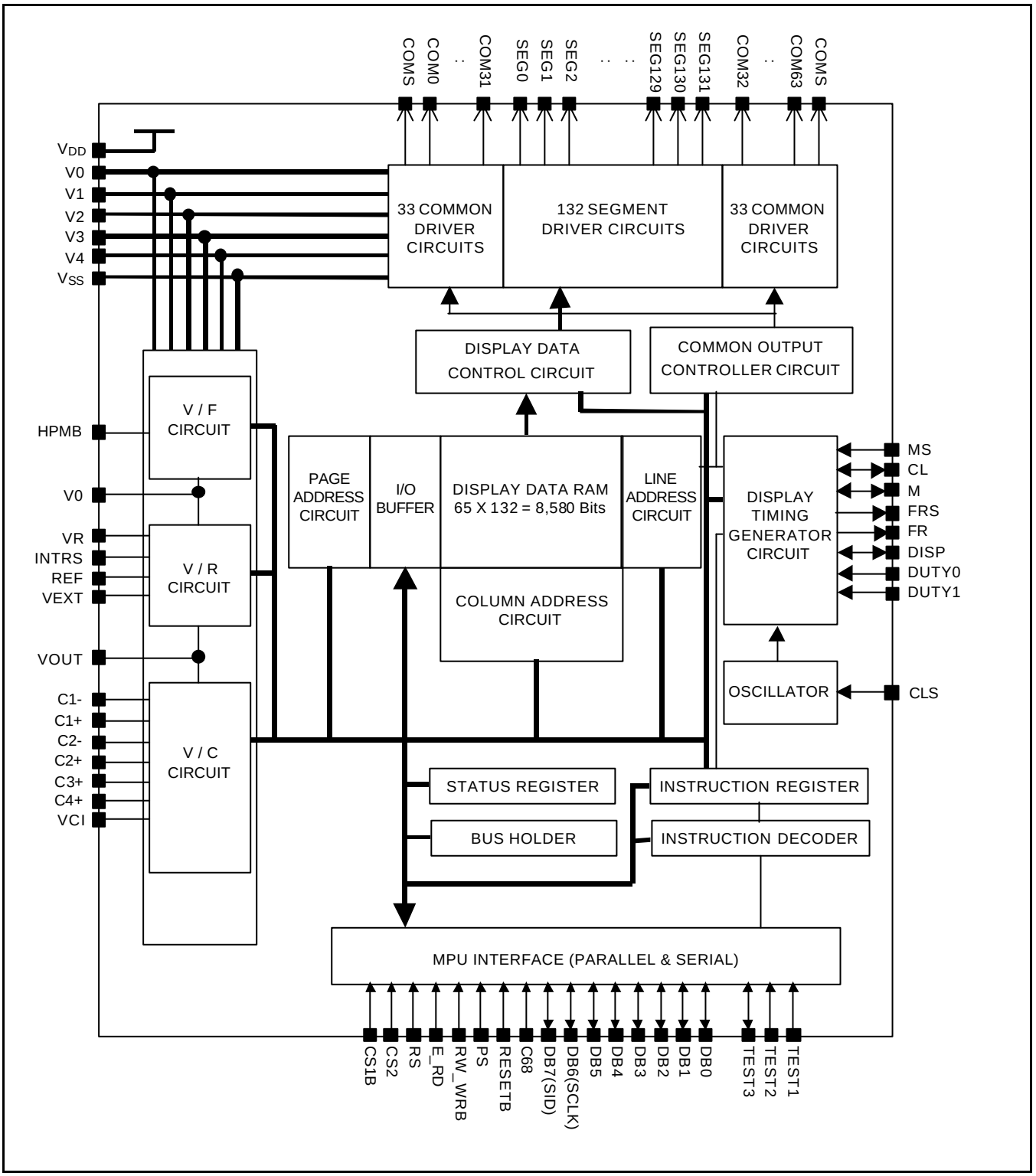


Figure 1. Block Diagram

PAD CONFIGURATION

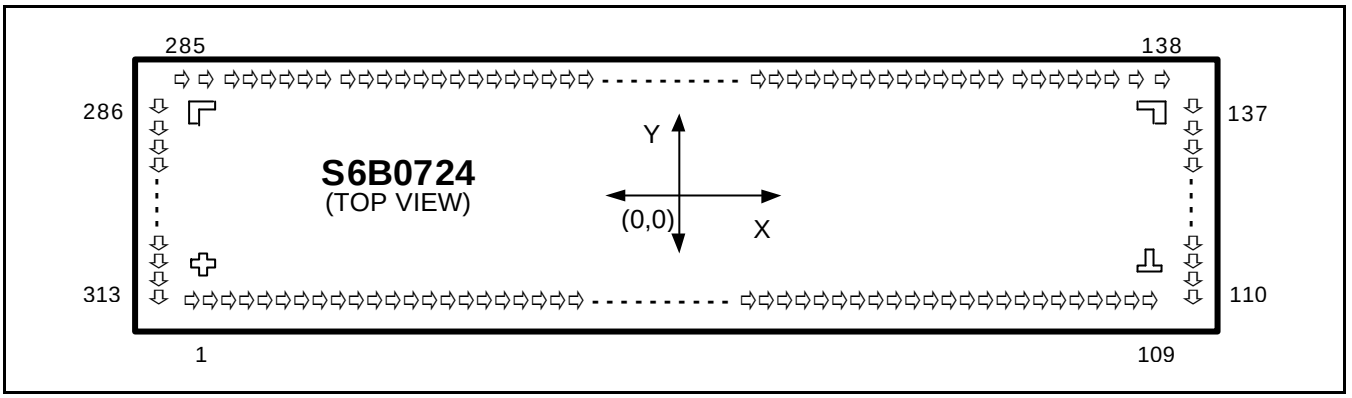
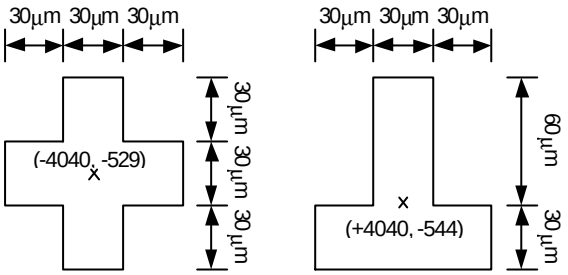


Figure 2. S6B0724 Chip Configuration

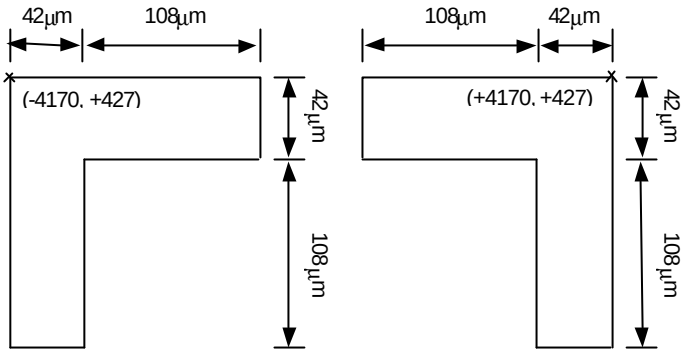
Table 1. S6B0724 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	9680	2030	µm
Pad pitch	1 to 109	70		
	110 to 137, 140 to 283 287 to 313	60		
	137 to 139, 284 to 286	80		
Bumped pad size	1 to 109	50	100	
	110 to 136	122	40	
	140 to 283	40	122	
	287 to 313	122	40	
	138,139,284,285	60	122	
	137, 286	122	60	
Bumped pad height	All pad	14 (Typ.)		

COG Align Key Coordinate



ILB Align Key Coordinate (with Gold Bump*)



*When dsigning electrode pattern must be prohibited on this area (ILB Align Key). If electrode pattern is used for routing over this area, it can be happened pattern-short through bumped pattern on ILB Align Key

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
1	FRS	-3780	-879	51	C4+	-280	-879	101	CLS	3220	-879
2	FR	-3710	-879	52	C4+	-210	-879	102	VSS	3290	-879
3	TEST1	-3640	-879	53	C4+	-140	-879	103	C68	3360	-879
4	TEST2	-3570	-879	54	C3+	-70	-879	104	PS	3430	-879
5	TEST3	-3500	-879	55	C3+	0	-879	105	VDD	3500	-879
6	M	-3430	-879	56	C3+	70	-879	106	HPMB	3570	-879
7	CL	-3360	-879	57	C3+	140	-879	107	VSS	3640	-879
8	DISP	-3290	-879	58	C1-	210	-879	108	INTRS	3710	-879
9	VSS	-3220	-879	59	C1-	280	-879	109	VDD	3780	-879
10	VSS	-3150	-879	60	C1-	350	-879	110	COM31	4693	-780
11	CS1B	-3080	-879	61	C1-	420	-879	111	COM30	4693	-720
12	CS2	-3010	-879	62	C1+	490	-879	112	COM29	4693	-660
13	VDD	-2940	-879	63	C1+	560	-879	113	COM28	4693	-600
14	RESETB	-2870	-879	64	C1+	630	-879	114	COM27	4693	-540
15	RS	-2800	-879	65	C1+	700	-879	115	COM26	4693	-480
16	VSS	-2730	-879	66	C2+	770	-879	116	COM25	4693	-420
17	RW_WRB	-2660	-879	67	C2+	840	-879	117	COM24	4693	-360
18	E_RDB	-2590	-879	68	C2+	910	-879	118	COM23	4693	-300
19	VDD	-2520	-879	69	C2+	980	-879	119	COM22	4693	-240
20	DB0	-2450	-879	70	C2-	1050	-879	120	COM21	4693	-180
21	DB1	-2380	-879	71	C2-	1120	-879	121	COM20	4693	-120
22	DB2	-2310	-879	72	C2-	1190	-879	122	COM19	4693	-60
23	DB3	-2240	-879	73	C2-	1260	-879	123	COM18	4693	0
24	DB4	-2170	-879	74	VDD	1330	-879	124	COM17	4693	60
25	DB5	-2100	-879	75	VEXT	1400	-879	125	COM16	4693	120
26	DB6	-2030	-879	76	VEXT	1470	-879	126	COM15	4693	180
27	DB7	-1960	-879	77	REF	1540	-879	127	COM14	4693	240
28	VSS	-1890	-879	78	VSS	1610	-879	128	COM13	4693	300
29	VDD	-1820	-879	79	V1	1680	-879	129	COM12	4693	360
30	DUTY0	-1750	-879	80	V1	1750	-879	130	COM11	4693	420
31	DUTY1	-1680	-879	81	V1	1820	-879	131	COM10	4693	480
32	VSS	-1610	-879	82	V2	1890	-879	132	COM9	4693	540
33	VDD	-1540	-879	83	V2	1960	-879	133	COM8	4693	600
34	VDD	-1470	-879	84	V2	2030	-879	134	COM7	4693	660
35	VDD	-1400	-879	85	V3	2100	-879	135	COM6	4693	720
36	VDD	-1330	-879	86	V3	2170	-879	136	COM5	4693	780
37	VDD	-1260	-879	87	V3	2240	-879	137	DUMMY1	4693	860
38	VCI	-1190	-879	88	V4	2310	-879	138	DUMMY2	4470	868
39	VCI	-1120	-879	89	V4	2380	-879	139	DUMMY3	4390	868
40	VCI	-1050	-879	90	V4	2450	-879	140	COM4	4310	868
41	VSS	-980	-879	91	V0	2520	-879	141	COM3	4250	868
42	VSS	-910	-879	92	V0	2590	-879	142	COM2	4190	868
43	VSS	-840	-879	93	V0	2660	-879	143	COM1	4130	868
44	VSS	-770	-879	94	VR	2730	-879	144	COM0	4070	868
45	VSS	-700	-879	95	VR	2800	-879	145	COMS	4010	868
46	VOUT	-630	-879	96	VR	2870	-879	146	SEG0	3930	868
47	VOUT	-560	-879	97	VSS	2940	-879	147	SEG1	3870	868
48	VOUT	-490	-879	98	VSS	3010	-879	148	SEG2	3810	868
49	VOUT	-420	-879	99	VDD	3080	-879	149	SEG3	3750	868
50	C4+	-350	-879	100	MS	3150	-879	150	SEG4	3690	868

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
151	SEG5	3630	868	201	SEG55	630	868	251	SEG105	-2370	868
152	SEG6	3570	868	202	SEG56	570	868	252	SEG106	-2430	868
153	SEG7	3510	868	203	SEG57	510	868	253	SEG107	-2490	868
154	SEG8	3450	868	204	SEG58	450	868	254	SEG108	-2550	868
155	SEG9	3390	868	205	SEG59	390	868	255	SEG109	-2610	868
156	SEG10	3330	868	206	SEG60	330	868	256	SEG110	-2670	868
157	SEG11	3270	868	207	SEG61	270	868	257	SEG111	-2730	868
158	SEG12	3210	868	208	SEG62	210	868	258	SEG112	-2790	868
159	SEG13	3150	868	209	SEG63	150	868	259	SEG113	-2850	868
160	SEG14	3090	868	210	SEG64	90	868	260	SEG114	-2910	868
161	SEG15	3030	868	211	SEG65	30	868	261	SEG115	-2970	868
162	SEG16	2970	868	212	SEG66	-30	868	262	SEG116	-3030	868
163	SEG17	2910	868	213	SEG67	-90	868	263	SEG117	-3090	868
164	SEG18	2850	868	214	SEG68	-150	868	264	SEG118	-3150	868
165	SEG19	2790	868	215	SEG69	-210	868	265	SEG119	-3210	868
166	SEG20	2730	868	216	SEG70	-270	868	266	SEG120	-3270	868
167	SEG21	2670	868	217	SEG71	-330	868	267	SEG121	-3330	868
168	SEG22	2610	868	218	SEG72	-390	868	268	SEG122	-3390	868
169	SEG23	2550	868	219	SEG73	-450	868	269	SEG123	-3450	868
170	SEG24	2490	868	220	SEG74	-510	868	270	SEG124	-3510	868
171	SEG25	2430	868	221	SEG75	-570	868	271	SEG125	-3570	868
172	SEG26	2370	868	222	SEG76	-630	868	272	SEG126	-3630	868
173	SEG27	2310	868	223	SEG77	-690	868	273	SEG127	-3690	868
174	SEG28	2250	868	224	SEG78	-750	868	274	SEG128	-3750	868
175	SEG29	2190	868	225	SEG79	-810	868	275	SEG129	-3810	868
176	SEG30	2130	868	226	SEG80	-870	868	276	SEG130	-3870	868
177	SEG31	2070	868	227	SEG81	-930	868	277	SEG131	-3930	868
178	SEG32	2010	868	228	SEG82	-990	868	278	COM32	-4010	868
179	SEG33	1950	868	229	SEG83	-1050	868	279	COM33	-4070	868
180	SEG34	1890	868	230	SEG84	-1110	868	280	COM34	-4130	868
181	SEG35	1830	868	231	SEG85	-1170	868	281	COM35	-4190	868
182	SEG36	1770	868	232	SEG86	-1230	868	282	COM36	-4250	868
183	SEG37	1710	868	233	SEG87	-1290	868	283	COM37	-4310	868
184	SEG38	1650	868	234	SEG88	-1350	868	284	DUMMY4	-4390	868
185	SEG39	1590	868	235	SEG89	-1410	868	285	DUMMY5	-4470	868
186	SEG40	1530	868	236	SEG90	-1470	868	286	DUMMY6	-4693	860
187	SEG41	1470	868	237	SEG91	-1530	868	287	COM38	-4693	780
188	SEG42	1410	868	238	SEG92	-1590	868	288	COM39	-4693	720
189	SEG43	1350	868	239	SEG93	-1650	868	289	COM40	-4693	660
190	SEG44	1290	868	240	SEG94	-1710	868	290	COM41	-4693	600
191	SEG45	1230	868	241	SEG95	-1770	868	291	COM42	-4693	540
192	SEG46	1170	868	242	SEG96	-1830	868	292	COM43	-4693	480
193	SEG47	1110	868	243	SEG97	-1890	868	293	COM44	-4693	420
194	SEG48	1050	868	244	SEG98	-1950	868	294	COM45	-4693	360
195	SEG49	990	868	245	SEG99	-2010	868	295	COM46	-4693	300
196	SEG50	930	868	246	SEG100	-2070	868	296	COM47	-4693	240
197	SEG51	870	868	247	SEG101	-2130	868	297	COM48	-4693	180
198	SEG52	810	868	248	SEG102	-2190	868	298	COM49	-4693	120
199	SEG53	750	868	249	SEG103	-2250	868	299	COM50	-4693	60
200	SEG54	690	868	250	SEG104	-2310	868	300	COM51	-4693	0

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
301	COM52	-4693	-60								
302	COM53	-4693	-120								
303	COM54	-4693	-180								
304	COM55	-4693	-240								
305	COM56	-4693	-300								
306	COM57	-4693	-360								
307	COM58	-4693	-420								
308	COM59	-4693	-480								
309	COM60	-4693	-540								
310	COM61	-4693	-600								
311	COM62	-4693	-660								
312	COM63	-4693	-720								
313	COMS	-4693	-780								

PIN DESCRIPTION

POWER SUPPLY

Table 3. Power Supply Pins Description

<table>
<tr><th>Name</th><th>I/O</th><th colspan="5">Description</th></tr>
<tr><td>VDD</td><td>Supply</td><td colspan="5">Power supply</td></tr>
<tr><td>VSS</td><td>Supply</td><td colspan="5">Ground</td></tr>
<tr><td rowspan="8">V0
V1
V2
V3
V4</td><td rowspan="8">I/O</td><td colspan="5">LCD driver supply voltages
The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application.
Voltages should have the following relationship;
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.</td></tr>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/9 bias</td><td>(8/9) x V0</td><td>(7/9) x V0</td><td>(2/9) x V0</td><td>(1/9) x V0</td></tr>
<tr><td>1/8 bias</td><td>(7/8) x V0</td><td>(6/8) x V0</td><td>(2/8) x V0</td><td>(1/8) x V0</td></tr>
<tr><td>1/7 bias</td><td>(6/7) x V0</td><td>(5/7) x V0</td><td>(2/7) x V0</td><td>(1/7) x V0</td></tr>
<tr><td>1/6 bias</td><td>(5/6) x V0</td><td>(4/6) x V0</td><td>(2/6) x V0</td><td>(1/6) x V0</td></tr>
<tr><td>1/5 bias</td><td>(4/5) x V0</td><td>(3/5) x V0</td><td>(2/5) x V0</td><td>(1/5) x V0</td></tr>
</table>

LCD DRIVER SUPPLY

Table 4. LCD Driver Supply Pins Description

Name	I/O	Description
C1-	O	Capacitor 1 negative connection pin for voltage converter
C1+	O	Capacitor 1 positive connection pin for voltage converter
C2-	O	Capacitor 2 negative connection pin for voltage converter
C2+	O	Capacitor 2 positive connection pin for voltage converter
C3+	O	Capacitor 3 positive connection pin for voltage converter
C4+	O	Capacitor 4 positive connection pin for voltage converter
VOUT	I/O	Voltage converter input / output pin Connect this pin to V_{SS} through capacitor.
VR	I	V0 voltage adjustment pin It is valid only when internal voltage regulator resistors are not used (INTRS = "L").
VCI	I	This is the reference voltage for the voltage converter circuit for the LCD drive. Whether internal voltage converter use or not use, this pin should be fixed. The voltage should have the following range: 2.4V ≤ VCI ≤ 5.5V
VEXT	I	This is the externally input reference voltage (V_{REF}) for the internal voltage regulator. It is valid only when external V_{REF} is used (REF = "L"). When using internal V_{REF}, this pin is Open
REF	I	Select the external V_{REF} voltage via VEXT pin – REF = "L": using the external V_{REF} – REF = "H": using the internal V_{REF}

SYSTEM CONTROL

Table 5. System Control Pins Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>MS</td><td>I</td><td>Master / slave mode select input
Master makes some signals for display, and slave gets them. This is for display synchronization.
– MS = "H": master mode
– MS = "L": slave mode
The following table depends on the MS status.
<table>
<tr><th>MS</th><th>CLS</th><th>OSC circuit</th><th>Power supply circuit</th><th>CL</th><th>M</th><th>FR</th><th>DISP</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>-</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>CLS</td><td>I</td><td>Built-in oscillator circuit enable / disable select pin
– CLS = "H": enable
– CLS = "L": disable (external display clock input to CL pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input / output pin
When the S6B0724 is used in master/slave mode (multi-chip), the CL pins must be connected each other.</td></tr>
<tr><td>M</td><td>I/O</td><td>LCD AC Signal input / output pin
When the S6B0724 is used in master/slave mode (multi-chip), the M pins must be connected each other.
– MS = "H": output
– MS = "L": input</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver segment output pin
This pin is used together with the FR pin.</td></tr>
<tr><td>FR</td><td>O</td><td>Static driver common output pin
This pin is used together with the FRS pin.</td></tr>
<tr><td>DISP</td><td>I/O</td><td>LCD display blanking control input / output
When S6B0724 is used in master / slave mode (multi-chip), the DISP pins must be connected each other.
– MS = "H": output
– MS = "L": input</td></tr>
<tr><td>INTRS</td><td>I</td><td>Internal resistor select pin
This pin selects the resistors for adjusting V0 voltage level and is valid only in master operation.
– INTRS = "H": use the internal resistors
– INTRS = "L": use the external resistors
V0 voltage is controlled by VR pin and external resistive divider.</td></tr>
</table>

Table 5. System Control Pins Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="3">Description</th></tr>
<tr><td rowspan="7">DUTY0
DUTY1</td><td rowspan="7">I</td><td colspan="3">The LCD driver duty ratio depends on the following table.</td></tr>
<tr><td>DUTY1</td><td>DUTY0</td><td>Duty ratio</td></tr>
<tr><td>L</td><td>L</td><td>1/33</td></tr>
<tr><td>L</td><td>H</td><td>1/49</td></tr>
<tr><td>H</td><td>L</td><td>1/55</td></tr>
<tr><td>H</td><td>H</td><td>1/65</td></tr>
<tr><td colspan="3"></td></tr>
<tr><td>HPMB</td><td>I</td><td colspan="3">Power control pin of the power supply circuits for LCD driver
– HPMB = "H": normal mode
– HPMB = "L": high power mode
This pin is valid only in master operation.</td></tr>
</table>

MICROPROCESSOR INTERFACE

Table 6. Microprocessor Interface Pins Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESETB</td><td>I</td><td>Reset input pin
When RESETB is "L", initialization is executed.</td></tr>
<tr><td rowspan="5">PS</td><td rowspan="5">I</td><td>Parallel / Serial data input select input
<table>
<tr><td>PS</td><td>Interface mode</td><td>Chip select</td><td>Data / instruction</td><td>Data</td><td>Read / Write</td><td>Serial clock</td></tr>
<tr><td>H</td><td>Parallel</td><td>CS1B, CS2</td><td>RS</td><td>DB0 to DB7</td><td>E_RDB
RW_WRB</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>CS1B, CS2</td><td>RS</td><td>SID (DB7)</td><td>Write only</td><td>SCLK (DB6)</td></tr>
</table></td></tr>
<tr><td>*NOTE: In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RDB and RW_WRB must be fixed to either "H" or "L".</td></tr>
<tr><td rowspan="3">C68</td><td rowspan="3">I</td><td rowspan="3">Microprocessor Interface Select input pin in parallel mode
– C68 = "H": 6800-series MPU interface
– C68 = "L": 8080-series MPU interface</td></tr>
<tr><td rowspan="3">CS1B
CS2</td><td rowspan="3">I</td><td rowspan="3">Chip select input pins
Data / instruction I/O is enabled only when CS1B is "L" and CS2 is "H". When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td rowspan="3">RS</td><td rowspan="3">I</td><td rowspan="3">Register select input pin
– RS = "H": DB0 to DB7 are display data
– RS = "L": DB0 to DB7 are control data</td></tr>
<tr><td rowspan="4">RW_WRB</td><td rowspan="4">I</td><td>Read / Write execution control pin
<table>
<tr><td>C68</td><td>MPU Type</td><td>RW_WRB</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read / Write control input pin
– RW = "H": read
– RW = "L": write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WRB</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WRB signal.</td></tr>
</table></td></tr>
<tr><td></td></tr>
</table>

Table 6. Microprocessor Interface Pins Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="5">E_RDB</td><td rowspan="5">I</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>C68</td><td>MPU Type</td><td>E_RDB</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
– RW = "H": When E is "H", DB0 to DB7 are in an output status.
– RW = "L": The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RDB</td><td>Read enable clock input pin
When /RDB is "L", DB0 to DB7 are in an output status.</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td colspan="4">8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L");
– DB0 to DB5: high impedance
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>TEST1
to
TEST3</td><td>I/O</td><td colspan="4">These are pins for IC chip testing.
They are set to Open.</td></tr>
</table>

LCD DRIVER OUTPUTS

Table 7. LCD Driver Output Pins Description

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="9">SEG0
to
SEG131</td><td rowspan="9">O</td><td colspan="4">LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.</td></tr>
<tr><td rowspan="2">Display data</td><td rowspan="2">M</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td><td>VSS</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td rowspan="8">COM0
to
COM63</td><td rowspan="8">O</td><td colspan="4">LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.</td></tr>
<tr><td>Scan data</td><td>M</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">VSS</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">VSS</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>COMS</td><td>O</td><td colspan="4">Common output for the icons
The output signals of two pins are same. When not used, these pins should be left Open. In multi-chip (master / slave) mode, all COMS pin on both master and slave units are the same signal.</td></tr>
</table>

NOTE: **DUMMY** - **These pins should be opened (floated).**

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There are CS1B and CS2 pins for chip selection. The S6B0724 can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, RS, E_RDB, and RW_WRB inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

S6B0724 has three types of interface with an MPU, which are one serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in table 8.

Table 8. Parallel / Serial Interface Mode

PS	Type	CS1B	CS2	C68	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	*×	Serial-mode

*×: Don't care

Parallel interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68 as shown in table 9. The type of data transfer is determined by signals at RS, E_RDB and RW_WRB as shown in Table 10.

Table 9. Microprocessor Selection for Parallel Interface

C68	CS1B	CS2	RS	E_RDB	RW_WRB	DB0 to DB7	MPU bus
H	CS1B	CS2	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	RS	/RDB	/WRB	DB0 to DB7	8080-series

Table 10. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RDB (E)	RW_WRB (RW)	E_RDB (/RDB)	RW_WRB (/WRB)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

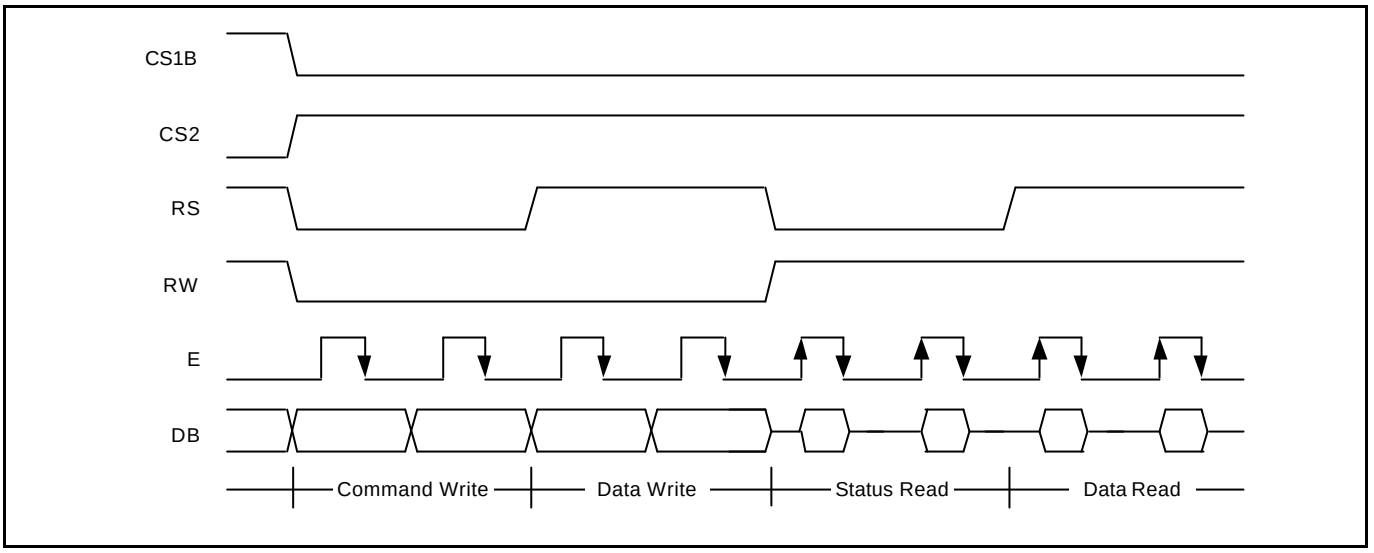


Figure 3. 6800-Series MPU Interface protocol (PS="H", MI="H")

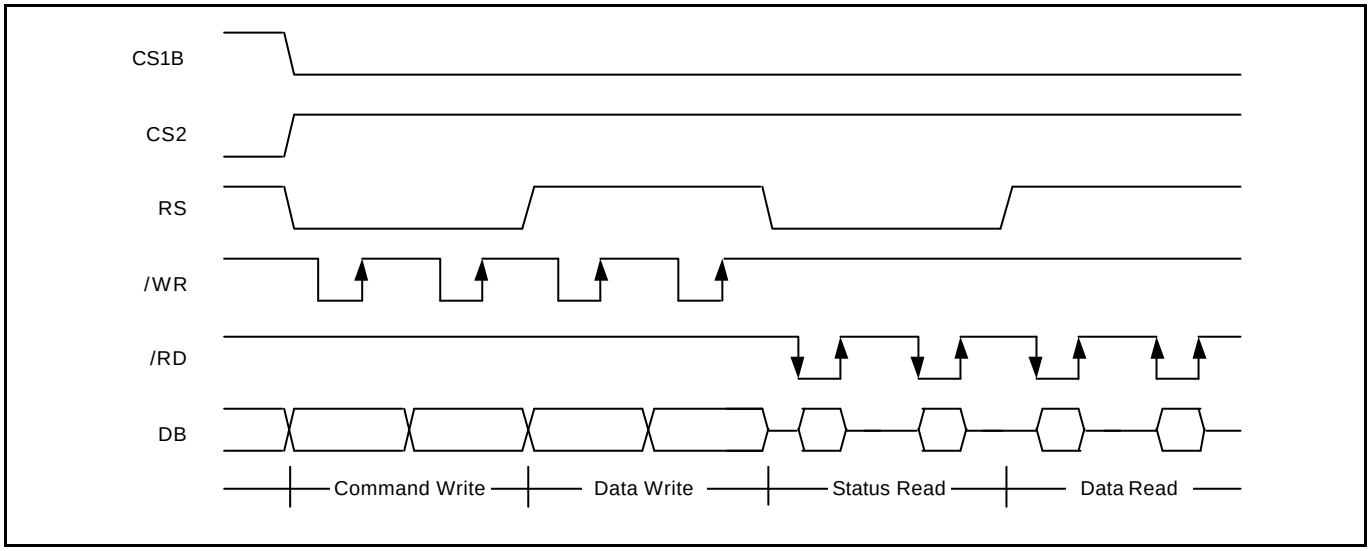


Figure 4. 8080-Series MPU Interface Protocol (PS="H", MI="L")

Serial Interface (PS = "L")

When the S6B0724 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

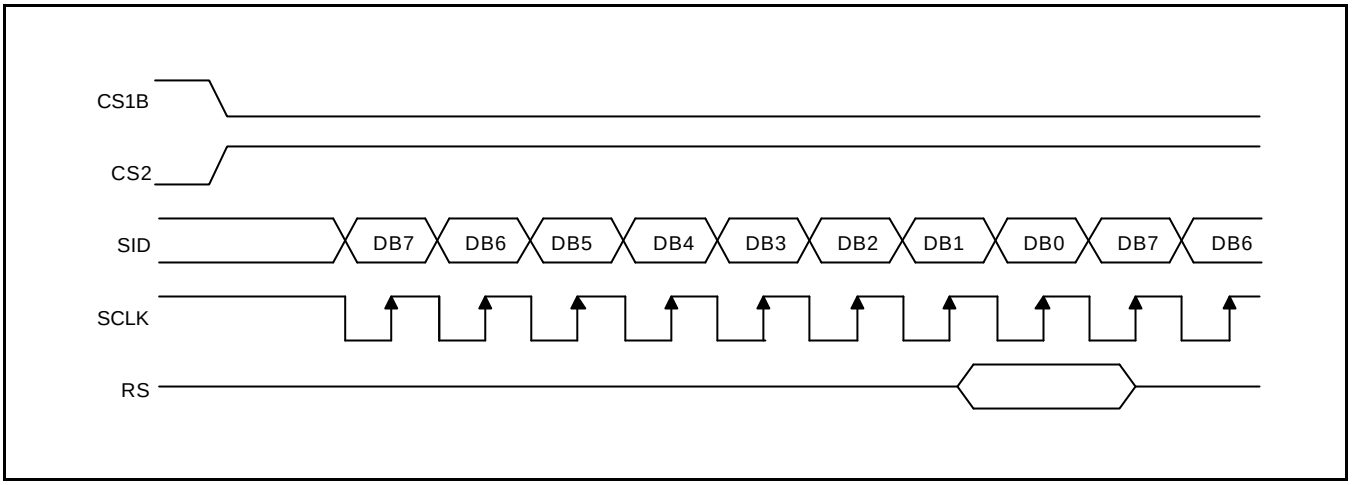


Figure 5. Serial Interface Timing

Busy Flag

The Busy Flag indicates whether the S6B0724 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The S6B0724 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 4. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 5. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

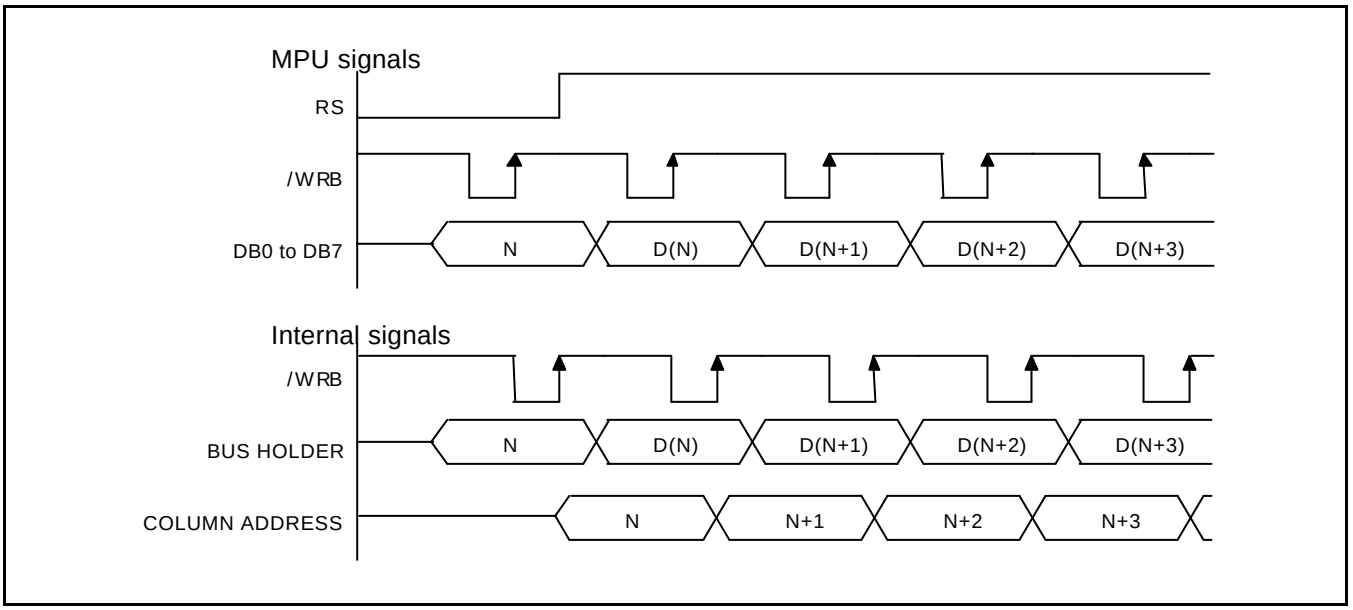


Figure 6. Write Timing

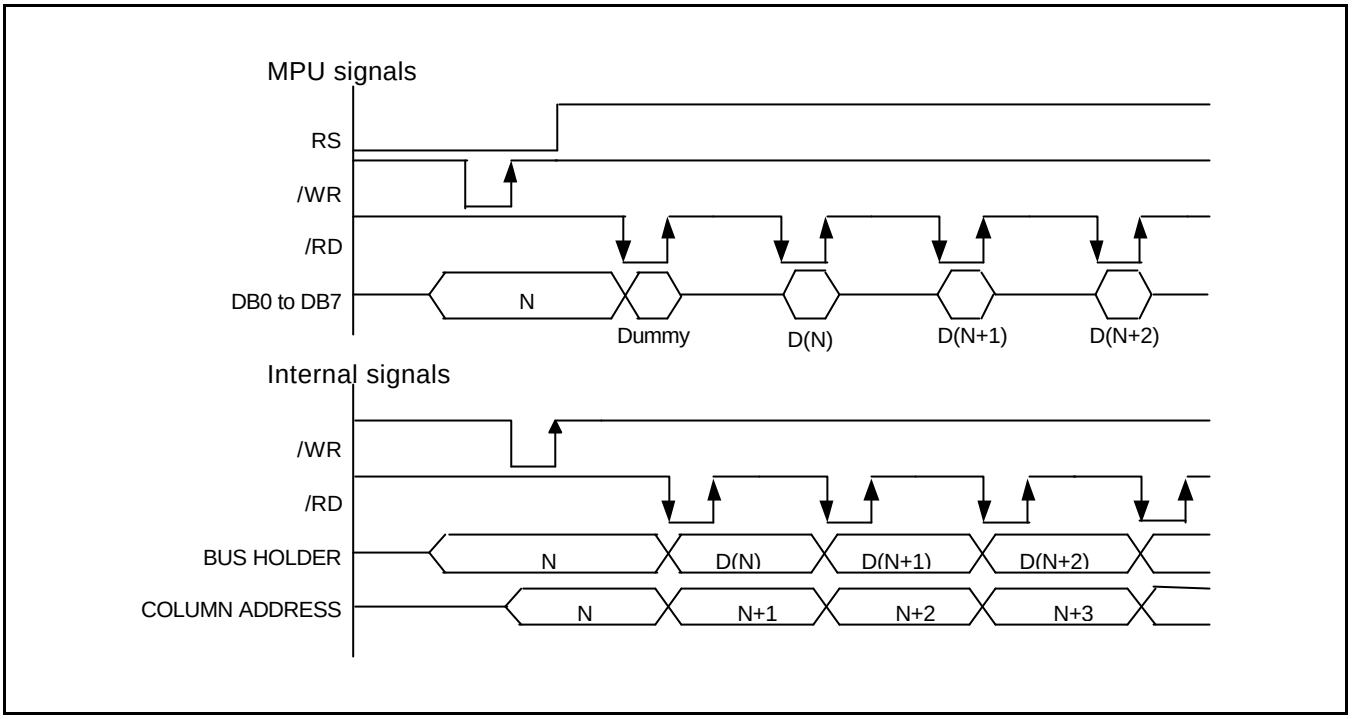


Figure 7. Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 65-row by 132-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in figure 6. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

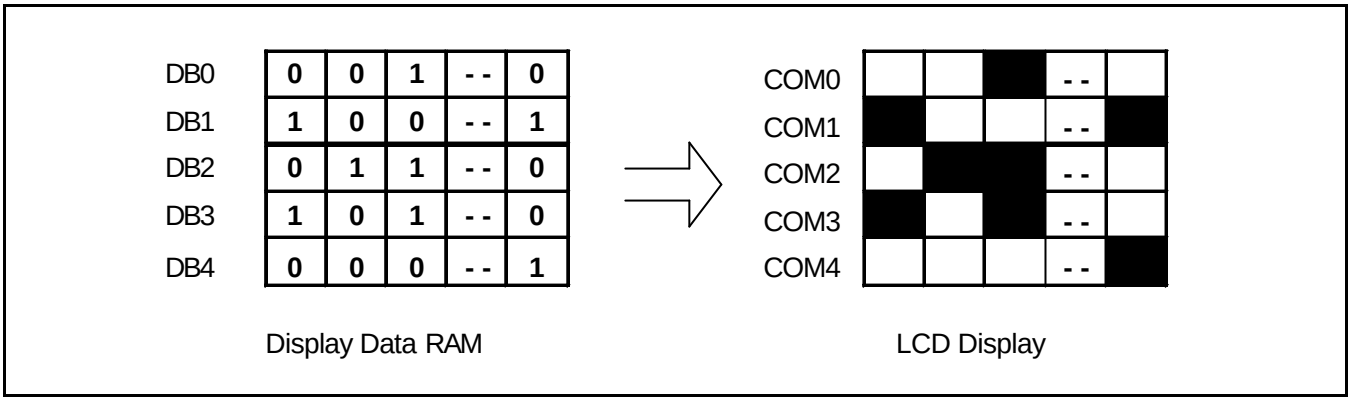


Figure 8. RAM-to-LCD Data Transfer

Page Address Circuit

This circuit is for providing a Page Address to DISPLAY-DATA-RAM shown in figure 8. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 8 (DB3 is "H", but DB2, DB1 and DB0 are "L") is a special RAM area for the icons and display data DB0 is only valid. When Page Address is above 8, it is impossible to access to on-chip RAM.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 8. It incorporates 6-bit line address register changed by only the initial display line instruction and 6-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the Line Address for transferring the 132-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

Column Address circuit has an 8-bit preset counter that provides column address to the Display Data RAM as shown in figure 8. When set Column Address MSB / LSB instruction is issued, 8-bit [Y7:Y0] is updated. And, since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 84H. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the Column Address counter is independent of page address register.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC Select instruction. Refer to the following figure 7.

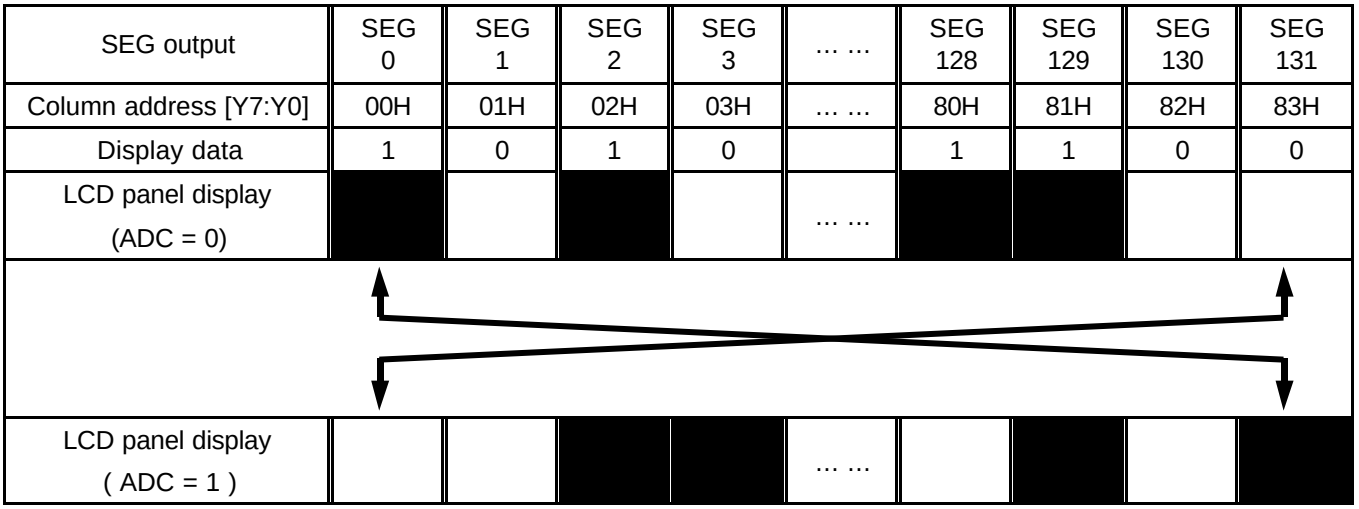


Figure 9. The Relationship between the Column Address and the Segment Outputs

Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

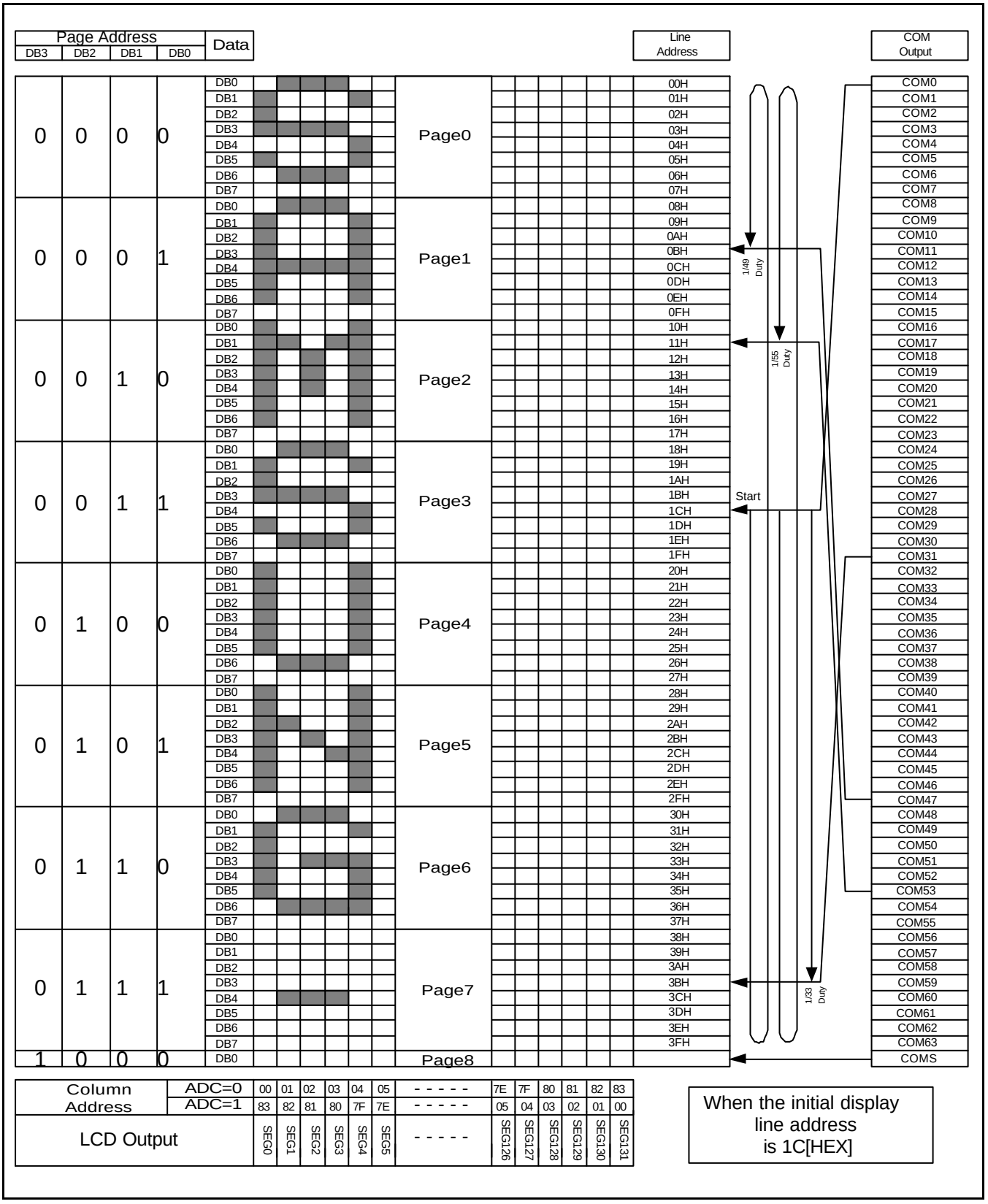


Figure 10. Display Data RAM Map

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip oscillator and its frequency is nearly independent of V_{DD}. This oscillator signal is used in the voltage converter and display timing generation circuit. The oscillator circuit is only enabled when MS = "H" and CLS = "H". When on-chip oscillator is not used, CLS pin must be "L" condition. In this time, external clock must be input from CL pin

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL generated by oscillation clock, generates a clock to the line counter and a latch signal to the display data latch. The line address of on-chip RAM is generated in synchronization with the display dock (CL) and the 132-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data which is read to the LCD driver is completely independent of the access to the display data RAM from the microprocessor. The LCD AC signal, M is generated from the display clock. 2-frame AC driver waveforms with internal timing signal are shown in figure 9.

In a multiple chip configuration, the slave chip requires the M, CL and DISP signals from the master. Table 11 shows the M, SYNC, CL, and DISP status.

Table 11. Master and Slave Timing Signal Status

Operation mode	Oscillator	M	CL	DISP
Master	ON (internal clock used)	Output	Output	Output
	OFF(external clock used)	Output	Input	Output
Slave	-	Input	Input	Input

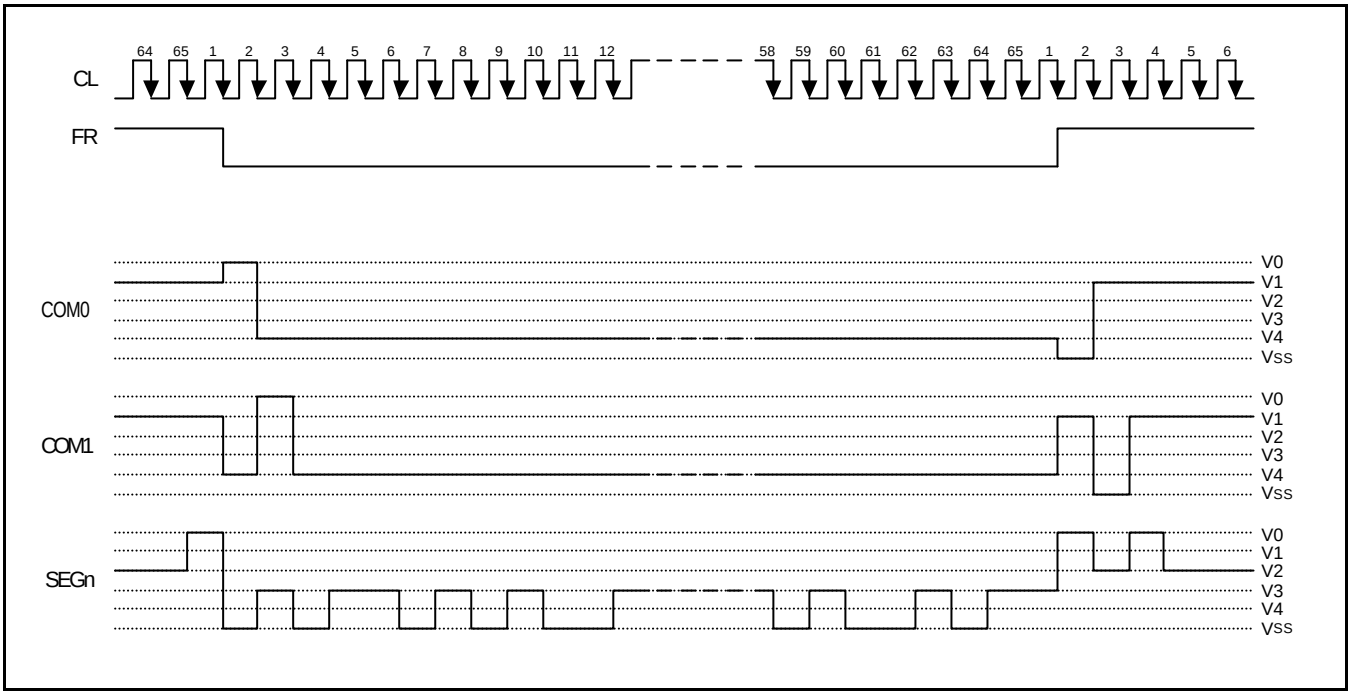


Figure 11. 2-frame AC Driving Waveform (Duty Ratio = 1/65)

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. SHL select Instruction specifies the scanning direction of the common output pins.

Table 12. The Relationship between Duty Ratio and Common Output

Duty	SHL	Common output pins							
		COM [0:15]	COM [16:23]	COM [24:26]	COM [27:36]	COM [37:39]	COM [40:47]	COM [48:63]	COMS
1/33	0	COM[0:15]	*NC					COM[16:31]	COMS
	1	COM[31:16]	*NC					COM[15:0]	
1/49	0	COM[0:23]		*NC			COM[24:47]		COMS
	1	COM[47:24]		*NC			COM[23:0]		
1/55		COM[0:26]			*NC	COM[27:53]			COMS
		COM[53:27]			*NC	COM[26:0]			
1/65	0	COM[0:63]							COMS
	1	COM[63:0]							

*NC: No Connection

LCD DRIVER CIRCUIT

This driver circuit is configured by 66-channel (including 2 COMS channels) common driver and 132-channel segment driver. This LCD panel driver voltage depends on the combination of display data and FR signal.

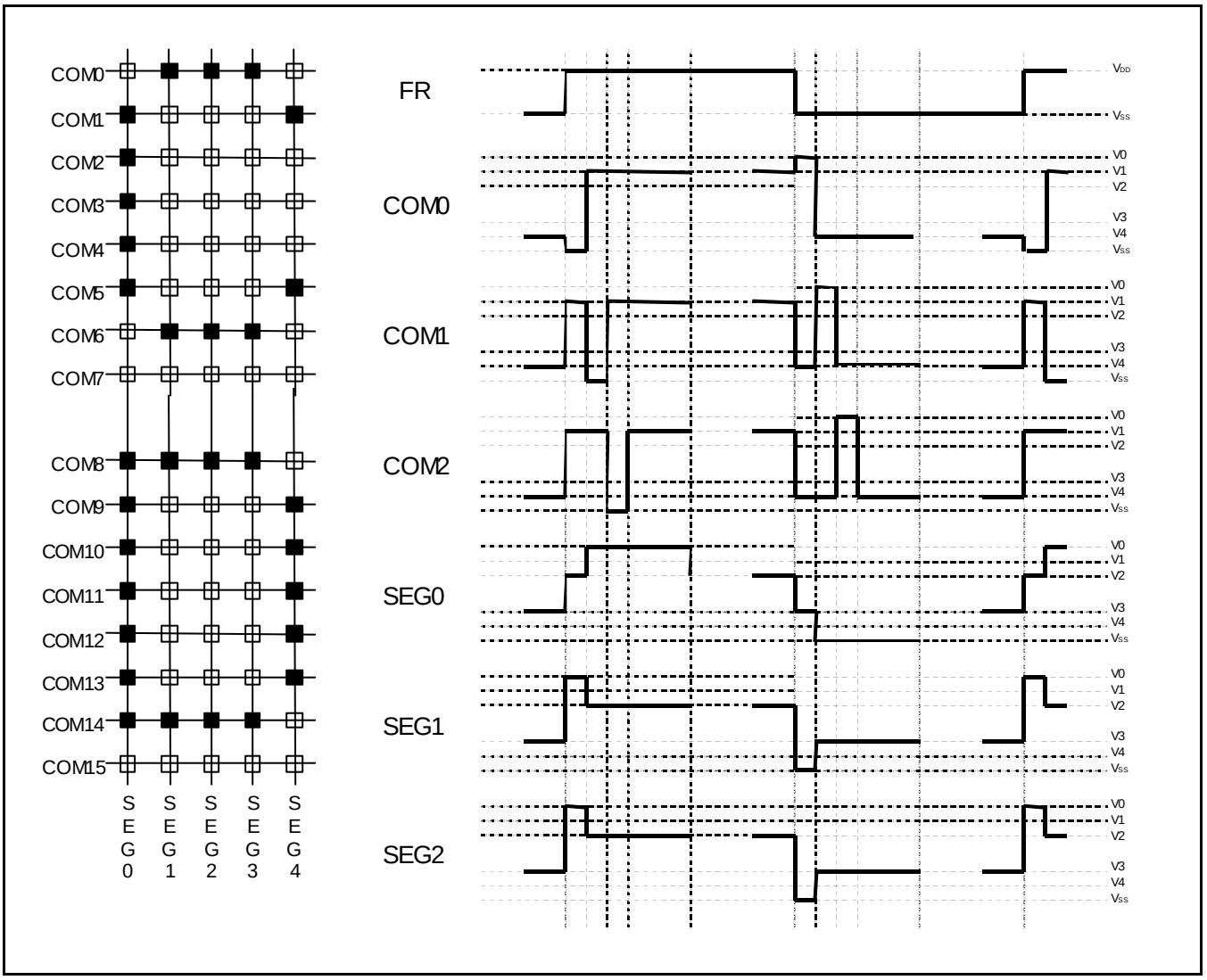


Figure 12. Segment and Common Timing

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to "Instruction Description". Table 13 shows the referenced combinations in using Power Supply circuits.

Table 13. Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VCI and VSS to 2, 3, 4 or 5 times toward positive side and boosted voltage is outputted from VOUT pin.

[C1 = 1.0 to 4.7 μF]

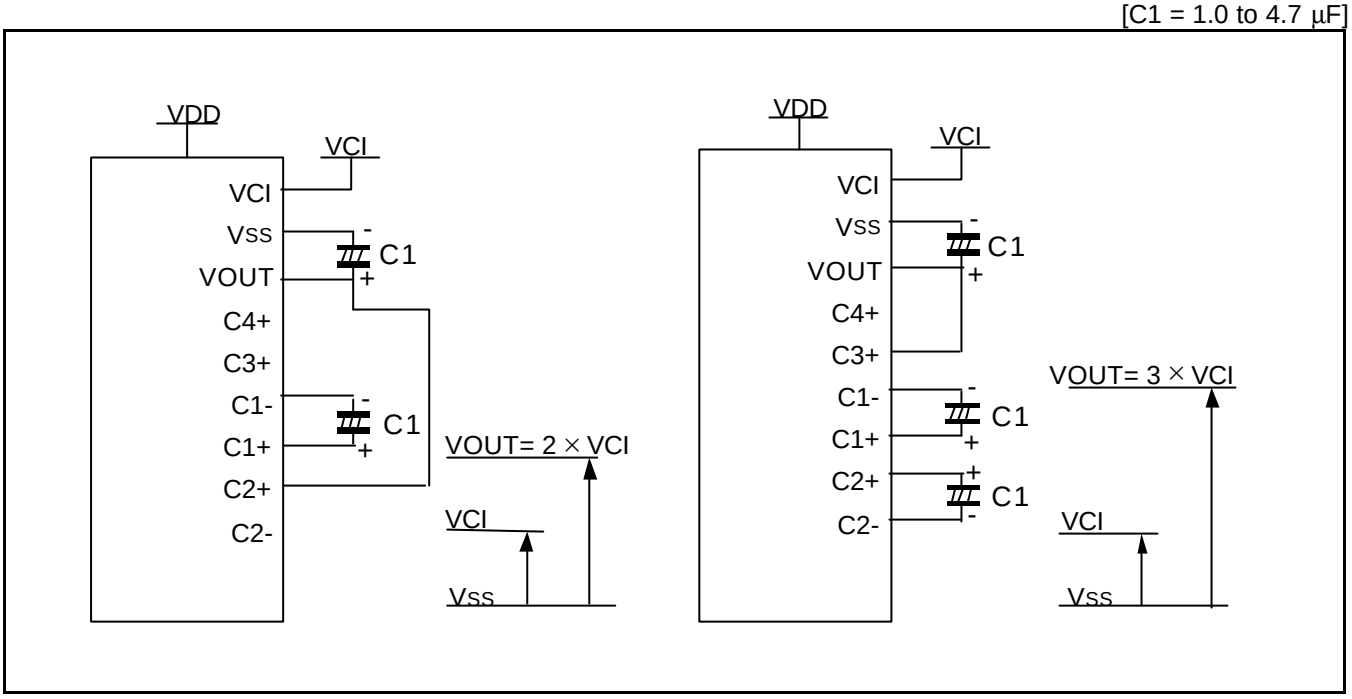


Figure 13. Two Times Boosting Circuit

Figure 14. Three Times Boosting Circuit

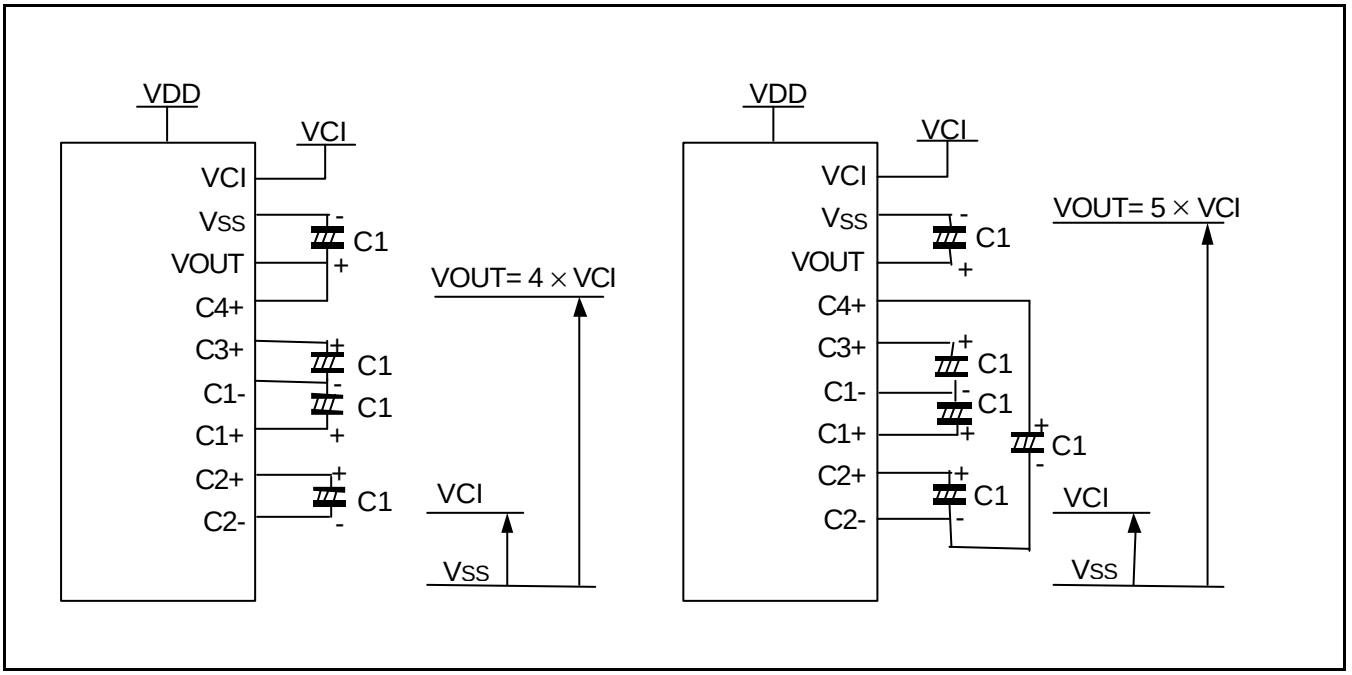


Figure 15. Four Times Boosting Circuit

Figure 16. Five Times Boosting Circuit

* The VCI voltage range must be set so that the VOUT voltage does not exceed the absolute maximum rated value

SAMSUNG ELECTRONICS

Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in figure 15, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And V_{EV} called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta = 25°C is shown in table 14-1.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 1)}$$

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{162}\right) \times V_{REF} \quad [V] \text{ ------ (Eq. 2)}$$

Table 14-1. V_{REF} Voltage at Ta = 25 °C

REF	Temp. coefficient	V_{REF} [V]
H	-0.05% / °C	2.1
L	External input	VEXT

Table 14-2. Electronic Contrast Control Register (64 Steps)

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (a)	V0	Contrast
0	0	0	0	0	0	0	Minimum	Low
0	0	0	0	0	1	1		
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	32 (default)	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	62		
1	1	1	1	1	1	63	Maximum	High

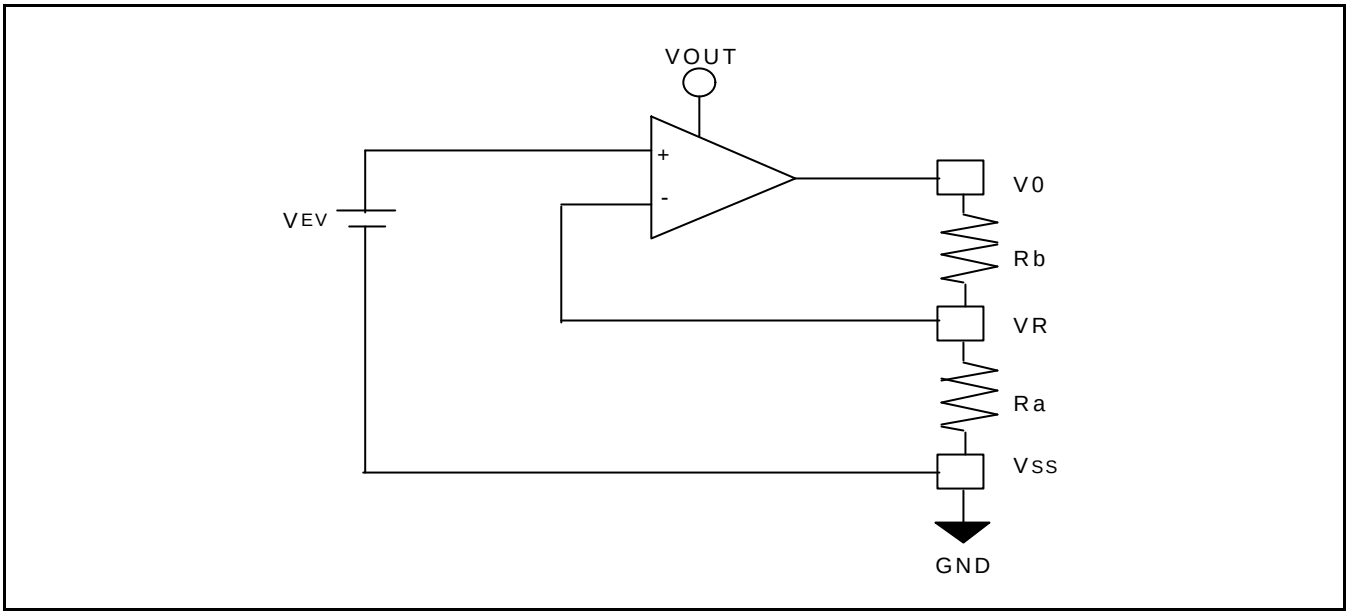


Figure 17. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb. (INTRS = "H")

When INTRS pin is "H", resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 15. Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1+(Rb / Ra)	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.4

The following figure shows V0 voltage measured by adjusting internal regulator resistor ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

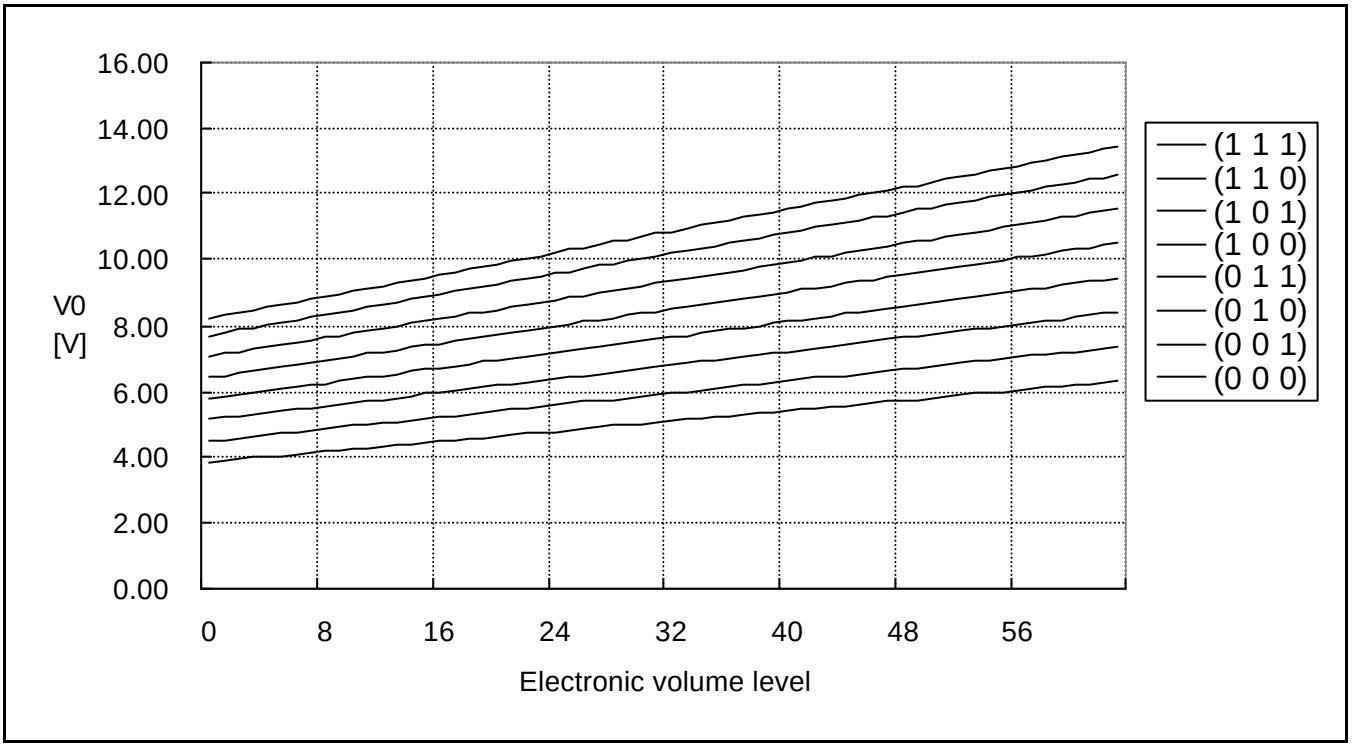


Figure 18. Electronic Volume Level

In Case of Using External Resistors, Ra and Rb. (INTRS = "L")

When INTRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 uA

From Eq. 1

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 3)}$$

From Eq. 2

$$V_{EV} = \left(1 - \frac{(63 - 32)}{162}\right) \times 2.1 \cong 1.698 \quad [V] \text{ ------ (Eq. 4)}$$

From requirement 3.

$$\frac{10}{Ra + Rb} = 1 \text{ [uA]} \quad \text{------ (Eq. 5)}$$

From equations Eq. 3, 4 and 5

$Ra \cong 1.69$ [MΩ]

$Rb \cong 8.31$ [MΩ]

The following table shows the range of V0 depending on the above requirements.

Table 16. V0 Depending on Electronic Volume Level

	Electronic volume level				
	0	**.....**	**32**	**.....**	**63**
V0	7.57	.....	10.00	.....	12.43

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4) and those output impedance are converted by the Voltage Follower for increasing drive capability. The following table shows the relationship between V1 to V4 level and each duty ratio.

Table 17. The Relationship between V1 to V4 Level and Duty Ratio

Duty ratio	DUTY1	DUTY0	LCD bias	V1	V2	V3	V4
1/33	L	L	1/5	(4/5) x V0	(3/5) x V0	(2/5) x V0	(1/5) x V0
			1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
1/49	L	H	1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
			1/8	(7/8) x V0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1/55	H	L	1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
			1/8	(7/8) x V0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1/65	H	H	1/7	(6/7) x V0	(5/7) x V0	(2/7) x V0	(1/7) x V0
			1/9	(8/9) x V0	(7/9) x V0	(2/9) x V0	(1/9) x V0

High Power Mode

The power supply circuit equipped in the S6B0724 for LCD drive has very low power consumption (in normal mode: HPMB = "H"). If use for LCD panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the HPMB pin to "L" (high power mode) can improve the quality of the display. Moreover, if the quality of display is inadequate even after High Power mode has been set, then it is necessary to add a liquid crystal drive power supply externally (Vout or V0 or V1 / V2 / V3 / V4).

REFERENCE CIRCUIT EXAMPLES

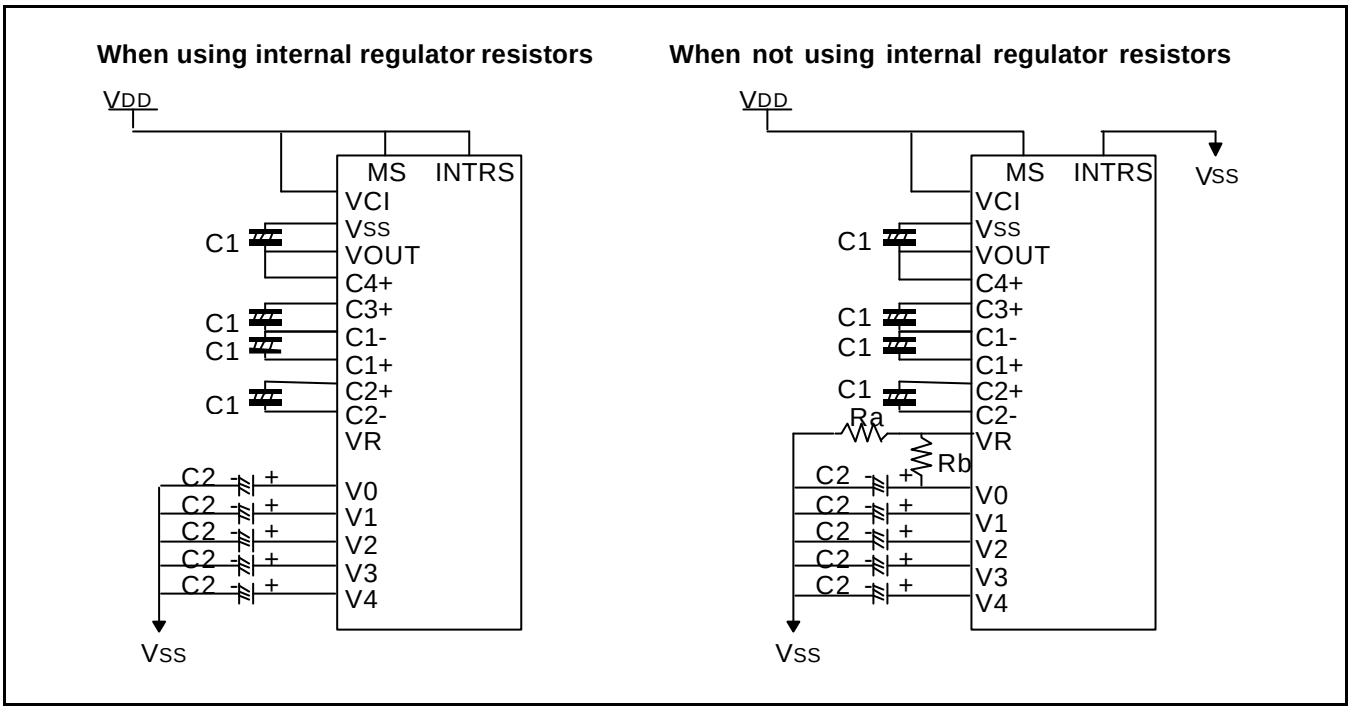


Figure 19. When Using all Internal LCD Power Circuits (VCI = VDD, 4-time V/C: ON, V/R: ON, V/F: ON)

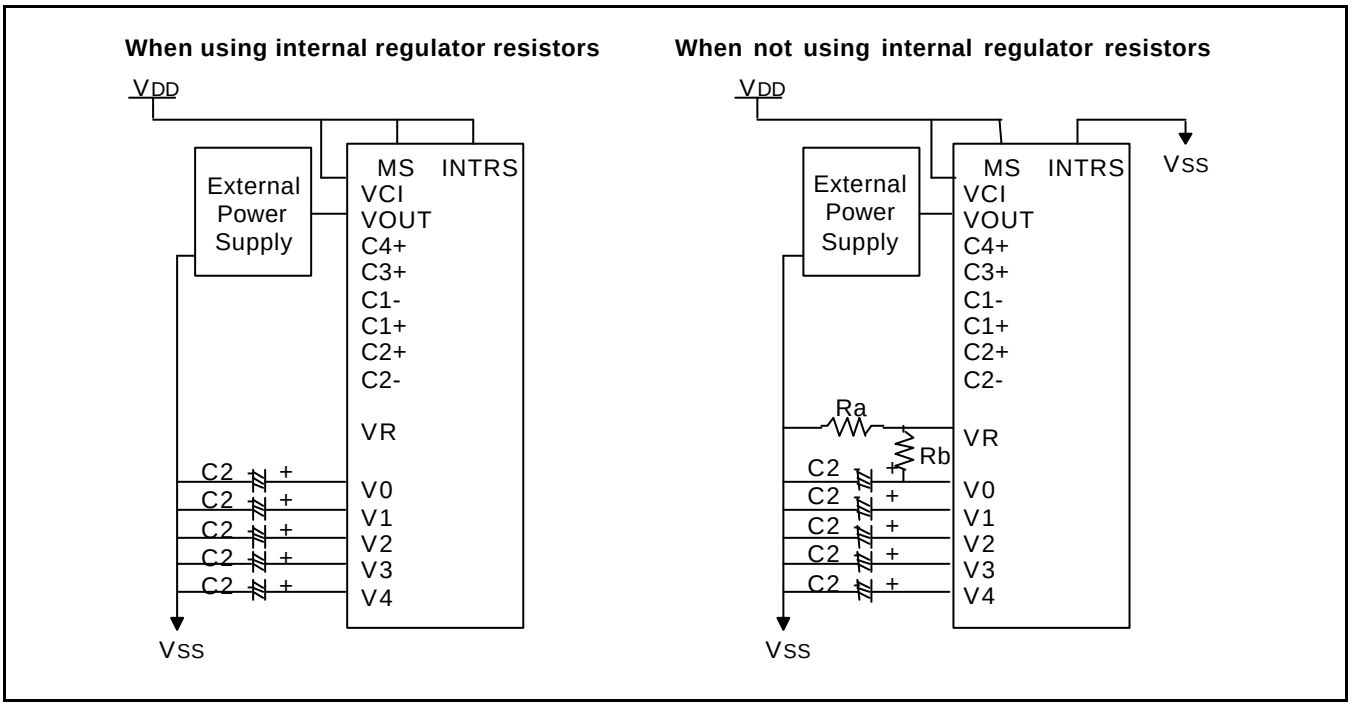


Figure 20. When Using some Internal LCD Power Circuits (VCI = VDD, V/C: OFF, V/R: ON, V/F: ON)

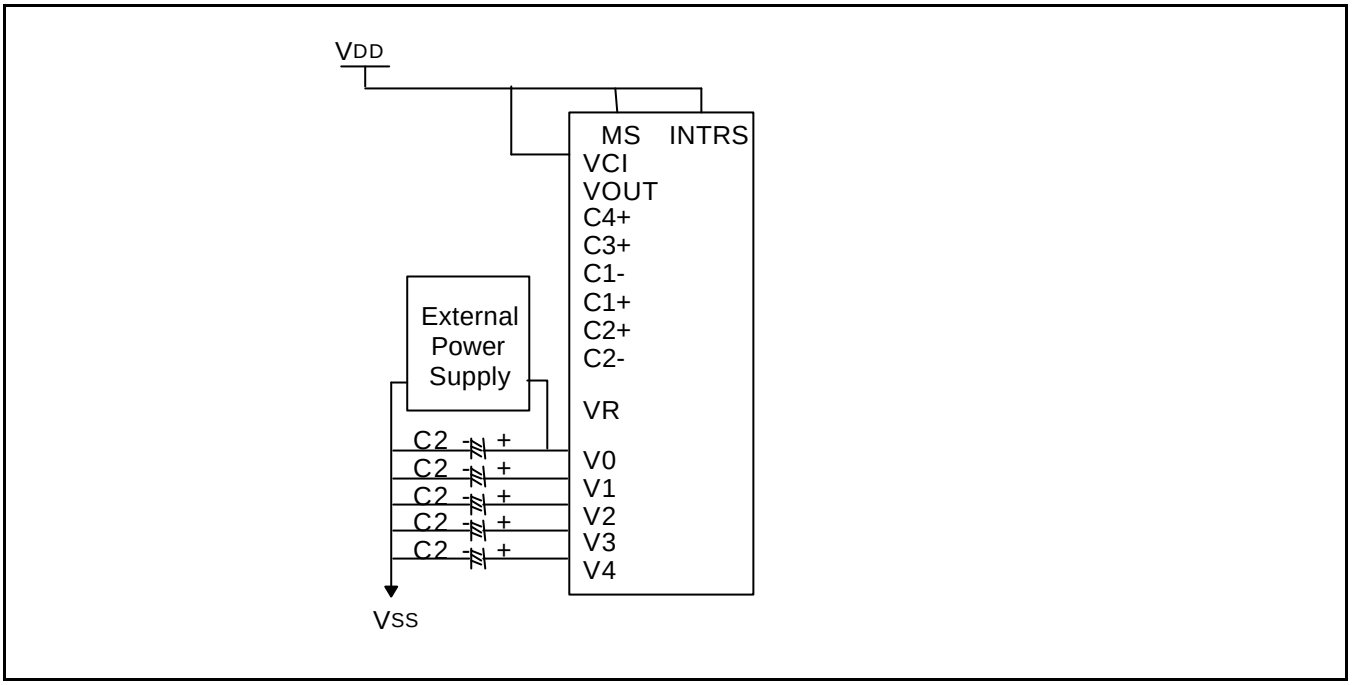
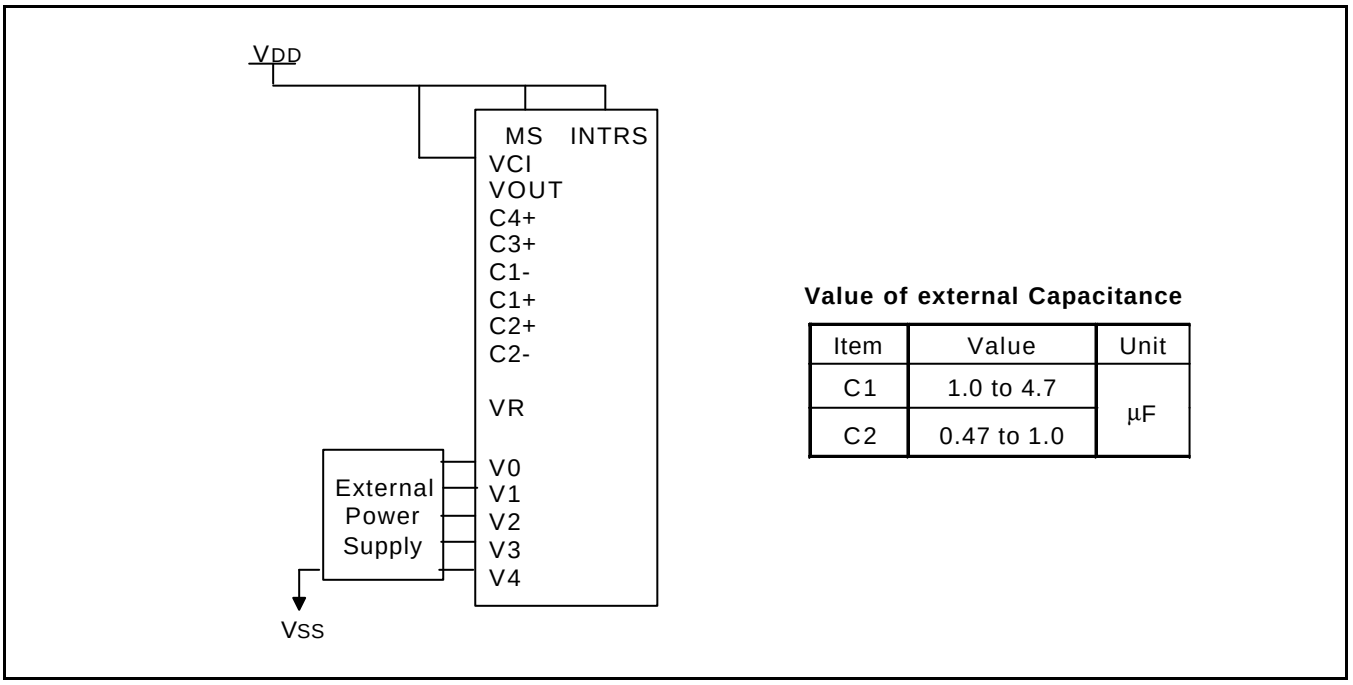


Figure 21. When Using some Internal LCD Power Circuits (VCI = VDD, V/C: OFF, V/R: OFF, V/F: ON)



Value of external Capacitance

Item	Value	Unit
C1	1.0 to 4.7	µF
C2	0.47 to 1.0	

Figure 22. When Not Using any Internal LCD Power Supply Circuits

(VCI = VDD, V/C: OFF, V/R: OFF, V/F: OFF)

* C1 and C2 are determined by the size of the LCD being driven.
  Select a value that will stabilize the liquid crystal drive voltage.

RESET CIRCUIT

Setting RESETB to "L" or Reset instruction can initialize internal function.
When RESETB becomes "L", following procedure is occurred.

Display ON / OFF: OFF
Entire display ON / OFF: OFF (normal)
ADC select: OFF (normal)
Reverse display ON / OFF: OFF (normal)
Power control register (VC, VR, VF) = (0, 0, 0)
Serial interface internal register data clear
LCD bias ratio: 1/9 (1/65 duty), 1/8 (1/55 duty), 1/8 (1/49 duty), 1/6 (1/33 duty)
On-chip oscillator OFF
Power save release
Read-modify-write: OFF
SHL select: OFF (normal)
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)
Reference voltage set: OFF
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
Test mode release

When RESET instruction is issued, following procedure is occurred.

Read-modify-write: OFF
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
SHL select: 0
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)
Reference voltage set: OFF
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
Test mode release

While RESETB is "L" or Reset instruction is executed, no instruction except read status could be accepted. Reset status appears at DB4. After DB4 becomes "L", any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 18. Instruction Table

×: Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	Turn on/off LCD panel When DON = 0: display OFF When DON = 1: display ON
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM0
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
Read status	0	1	BUSY	ADC	ONOFF	RESETB	0	0	0	0	Read the internal status
Write display data	1	0	Write data								Write data into DDRAM
Read display data	1	1	Read data								Read data from DDRAM
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC = 0: normal direction (SEG0→SEG131) When ADC = 1: reverse direction (SEG131→SEG0)
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Select normal / reverse display When REV = 0: normal display When REV = 1: reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Select normal/entire display ON When EON = 0: normal display. When EON = 1: entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL = 0: normal direction (COM0→COM63) When SHL = 1: reverse direction (COM63→COM0)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power save	-	-	-	-	-	-	-	-	-	-	Compound Instruction of display OFF and entire display ON

Table 18. Instruction Table (Continued)

×: Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
NOP	0	0	1	1	1	0	0	0	1	1	*Non-Operation command*
Test Instruction_1	0	0	1	1	1	1	×	×	×	×	*Don' t use this instruction*
Test Instruction_2	0	0	1	0	0	1	×	×	×	×	*Don' t use this instruction*

Display ON / OFF

Turns the Display ON or OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON
DON = 0: display OFF

Initial Display Line

Sets the line address of display RAM to determine the Initial Display Line. The RAM display data is displayed at the top row (COM0 when SHL = L, COM63 when SHL = H) of LCD panel.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the Column Address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	Y7	Y6	Y5	Y4

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

Read Status

Indicates the internal status of the S6B0724

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON / OFF	RESETB	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver 0: reverse direction (SEG131 → SEG0), 1: normal direction (SEG0 → SEG131)
ON / OFF	Indicates display ON / OFF status 0: display ON, 1: display OFF
RESETB	Indicates the initialization is in progress by RESETB signal 0: chip is active, 1: chip is being reset

Write Display Data

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

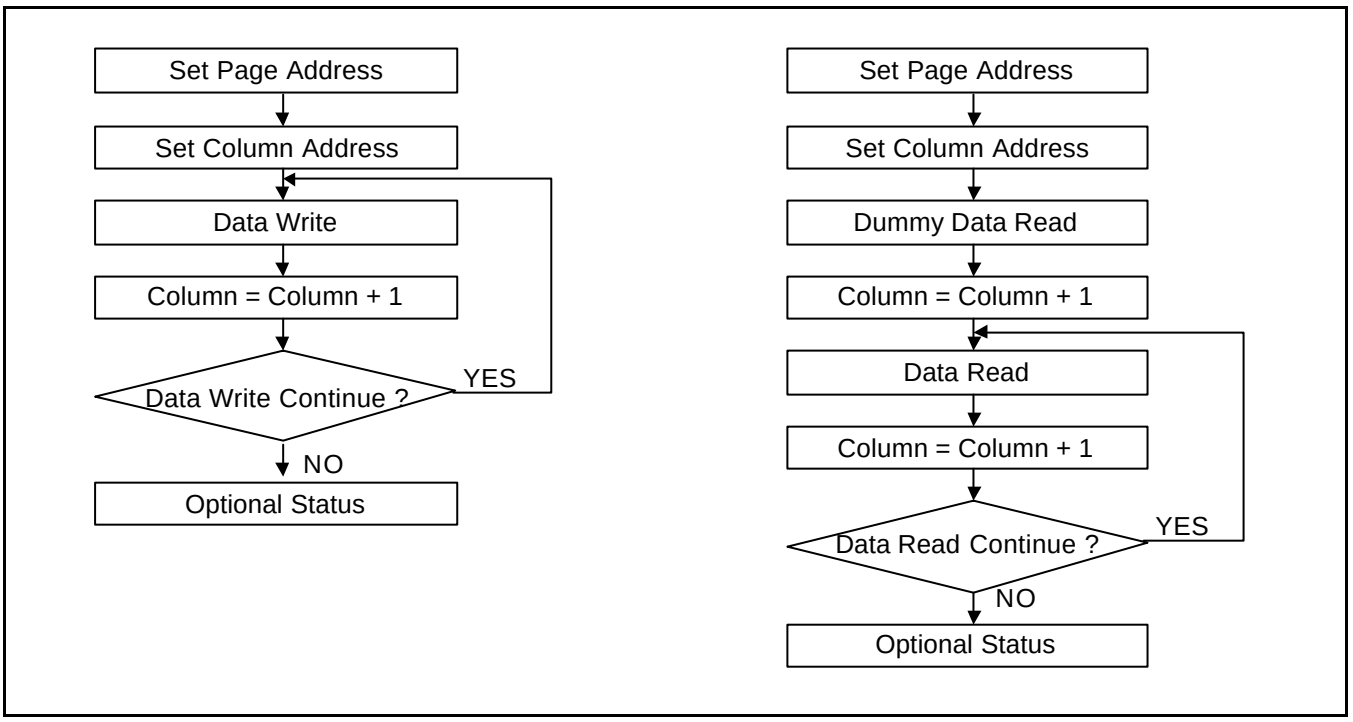


Figure 23. Sequence for Writing Display Data **Figure 24. Sequence for Reading Display Data**

Data Read Display Data

8-bit data from display data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	**1**	**Read data**							

ADC Select (Segment Driver Direction Select)

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins can be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG131)
ADC = 1: reverse direction (SEG131 → SEG0)

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = "1"	RAM bit data = "0"
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the reverse display ON / OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON = 0: normal display
EON = 1: entire display ON

Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	Bias

Duty ratio	DUTY1	DUTY0	LCD bias	
			Bias = 0	Bias = 1
1/33	0	0	1/6	1/5
1/49	0	1	1/8	1/6
1/55	1	0	1/8	1/6
1/65	1	1	1/9	1/7

Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the set Modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

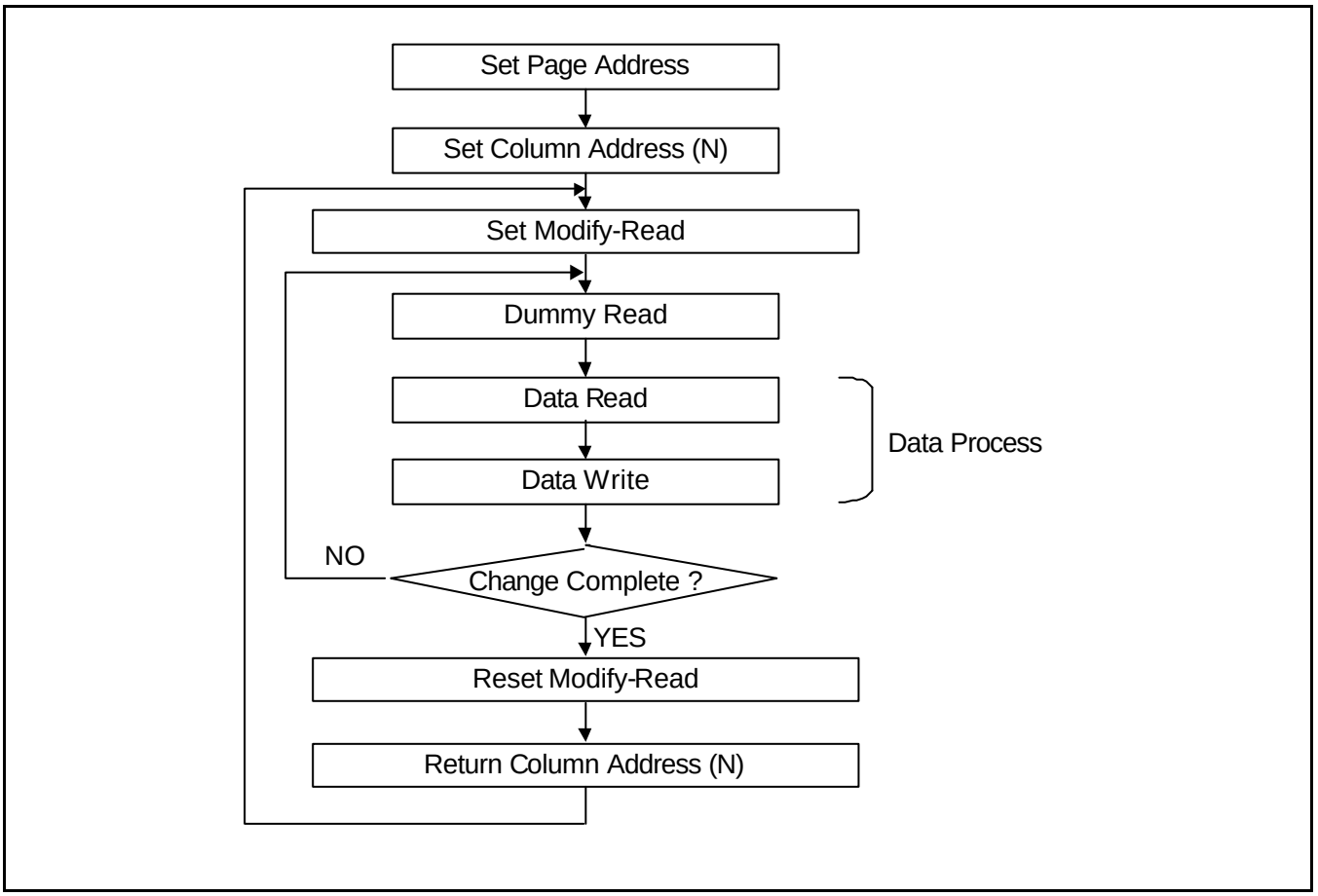


Figure 25. Sequence for Cursor Display

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

SHL Select (Common Output Mode Select)

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

×: Don' t care

SHL = 0: normal direction (COM0 → COM63)
SHL = 1: reverse direction (COM63 → COM0)

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
	0 1		Internal voltage regulator circuit is OFF Internal voltage regulator circuit is ON
		0 1	Internal voltage follower circuit is OFF Internal voltage follower circuit is ON

Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 15.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	(1 + Rb / Ra) ratio
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0 (default)
1	0	1	5.5
1	1	0	6.0
1	1	1	6.4

Reference Voltage Select

Consists of 2-byte instruction. The 1st instruction sets reference voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, reference voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (a)	V0	Contrast
0	0	0	0	0	0	0	Minimum	Low
0	0	0	0	0	1	1		
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	32 (default)	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	62		
1	1	1	1	1	1	63	Maximum	High

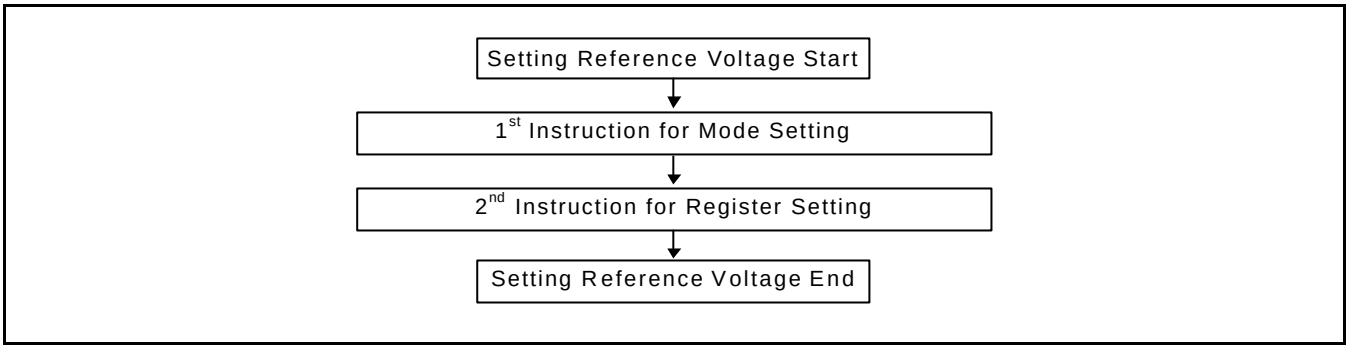


Figure 26. Sequence for Setting the Reference Voltage

Set Static Indicator State

Consists of two bytes instruction. The first byte instruction (set Static Indicator mode) enables the second byte instruction (set Static Indicator register) to be valid. The first byte sets the Static Indicator ON / OFF. When it is ON, the second byte updates the contents of Static Indicator register without issuing any other instruction and this Static Indicator state is released after setting the data of indicator register.

The 1st Instruction: Set Static Indicator Mode (ON / OFF)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	SM

SM = 0: static indicator OFF
SM = 1: static indicator ON

The 2nd Instruction: Set Static Indicator Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	×	×	×	S1	S0

S1	S0	Status of static indicator output
0	0	OFF
0	1	ON (about 1 second blinking)
1	0	ON (about 0.5 second blinking)
1	1	ON (always ON)

NOP

Non Operation Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Test Instruction (Test Instruction_1 & Test Instruction_2)

These are the instruction for IC chip testing. Please do not use it. If the Test Instruction is used by accident, it can be cleared by applying " 0" signal to the RESETB input pin or the reset instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	×	×	×	×
0	0	1	0	0	1	×	×	×	×

Power Save (Compound Instruction)

If the entire display ON / OFF instruction is issued during the display OFF state, S6B0724 enters the Power Save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, Power Save is entered to one mode of sleep and standby mode. When Static Indicator mode is ON, standby mode is issued. When OFF, sleep mode is issued. Power Save mode is released by the entire display OFF instruction.

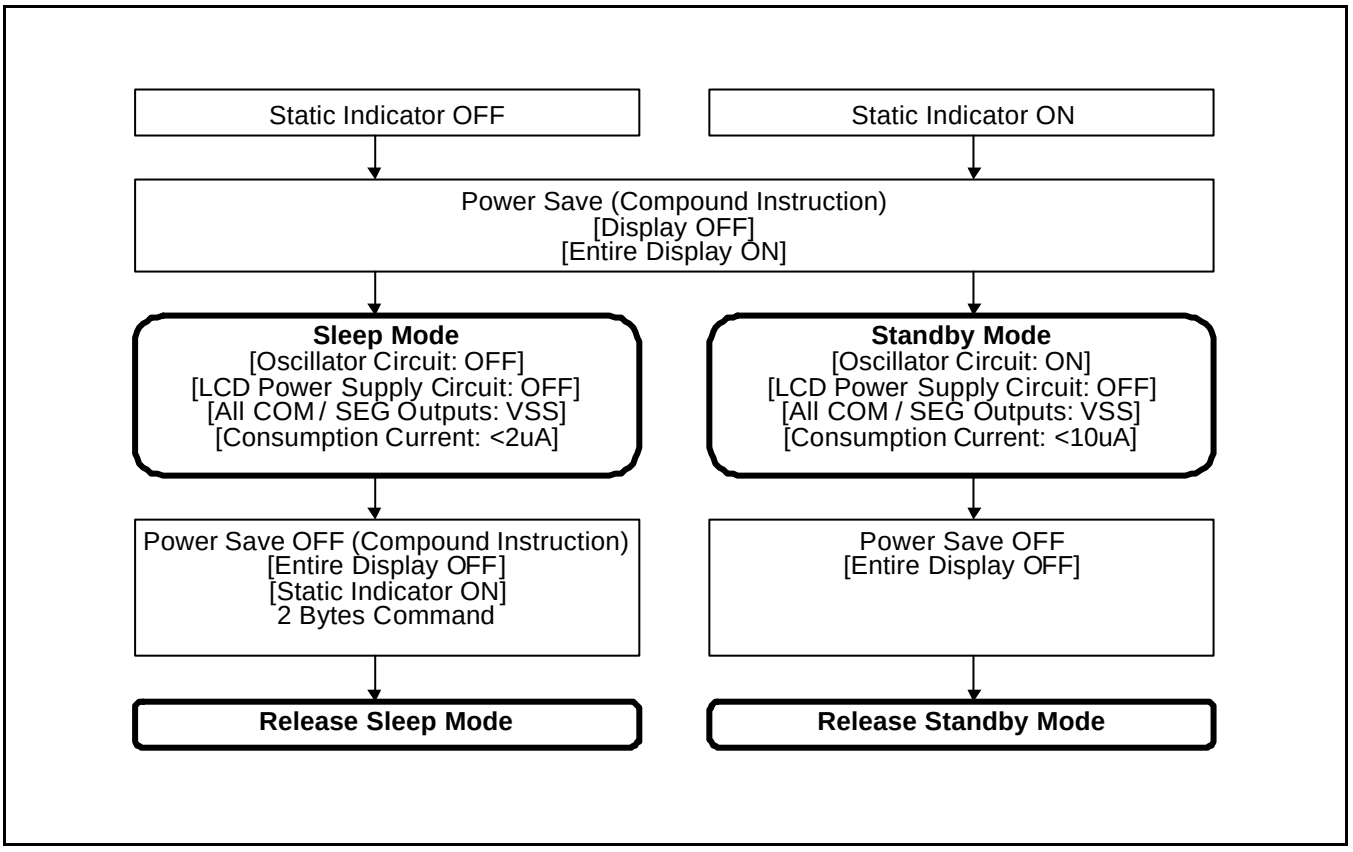


Figure 27. Power Save (Compound Instruction)

– Sleep Mode

This stops all operations in the LCD display system, and as long as there are no access from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

a. The oscillator circuit and the LCD power supply circuit are halted.
b. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a V_{SS} level.

– Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive.
The internal modes are in the following states during standby mode.

a. The LCD power supply circuits are halted. The oscillator circuit continues to operate.
b. The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs a V_{SS} level. The static drive system does not operate.
When a reset command is performed while in standby mode, the system enters sleep mode.

Referential Instruction Setup Flow (1)

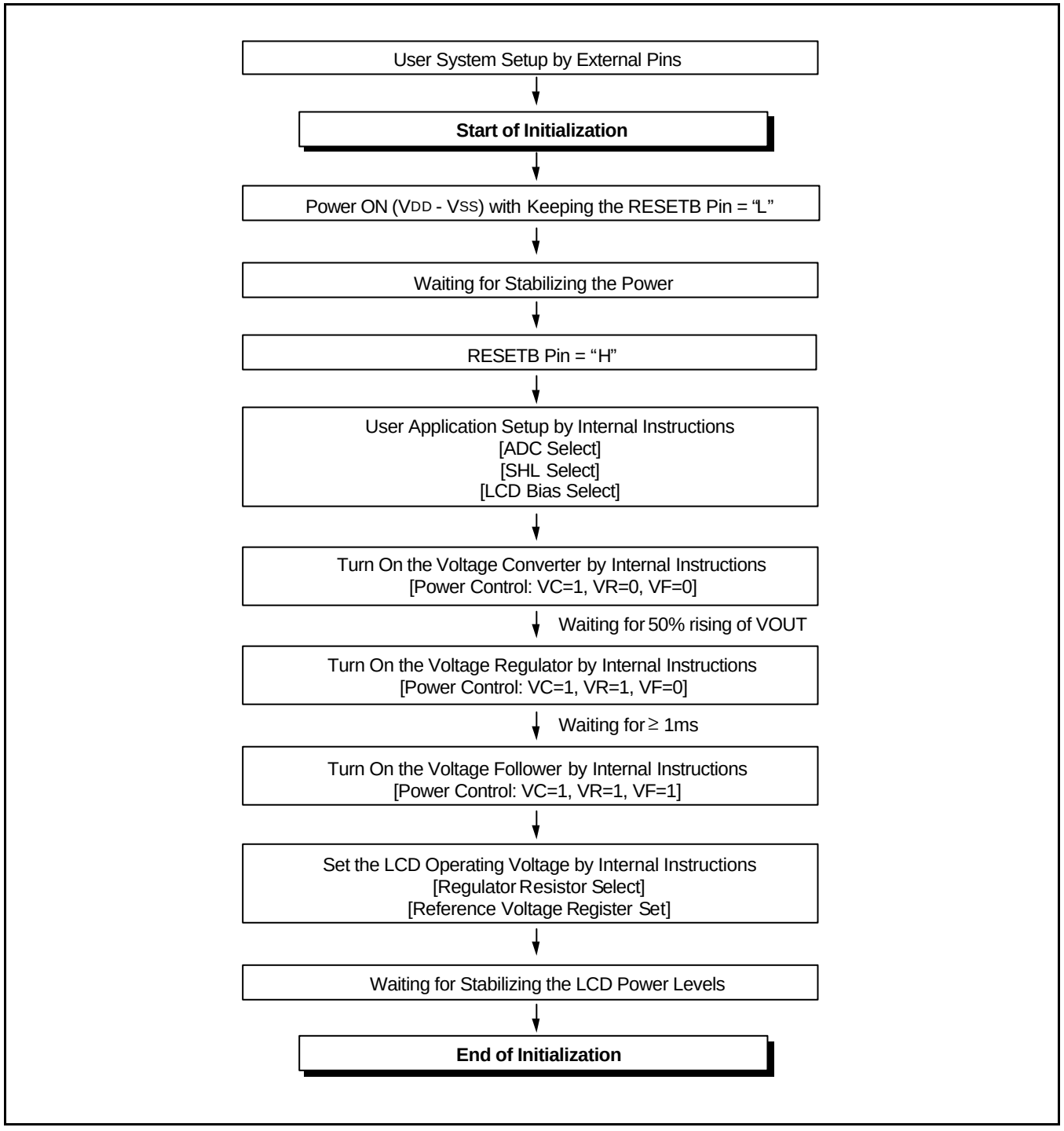


Figure 28. Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow (2)

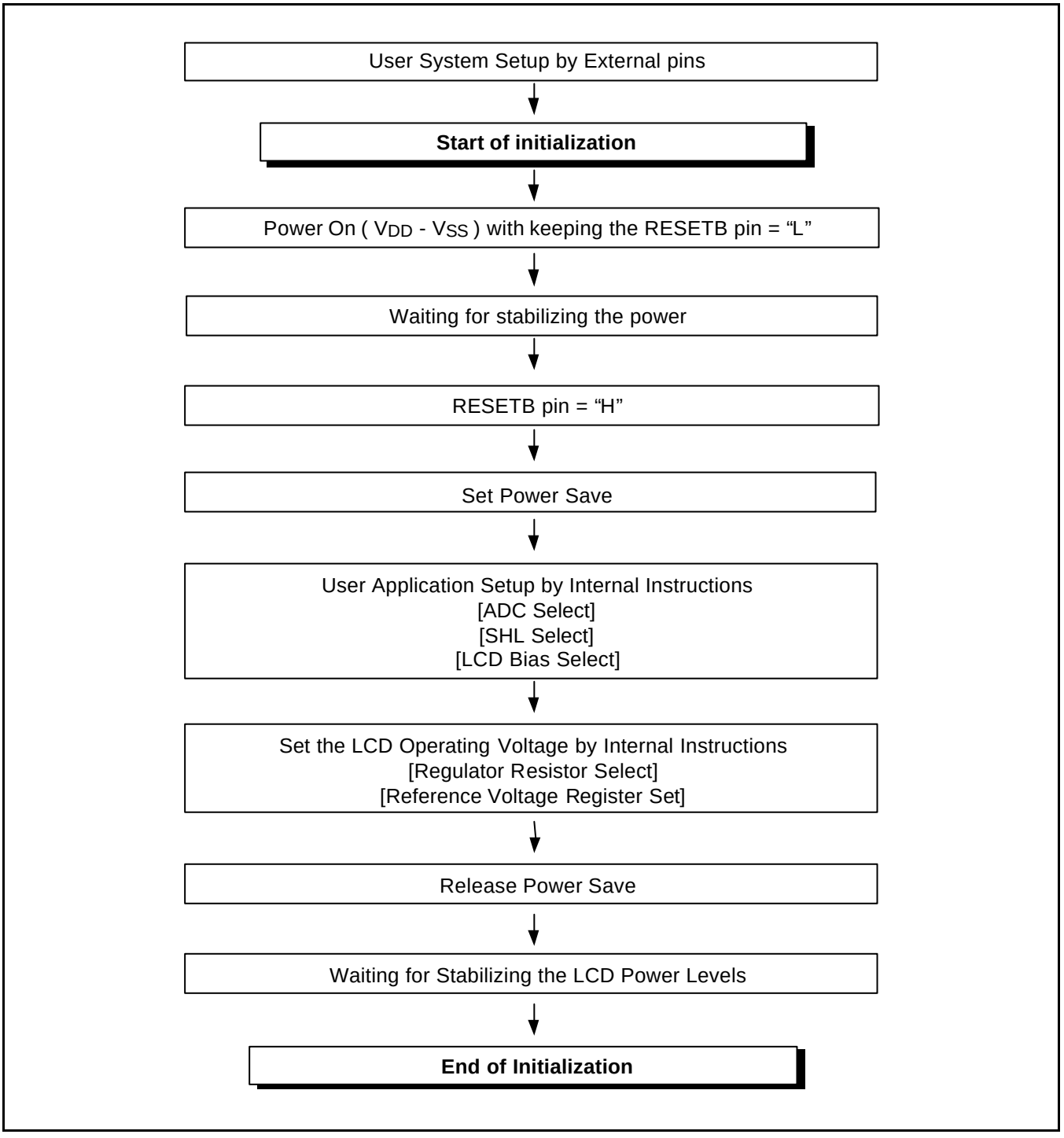


Figure 29. Initializing without the Built-in Power Supply Circuits

Referential Instruction Setup Flow (3)

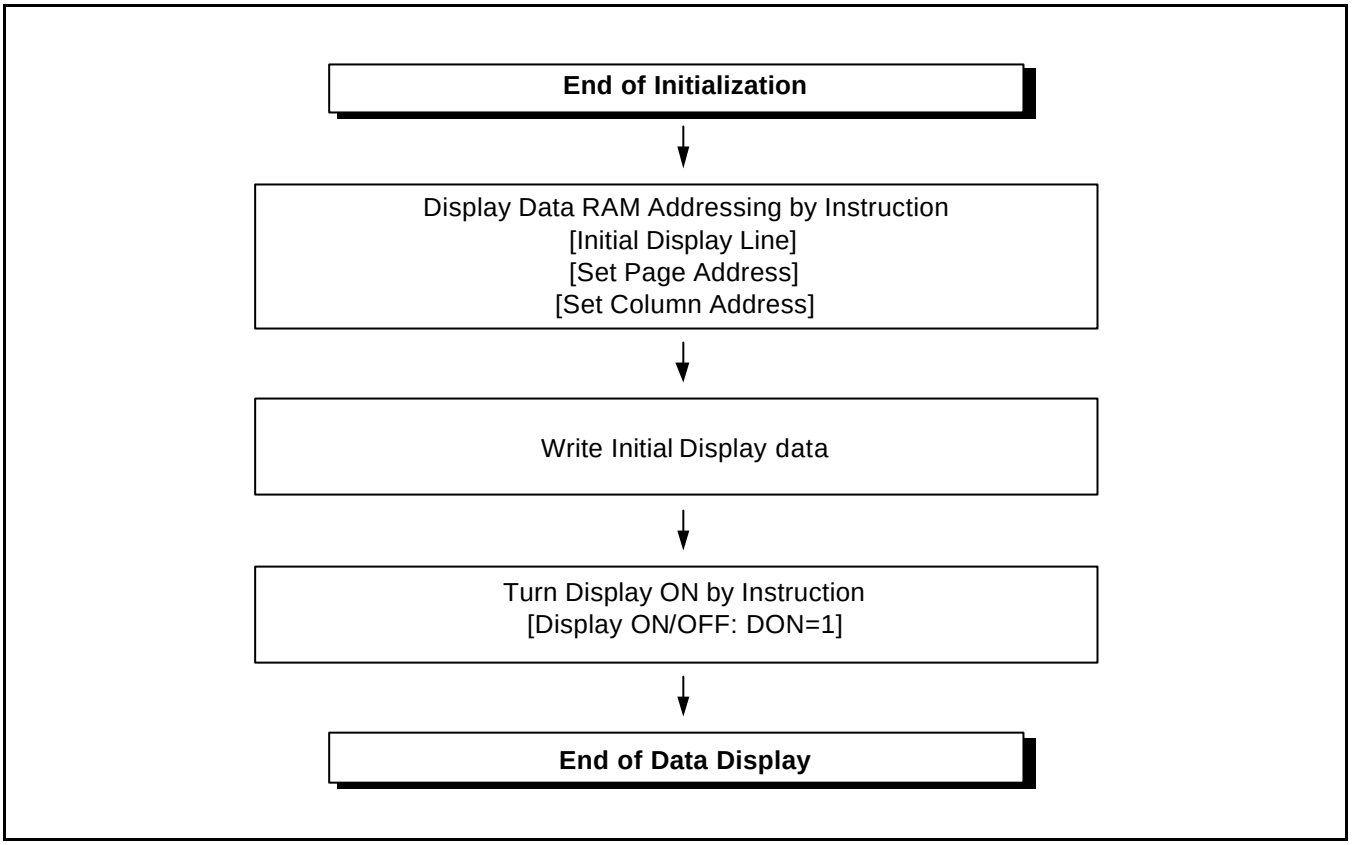


Figure 30. Data Displaying

Referential Instruction Setup Flow (4)

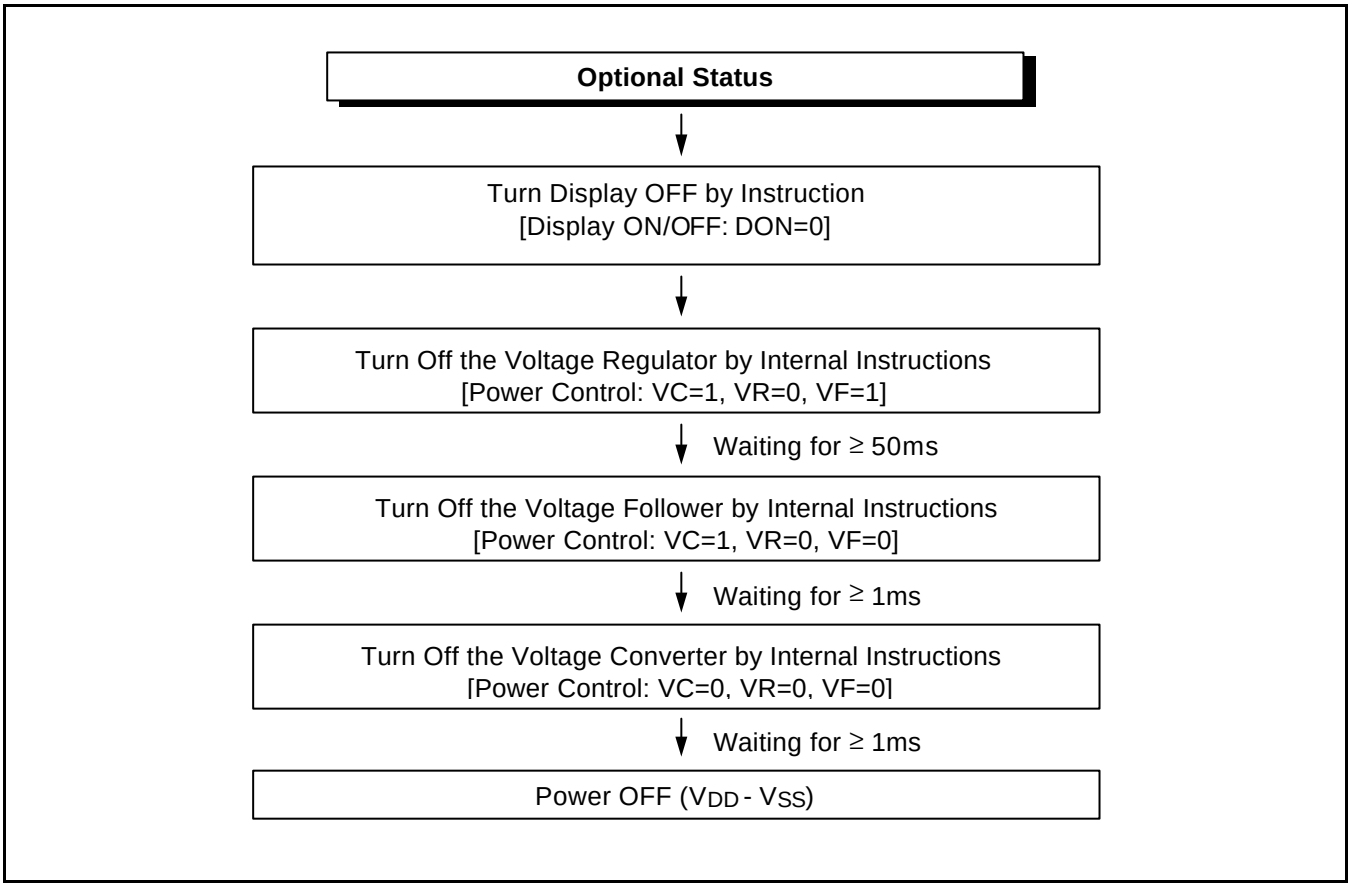


Figure 31. Power OFF

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 19. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	- 0.3 to +7.0	V
	V_{LCD}	- 0.3 to +17.0	V
Input voltage range	V_{IN}	- 0.3 to V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	- 40 to +85	°C
Storage temperature range	T_{STR}	- 55 to +125	°C

NOTES:

1. VDD and VLCD are based on VSS = 0V.
2. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS must always be satisfied.(VLCD = V0 – VSS)
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 20. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4 to 5.5V, Ta = -40 to 85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating voltage (1)		V_{DD}	Select by product code	2.4	-	3.6	V	VDD *1
				2.4	-	5.5		
Operating voltage (2)		V0		4.5	-	15.0	V	V0 *2
Input voltage	High	V_{IH}		0.8V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}		V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{DD} = 3.0V V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	µA	*5
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	µA	*6
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn *7
Oscillator frequency	Internal	f_{OSC}	V_{DD} = 3.0V Ta = 25°C Duty ratio = 1/65	32.7	43.6	54.5	kHz	CL *8
	External	f_{CL}		4.09	5.45	6.81		
Voltage converter input voltage		VCI	× 2	2.4	-	5.5	V	VCI
			× 3	2.4	-	5.0		
			× 4	2.4	-	3.75		
			× 5	2.4	-	3.0		
Voltage converter output voltage		VOUT	×2 / ×3 / ×4 / ×5 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator operating voltage		VOUT		6.0	-	16.0	V	VOUT
Voltage follower operating voltage		V0		4.5	-	15.0	V	V0 *9
Reference voltage		V_{REF}	V_{DD} = 3.0V Ta = 25°C	- 0.05%/°C	2.04	2.1	2.16	V	*10

Dynamic Current Consumption (1) when the Built-in Power Circuit is OFF (At Operate Mode)

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (1)	I_{DD1}	V_{DD} = 3.0V V0 – V_{SS} = 11.0V 1/65 duty ratio Display pattern OFF	-	15	23	µA	*11

Dynamic Current Consumption (2) when the Built-in Power Circuit is ON (At Operate Mode)

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	I_{DD2}	V_{DD} = 3.0V, (VCI = V_{DD}, 4 times boosting) V0 – V_{SS} = 11.0V, 1/65 duty ratio, Display pattern OFF, Normal power mode	-	40	60	µA	*12
		V_{DD} = 3.0V, (VCI = V_{DD}, 4 times boosting) V0 – V_{SS} = 11.0V, 1/65 duty ratio, Display pattern checker, Normal power mode	-	150	200	µA	*12

Current Consumption during Power Save Mode

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	I_{DDS1}	V_{DD} = 3.0V During sleep	-	-	2.0	µA	
Standby mode current	I_{DDS2}	V_{DD} = 3.0V During standby	-	-	10.0	µA	

Table 21. The Relationship between Oscillation Frequency and Frame Frequency

Duty ratio	Item	f_{CL}	f_M
1/65	On-chip oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{2 \times 8 \times 65}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{2 \times 65}$
1/55	On-chip oscillator circuit is used	$\frac{f_{OSC}}{9}$	$\frac{f_{OSC}}{2 \times 9 \times 55}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{2 \times 55}$
1/49	On-chip oscillator circuit is used	$\frac{f_{OSC}}{10}$	$\frac{f_{OSC}}{2 \times 10 \times 49}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{2 \times 49}$
1/33	On-chip oscillator circuit is used	$\frac{f_{OSC}}{15}$	$\frac{f_{OSC}}{2 \times 15 \times 33}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{2 \times 33}$

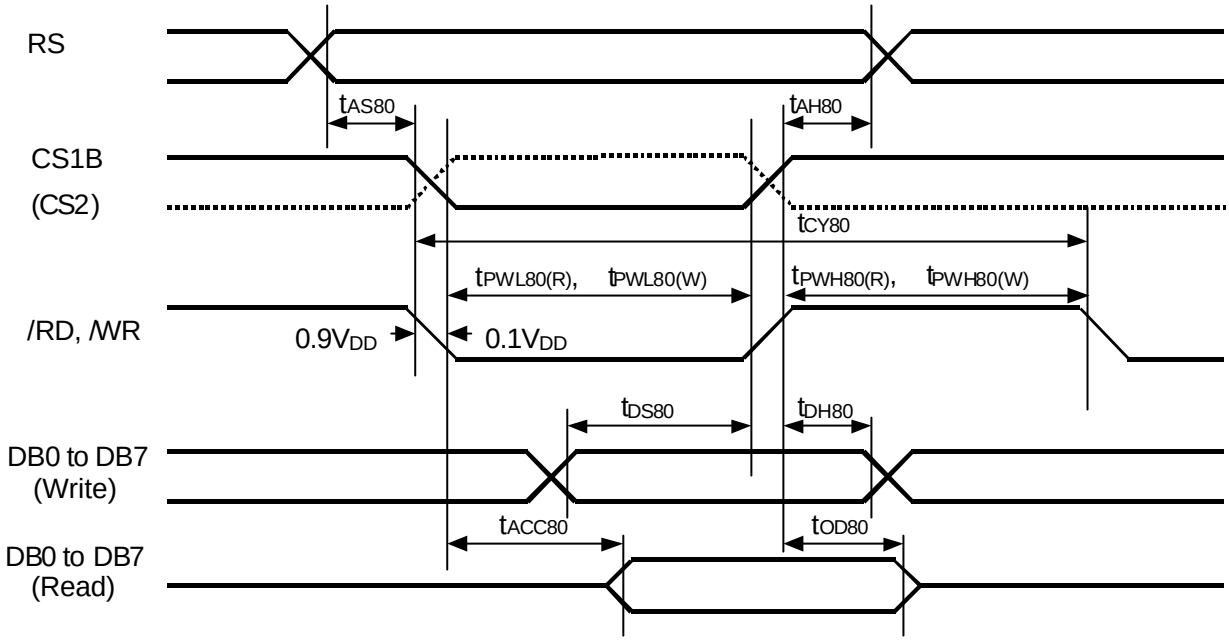
(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_{FR}: LCD AC signal frequency)

[* Remark Solves]

*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
*2. In case of external power supply is applied.
*3. CS1B, CS2, RS, DB0 to DB7, E_RDB, RW_WRB, RESETB, MS, C68, PS, INTRS, HPMB, CLS, CL, M, FR, DISP pins.
*4. DB0 to DB7, M, FR, DISP, CL pins.
*5. CS1B, CS2, RS, DB[7:0], E_RDB, RW_WRB, RESETB, MS, C68, PS, INTRS, HPMB, CLS, CL, M, FR, DISP pins.
*6. Applies when the DB[7:0], M, FR, DISP, and CL pins are in high impedance.
*7. Resistance value when ± 0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
RON= ΔV / 0.1 [kΩ] (ΔV: voltage change when ± 0.1[mA] is applied in the ON status.)
*8. See table 21 for the relationship between oscillation frequency and frame frequency.
*9. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range
*10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
*11,12. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is ON or OFF.
The current flowing through voltage regulation resistors (Ra and Rb) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc.

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)



** $t_{PWL80(W)}$ and $t_{PWL80(R)}$ is specified in the overlapped period when CS1B is low (CS2 is high) and /WR(/RD) is low.

Figure 32. Read / Write Characteristics (8080-series MPU)

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS80} t_{AH80}	0 0	-	-	ns	
System cycle time		/WR, /RD	t_{CY80}	300	-	-	ns	
Enable Pulse Low width	Read	/RD	$t_{PWL80\ (R)}$	120	-	-	ns	
	Write	/WR	$t_{PWL80\ (W)}$	60	-	-	ns	
Enable Pulse High width	Read	/RD	$t_{PWH80\ (R)}$	60	-	-	ns	
	Write	/WR	$t_{PWH80\ (W)}$	60	-	-	ns	
Data setup time Data hold time		DB7 To DB0	t_{DS80} t_{DH80}	40 15	-	-	ns	
Read access time Output disable time			t_{ACC80} t_{OD80}	- 10	-	140 100	ns	C_L = 100 pF

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS80} t_{AH80}	0 0	-	-	ns	
System cycle time		/WR, /RD	t_{CY80}	166	-	-	ns	
Enable Pulse Low width	Read	/RD	$t_{PWL80\ (R)}$	70	-	-	ns	
	Write	/WR	$t_{PWL80\ (W)}$	30	-	-	ns	
Enable Pulse High width	Read	/RD	$t_{PWH80\ (R)}$	30	-	-	ns	
	Write	/WR	$t_{PWH80\ (W)}$	30	-	-	ns	
Data setup time Data hold time		DB7 To DB0	t_{DS80} t_{DH80}	30 10	-	-	ns	
Read access time Output disable time			t_{ACC80} t_{OD80}	- 5	-	70 50	ns	C_L = 100 pF

Note: The input signal rising time and falling time (tr, tf) is specified at 15ns or less.
Or (tr + tf) < (t_{CY80} – $t_{PWL80\ (W)}$ – $t_{PWH80\ (W)}$) for write, (tr + tf) < (t_{CY80} – $t_{PWL80\ (R)}$ – $t_{PWH80\ (R)}$) for read.

Read / Write Characteristics (6800-series Microprocessor)

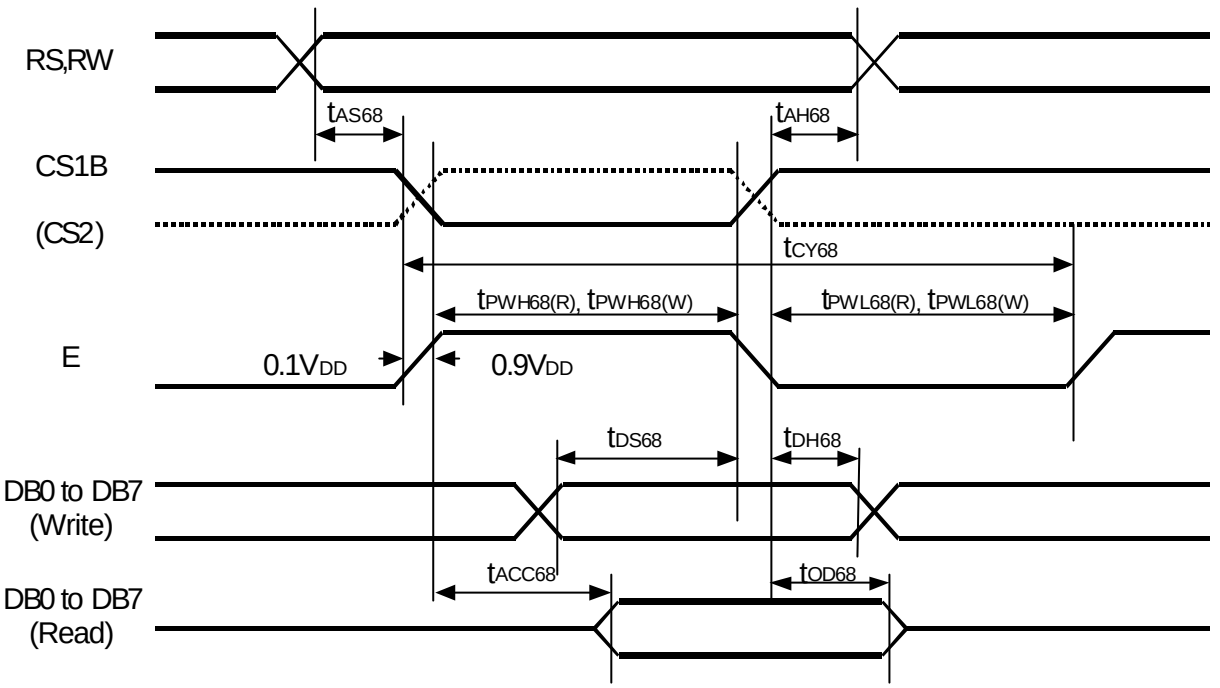


Figure 33. Read / Write Characteristics (6800-series Microprocessor)

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS,RW	t_{AS68} t_{AH68}	0 0	-	-	ns	
System cycle time		E	t_{CY68}	300	-	-	ns	
Enable Pulse High Width	Read	E	t_{PWH68} (R)	120			ns	
	Write		t_{PWH68} (W)	60				
Enable Pulse Low Width	Read	E	t_{PWL68} (R)	60			ns	
	Write		t_{PWL68} (W)	60				
Data setup time Data hold time		DB7 To DB0	t_{DS68} t_{DH68}	40 15	-	-	ns	
Access time Output disable time			t_{ACC68} t_{OD68}	- 10	-	140 100	ns	C_L = 100 pF

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS,RW	t_{AS68} t_{AH68}	0 0	-	-	ns	
System cycle time		E	t_{CY68}	166	-	-	ns	
Enable Pulse High Width	Read	E	t_{PWH68} (R)	70			ns	
	Write		t_{PWH68} (W)	30				
Enable Pulse Low Width	Read	E	t_{PWL68} (R)	30			ns	
	Write		t_{PWL68} (W)	30				
Data setup time Data hold time		DB7 To DB0	t_{DS68} t_{DH68}	30 10	-	-	ns	
Access time Output disable time			t_{ACC68} t_{OD68}	- 10	-	70 50	ns	C_L = 100 pF

Note: 1. The input signal rising time and falling time (tr, tf) is specified at 15ns or less. Or (tr + tf) < (t_{CY68} – t_{PWL68} (W) – t_{PWH68} (W)) for write, (tr + tf) < (t_{CY68} – t_{PWL68} (R) – t_{PWH68} (R)) for read.

Serial Interface Characteristics

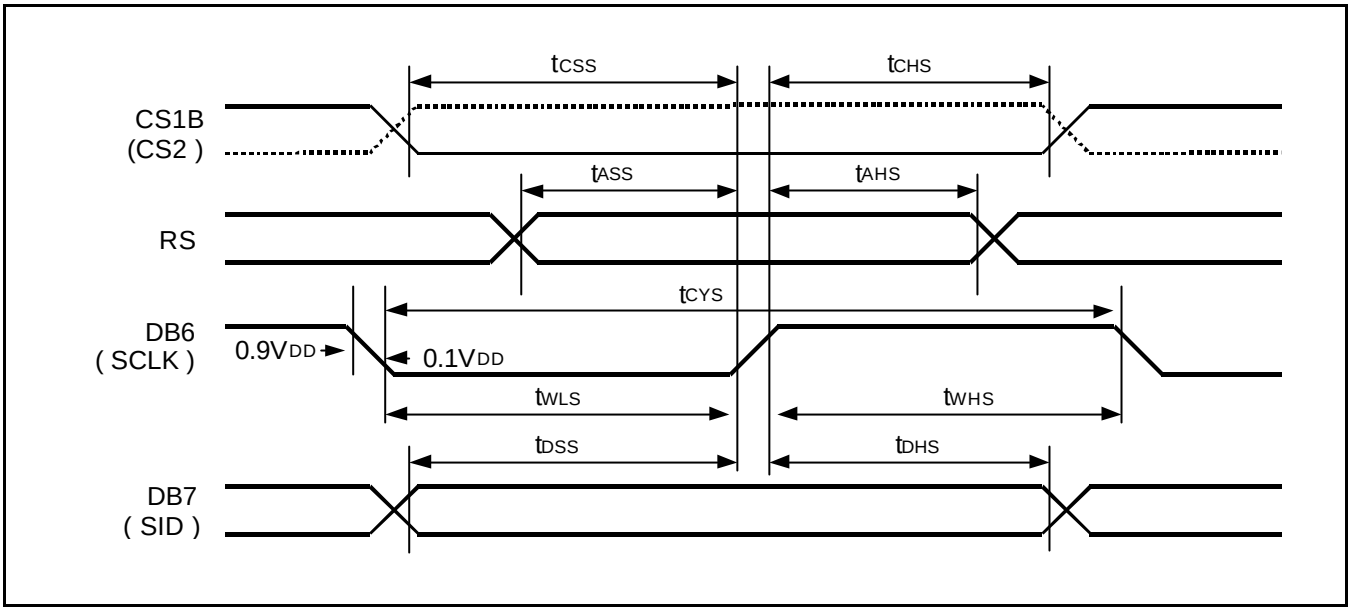


Figure 34. Serial Interface Characteristics

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	tCYS tWHS tWLS	250 100 100	- - -	- - -	ns	
Address setup time Address hold time	RS	tASS tAHS	150 150	- -	- -	ns	
Data setup time Data hold time	DB7 (SID)	tDSS tDHS	100 100	- -	- -	ns	
CS1B setup time CS1B hold time	CS1B	tCSS tCHS	150 150	- -	- -	ns	

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	tCYS tWHS tWLS	200 75 75	- - -	- - -	ns	
Address setup time Address hold time	RS	tASS tAHS	50 100	- -	- -	ns	
Data setup time Data hold time	DB7 (SID)	tDSS tDHS	50 50	- -	- -	ns	
CS1B setup time CS1B hold time	CS1B	tCSS tCHS	100 100	- -	- -	ns	

Reset Input Timing

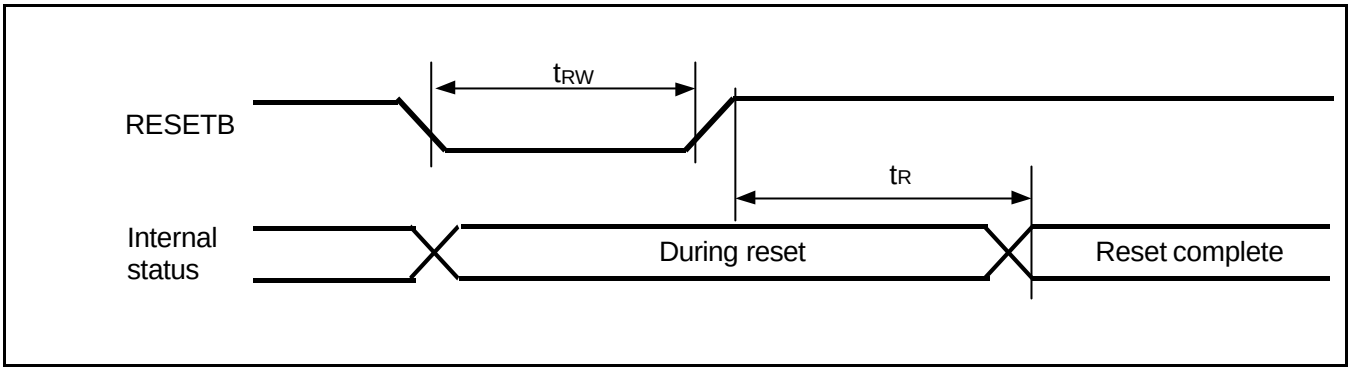


Figure 35. Reset Input Timing

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESETB	t_{RW}	1.0	-	-	µs	
Reset time	-	t_R	-	-	1.0	µs	

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESETB	t_{RW}	0.5	-	-	µs	
Reset time	-	t_R	-	-	0.5	µs	

Display Control Output Timing

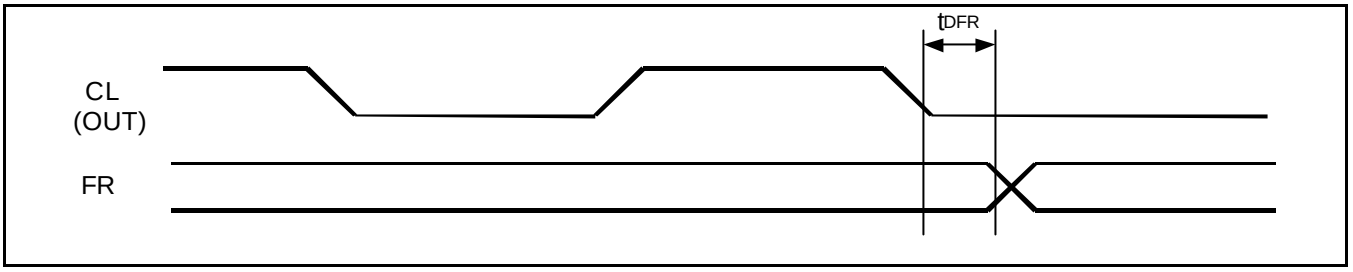


Figure 36. Display Control Output Timing

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
FR delay time	FR	t_{DFR}	-	20	80	ns	C_L = 50 pF

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
FR delay time	FR	t_{DFR}	-	10	40	ns	C_L = 50 pF

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS = "H", C68 = "H")

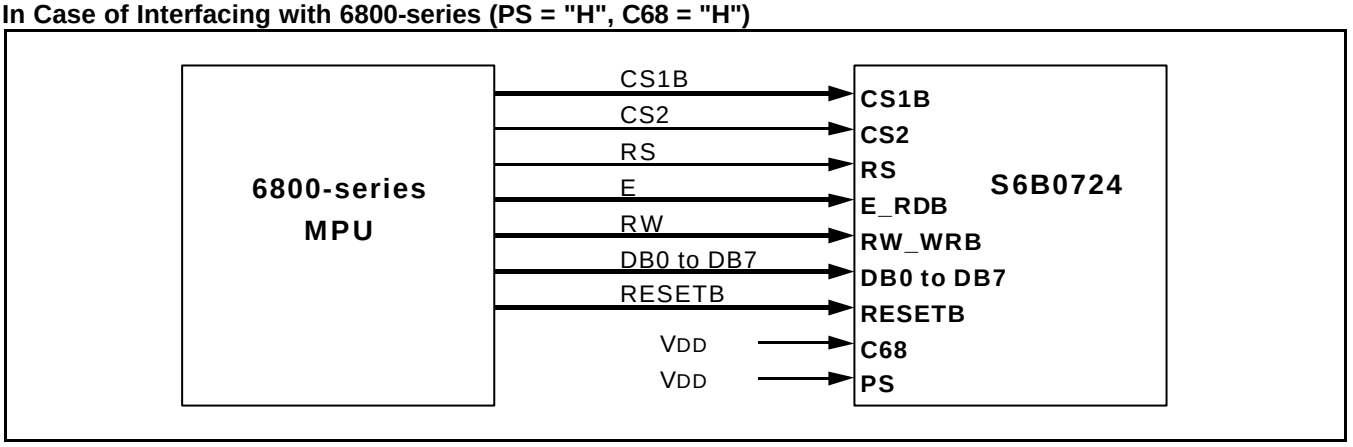


Figure 37. Interfacing with 6800-series (PS = "H", C68 = "H")

In Case of Interfacing with 8080-series (PS = "H", C68 = "L")

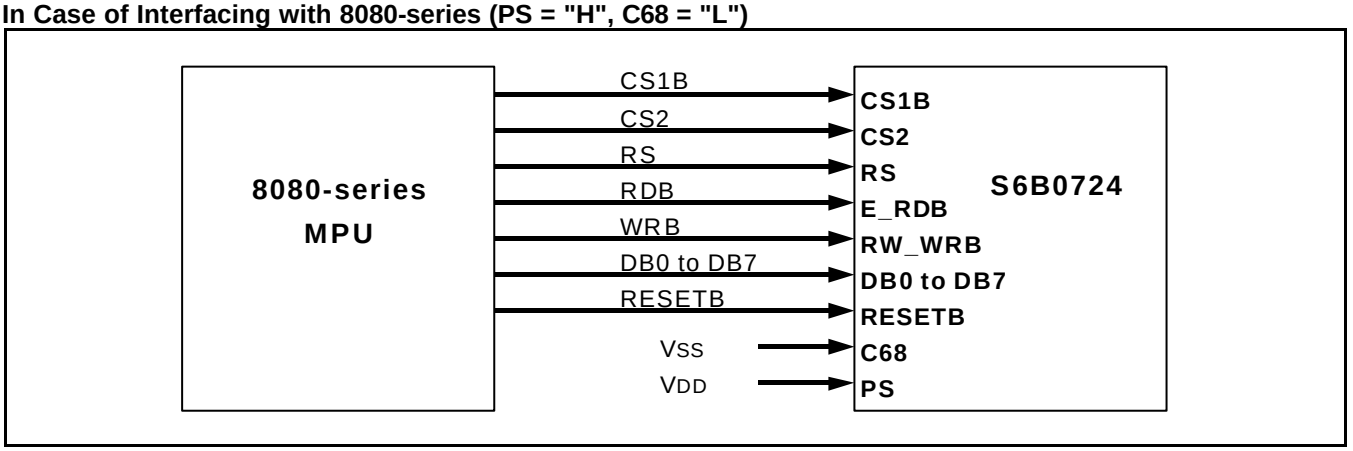


Figure 38. Interfacing with 8080-series (PS = "H", C68 = "L")

In Case of Serial Interface (PS = "L", C68 = "H or L")

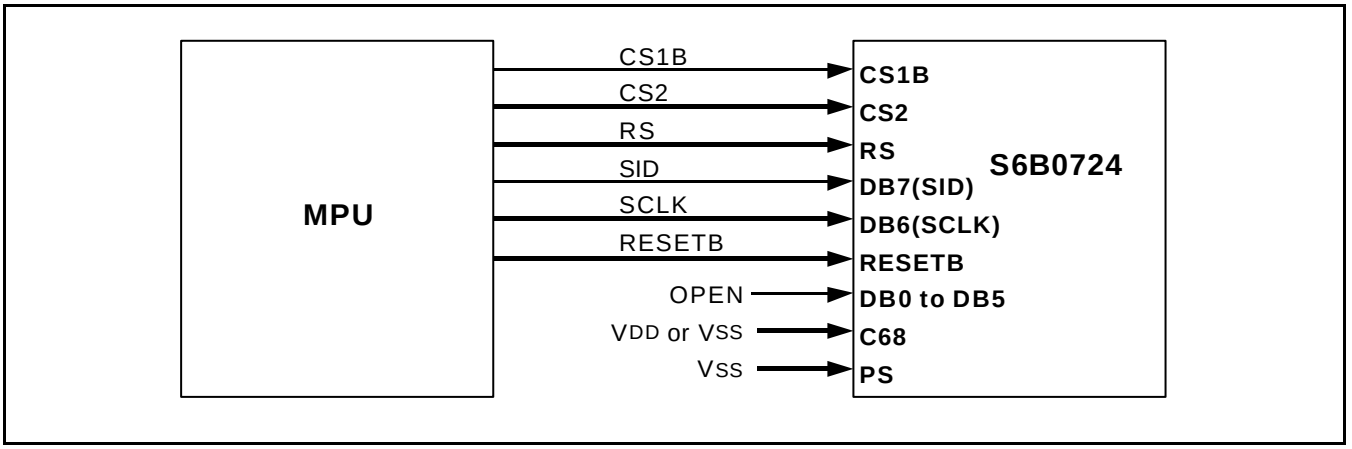


Figure 39. Serial Interface (PS = "L", C68 = "H or L")

CONNECTIONS BETWEEN S6B0724 AND LCD PANEL

Single Chip Structure (1/65 Duty Configurations)

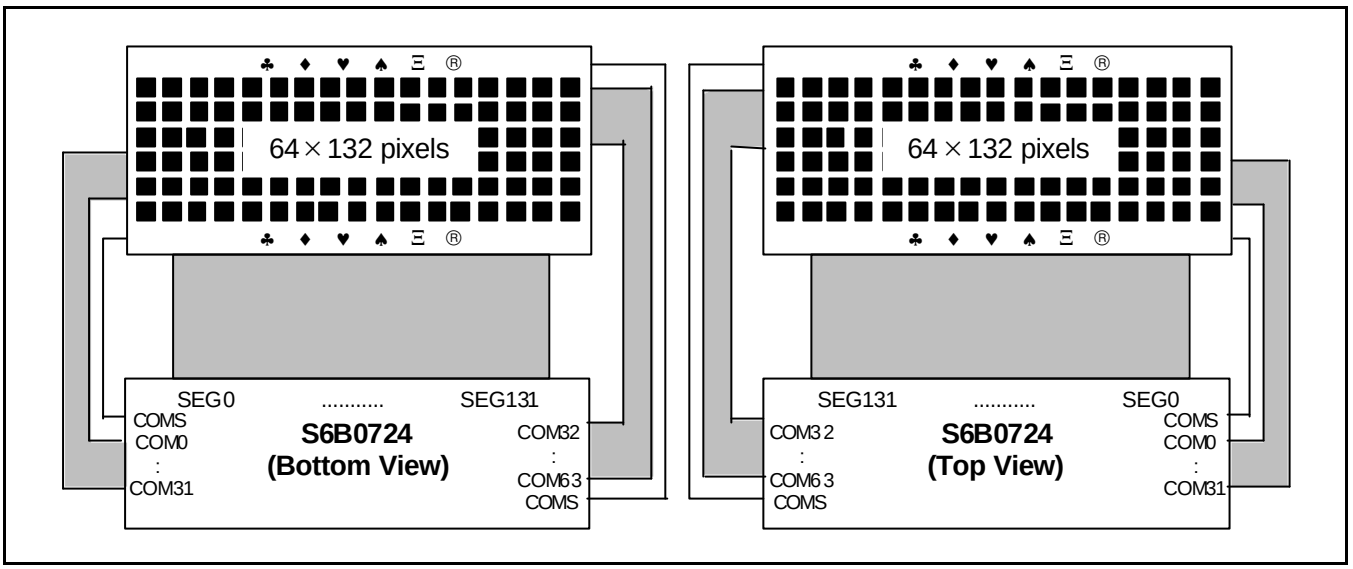


Figure 40. SHL = 1, ADC = 0

Figure 41. SHL = 1, ADC = 1

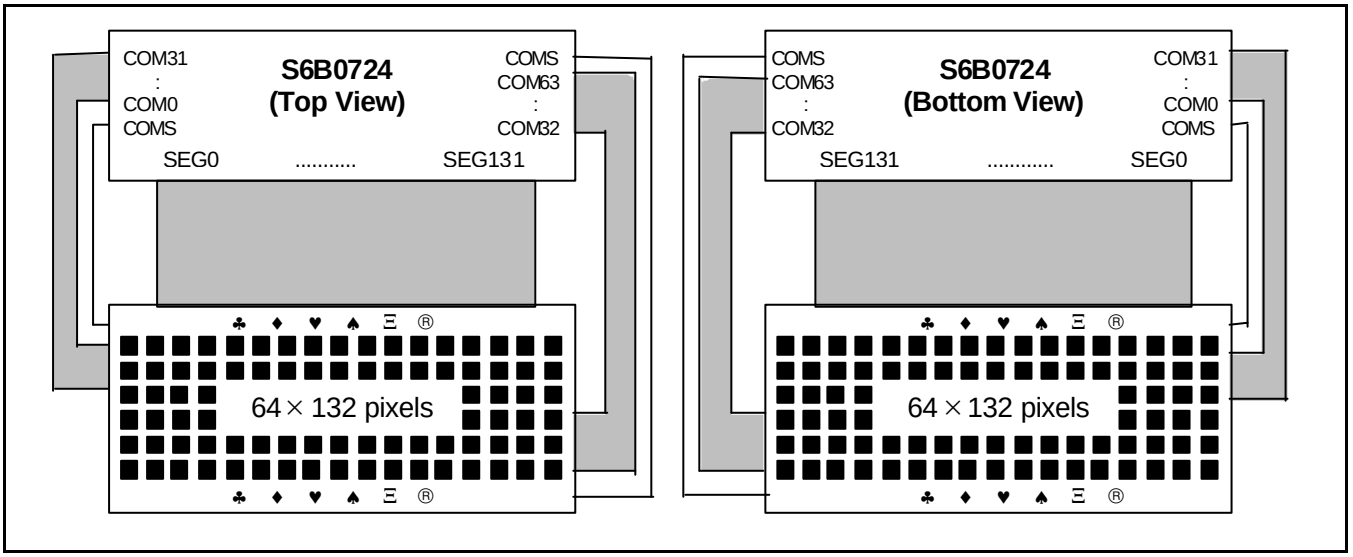


Figure 42. SHL = 0, ADC = 0

Figure 43. SHL = 0, ADC = 1

Single Chip Structure (1/55 Duty Configurations)

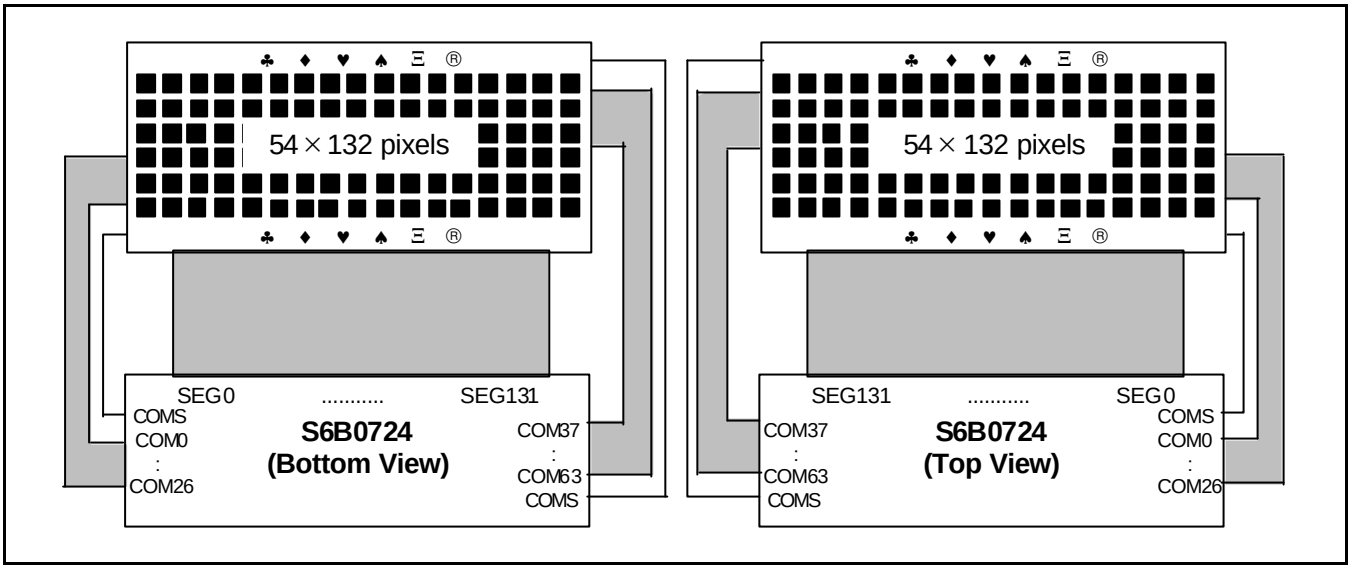


Figure 44. SHL = 1, ADC = 0

Figure 45. SHL = 1, ADC = 1

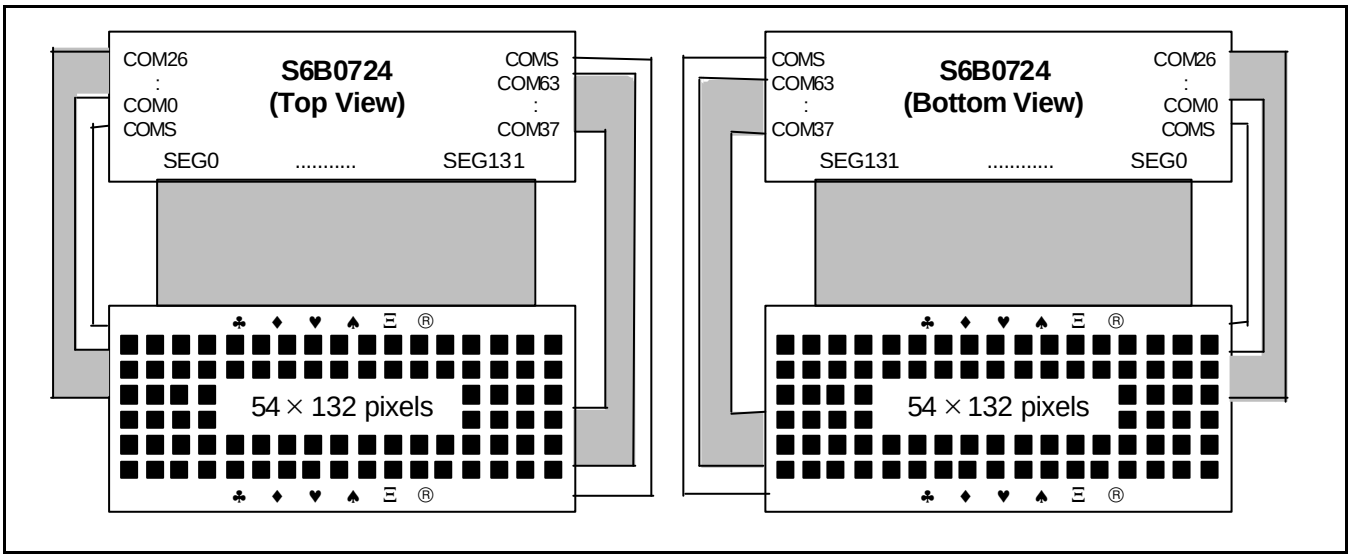


Figure 46. SHL = 0, ADC = 0

Figure 47. SHL = 0, ADC = 1

Single Chip Structure (1/49 Duty Configurations)

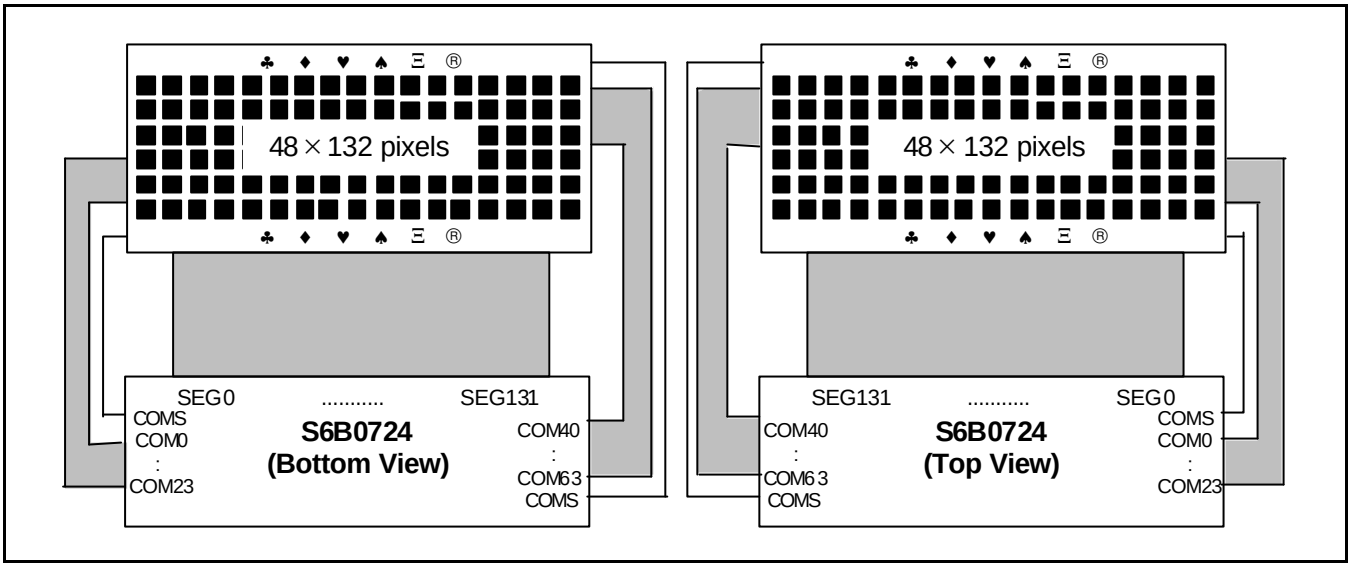


Figure 48. SHL = 1, ADC = 0

Figure 49. SHL = 1, ADC = 1

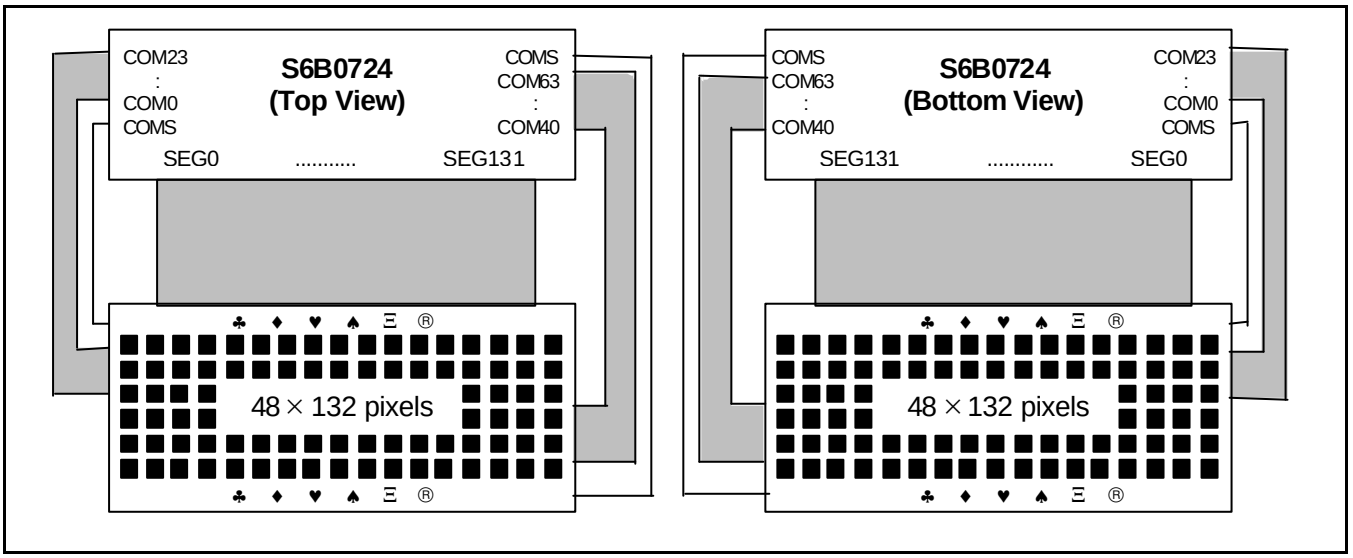


Figure 50. SHL = 0, ADC = 0

Figure 51. SHL = 0, ADC = 1

Single Chip Structure (1/33 Duty Configurations)

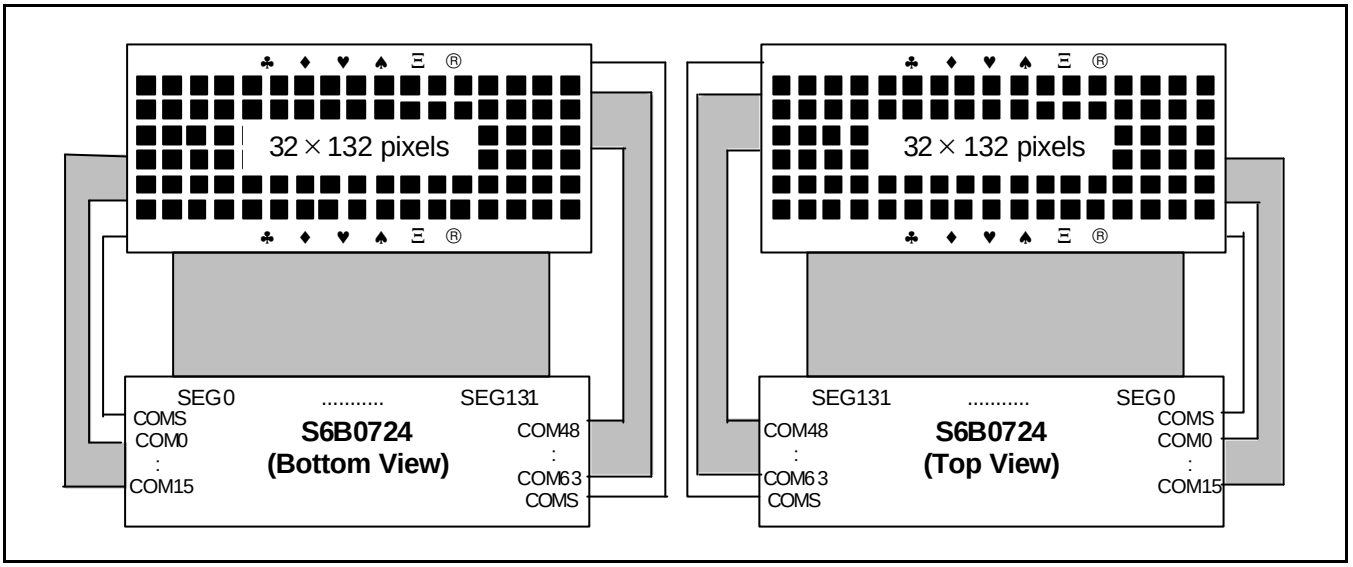


Figure 52. SHL = 1, ADC = 0

Figure 53. SHL = 1, ADC = 1

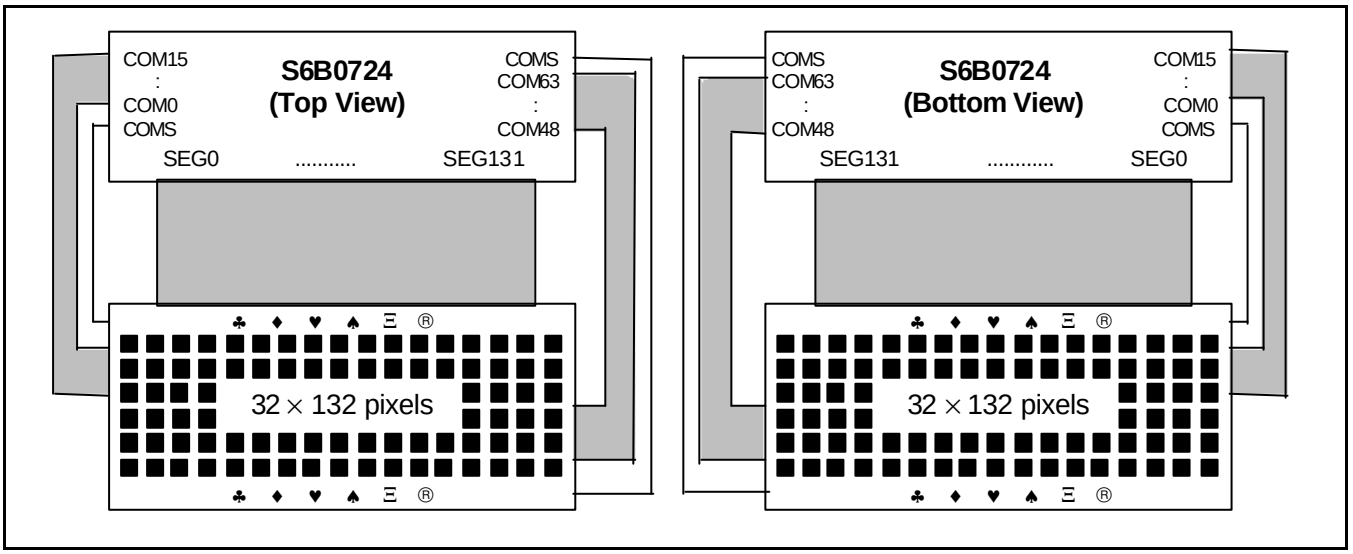


Figure 54. SHL = 0, ADC = 0

Figure 55. SHL = 0, ADC = 1

Multiple Chip Structure

- 65COM (64COM + 1COMS) ´ 264SEG (132SEG ´ 2)

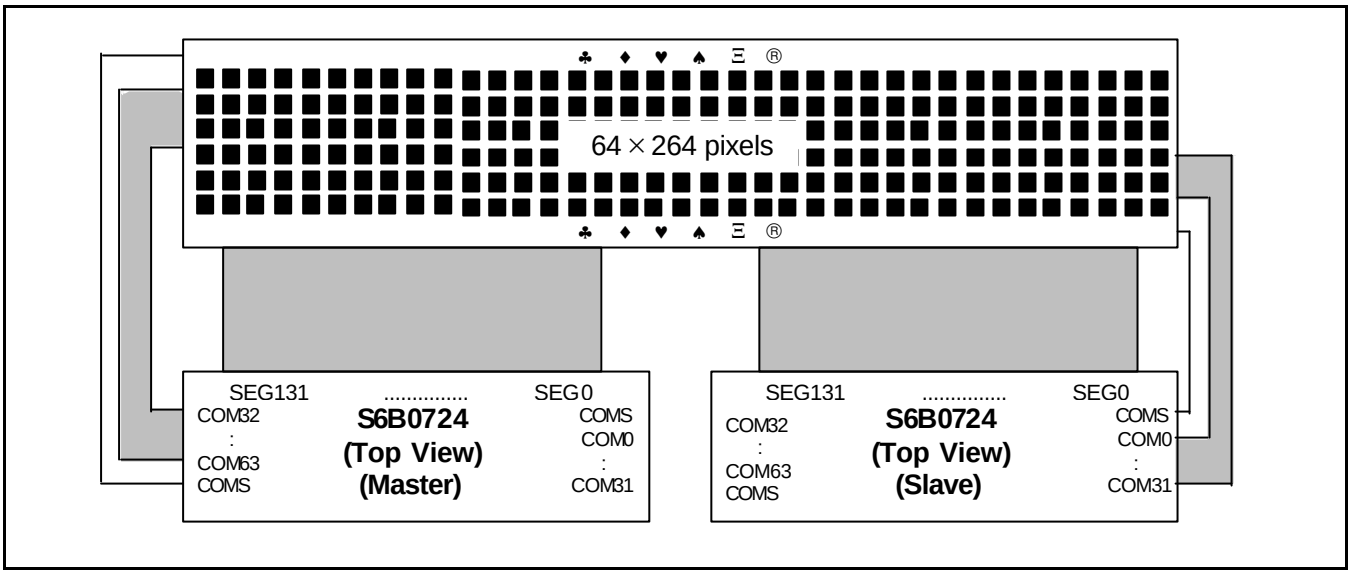


Figure 56. SHL = 1, ADC = 1

- Connect the following pins of two chips each other:
  - Display clock pins: CL, M
  - Display control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4

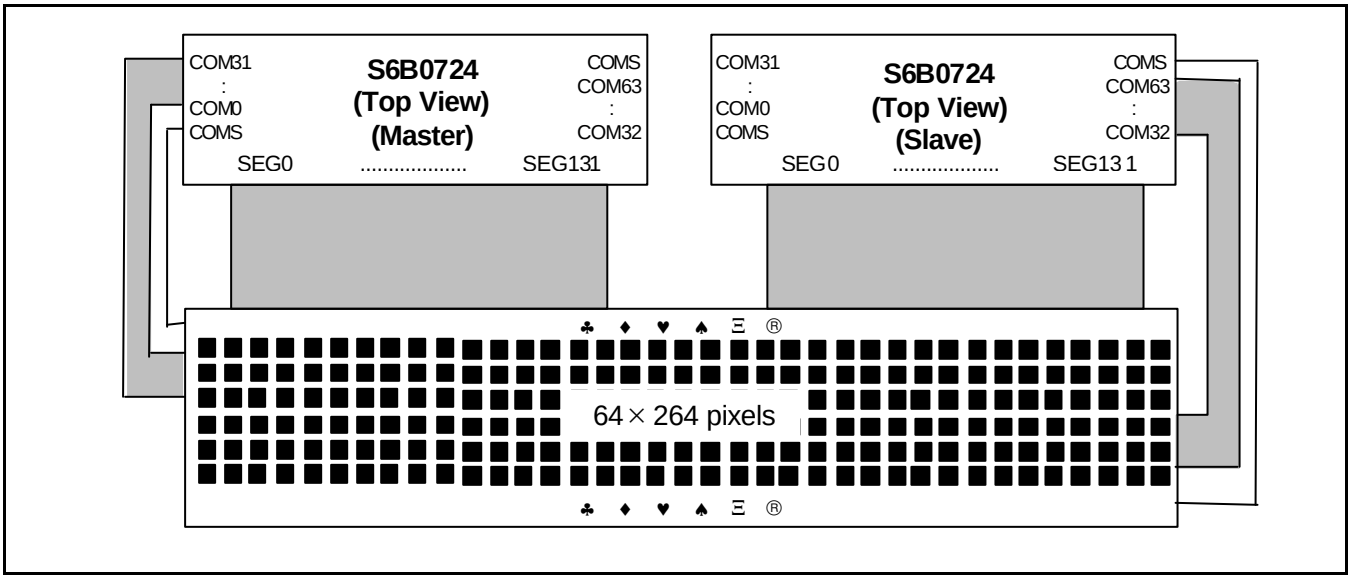


Figure 57. SHL = 0, ADC = 0

- Connect the following pins of two chips each other:
  - Display clock pins: CL, M
  - Display control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4

- 130COM (128COM + 2COMS) ´ 132SEG

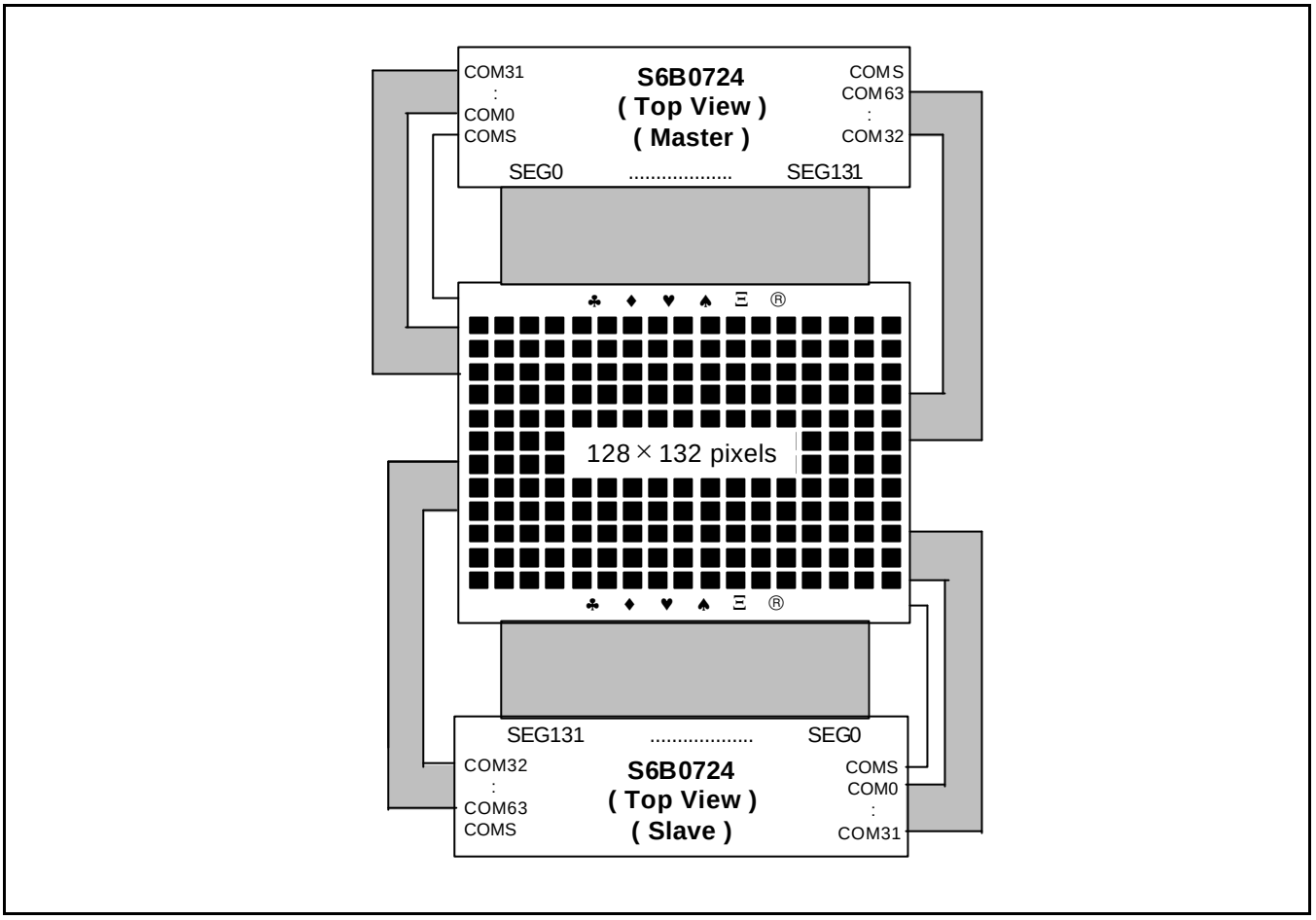


Figure 58. 130COM (128COM + 2COMS) ´ 132SEG

- Connect the following pins of two chips each other
  - Display clock pins: CL, M
  - Display control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4

- Common / Segment output direction select
  - Master chip: SHL = 0, ADC = 0
  - Slave chip: SHL = 1, ADC = 1