深圳市拓普微科技开发有限公司
SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LM240120HFW

LCD Module User Manual

Prepared by:	Checked by:	Approved by:
Wei		
Date: 2019-06-18	Date:	Date:

Rev.	Descriptions	Release Date
0.1	Preliminary release	2013-01-03
0.2	Update 1.4 Terminal Functions	2019-06-18

Table of Content

1. Basic Specifications

1.1 Display Specifications

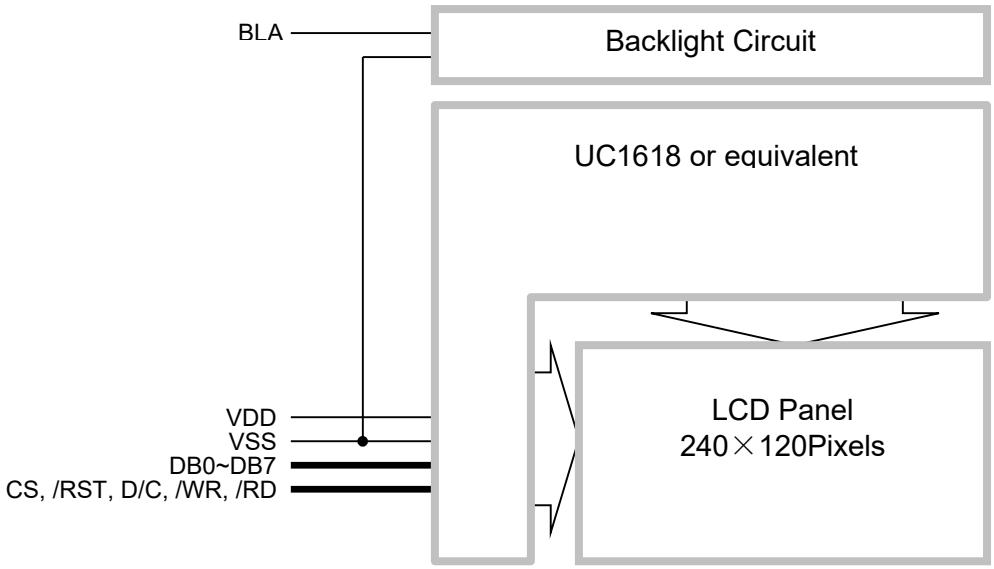
1) LCD Display Mode : STN-BLUE, Negative, Transmissive
2) Display Color : Display Data = “1” : Light Gray(*1)
: Display Data = “0” : Dark Blue (*2)
3) Viewing Angle : 12H
4) Driving Method : 1/120 duty, 1/11 bias
5) Backlight : White LED backlight

Note:
*1. Color tone may slightly change by Temperature and Driving Condition.
*2. The Color is defined as the inactive / background color
*3. Fine Contrast adjustment function is necessary in the application design for optimal display result

1.2 Mechanical Specifications

1) Outline Dimension : 79.0 x 42.3 x 8.2MAX (mm)
(See attached Outline Drawing for details)

1.3 Block Diagram



1.4 Terminal Functions

Pin No.	PIN Name	I/O	Descriptions			
			8080 mode	6800 mode	4-Wire SPI	3-Wire SPI
1	VSS	Supply	Negative power supply,0V			
2	VDD	Supply	Positive power supply			
3	DB7	I/O	8-bit Data bus; Three state I/O terminal for display data or instruction data when /CS=H,DB0~DB7=High Impedance		Connect to VSS	
4	DB6					
5	DB5					
6	DB4					
7	DB3 (SDA)				Serial data input	
8	DB2				Connect to VSS	
9	DB1					
10	DB0 (SCK)				Serial clock input	
11	/RD (E)	Input	/WR=H, /RD=L; Data or Status read form the LCD module	R/W=H,E=H; Data or Status read form the LCD module	Connect to VSS	
12	/WR (R/D)	Input	/WR=L→H, /RD=H; Data or Instruction latch into the LCD module	R/W=L,E=H→L; Data or Status latch into the LCD module	Connect to VSS	
13	D/C	Input	Register Select D/C = H, Transferring the Display Data D/C = L, Transferring the Control Data			Connect to VSS
14	/RST	Input	Reset signal /RST = L, Initialization is executed /RST = H, Normal running.			
15	CS	Input	Chip Select CS=H, enable access to the LCD module CS=L, disable access to the LCD module			
16	BLA	Supply	Positive power for LED backlight			

Note:
1. About Interface setting ,please refer to UC1618 datasheet for more detail.

Interface setting:
interface selection is available by the jumper on the back side of the lcd module.

JP1	JP2	JP3	JP4	Interface mode
OPEN	CLOSE	OPEN	CLOSE	8080 Mode(default)
OPEN	CLOSE	CLOSE	OPEN	6800 Mode
CLOSE	OPEN	OPEN	CLOSE	4 Wire SPI
CLOSE	OPEN	CLOSE	OPEN	3 Wire SPI

2. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	-0.3	+4.0	V	V_{SS} = 0V
Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	V_{SS} = 0V
Operating Temperature	T_{OP}	-30	+70	°C	No Condensation
Storage Temperature	T_{ST}	-40	+85	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

3. Electrical Characteristics

3.1 DC Characteristics

V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25°C

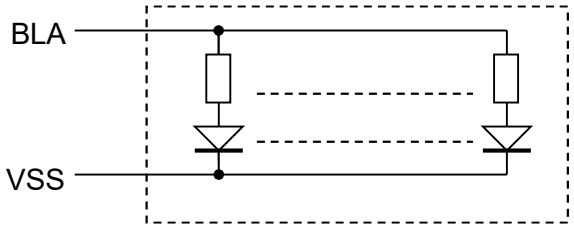
Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition / Application Pin
Operating Voltage	V_{DD}	3.3	3.3	3.6	V	VDD
Input High Voltage	V_{IH}	0.8xV_{DD}	-	V_{DD}	V	/RST, CS, D/C,
Input Low Voltage	V_{IL}	V_{SS}	-	0.2xV_{DD}	V	DB0~DB7, /RD, /WR
Operating Current	I_{DD}	-	0.8	2.5	mA	VDD

3.2 LED Backlight Circuit Characteristics

VSS=0V, If_{BLA}=68mA, T_{OP} =25°C

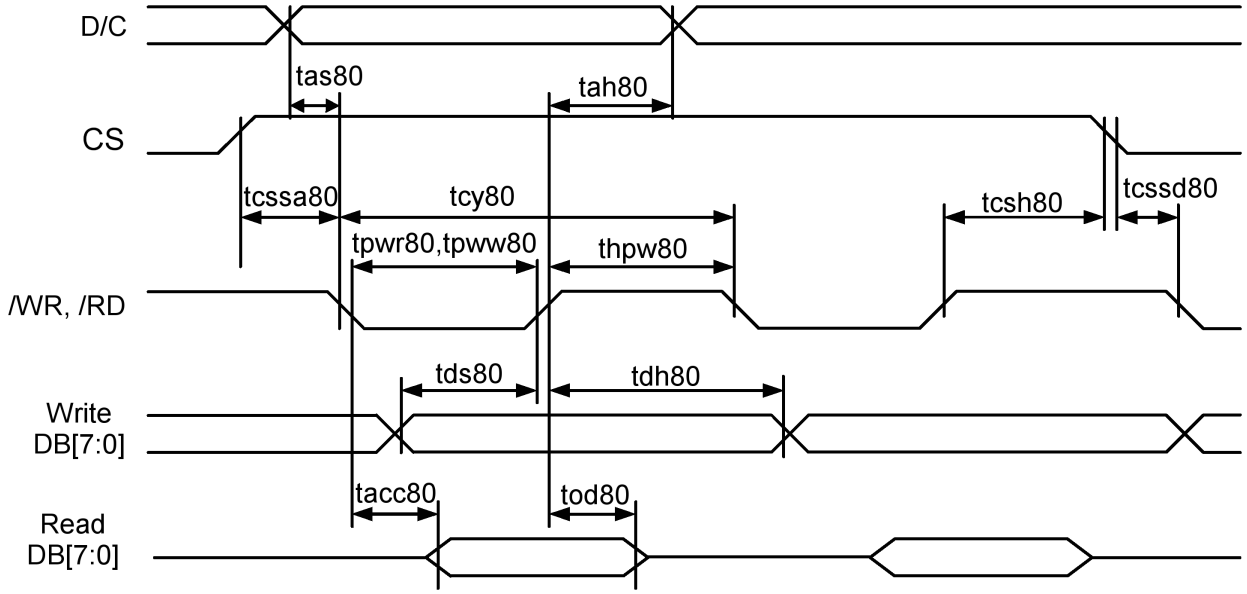
Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Forward Voltage	Vf_{BLA}	-	3.3	-	V	BLA
Forward Current	If_{BLA}	-	68	80	mA	BLA

Cautions:
Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.



3.3 AC Characteristics

3.3.1 8080 Mode System Bus Timing

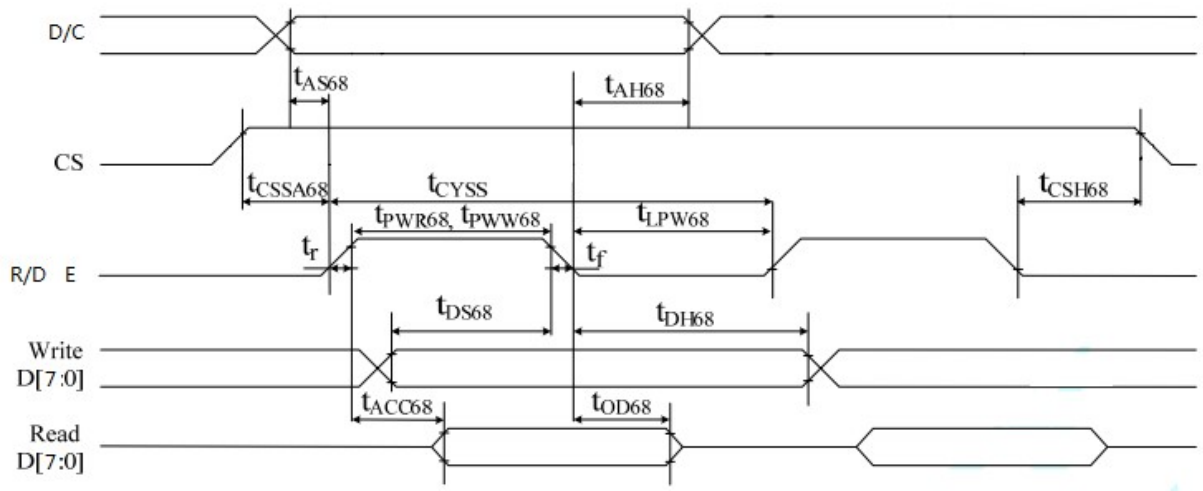


V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time (D/C)	tas80	5	-	-	ns
Address hold time (D/C)	tah80	25	-	-	ns
System cycle time	tcy80	280	-	-	ns
Read pulse width	tpwr80	87	-	-	ns
Write pulse width	tpww80	87	-	-	ns
High pulse width (read)	thpw80	100	-	-	ns
High pulse width (write)	thpw80	75	-	-	ns
Data setup time	tds80	38	-	-	ns
Data hold time	tdh80	25	-	-	ns
Data access time	tacc80	-	-	75	ns
Data output disable time	tod80	131	-	-	ns

Note:
*1. Input signal rise/fall time should be less than 15ns .
*2. CL=100pF
*3.All timing is using 20% and 80% of VDD as the reference.

3.3.2 6800 Mode System Bus Timing

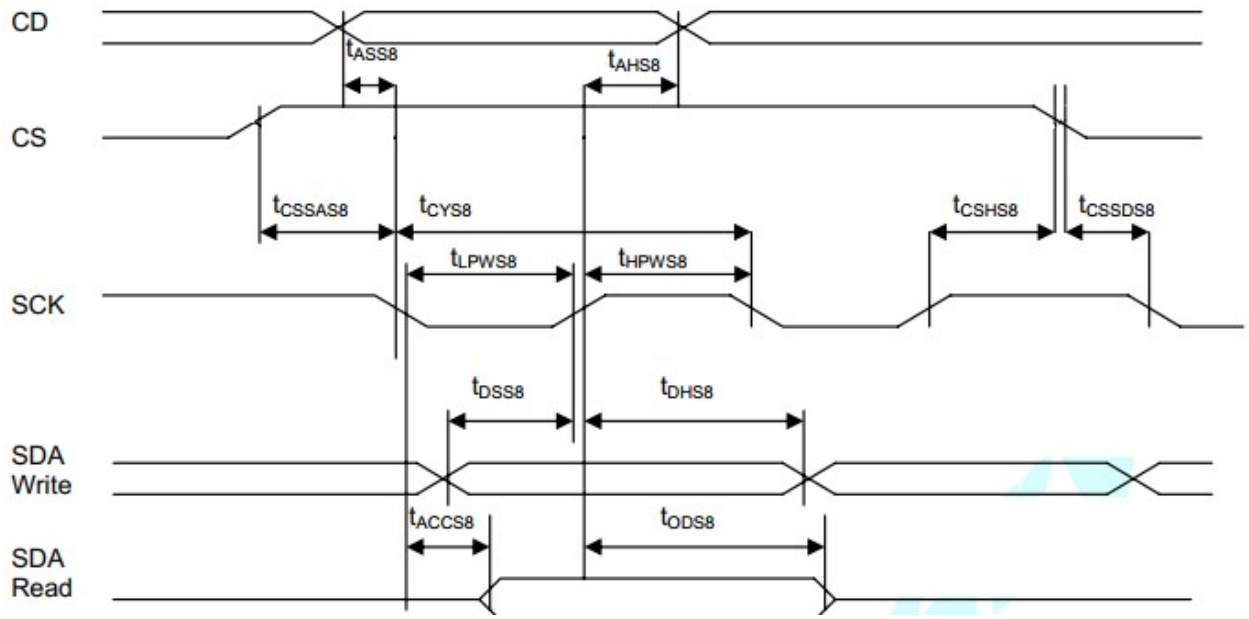


V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time (D/C)	Tas68	5	-	-	ns
Address hold time (D/C)	Tah68	25	-	-	ns
System cycle time	Tcy68	280	-	-	ns
Read pulse width	tpwr68	100	-	-	ns
Write pulse width	Tpww68	65	-	-	ns
High pulse width (read)	Thpw68	100	-	-	ns
High pulse width (write)	Thpw68	65	-	-	ns
Data setup time	Tds68	45	-	-	ns
Data hold time	Tdh68	10	-	-	ns
Data access time	Tacc68	-	-	150	ns
Data output disable time	tod68	120	-	-	ns

Note:
*1. Input signal rise/fall time should be less than 15ns .
*2. CL=100pF
*3.All timing is using 20% and 80% of VDD as the reference.

3.3.3 4-Wire SPI Timing

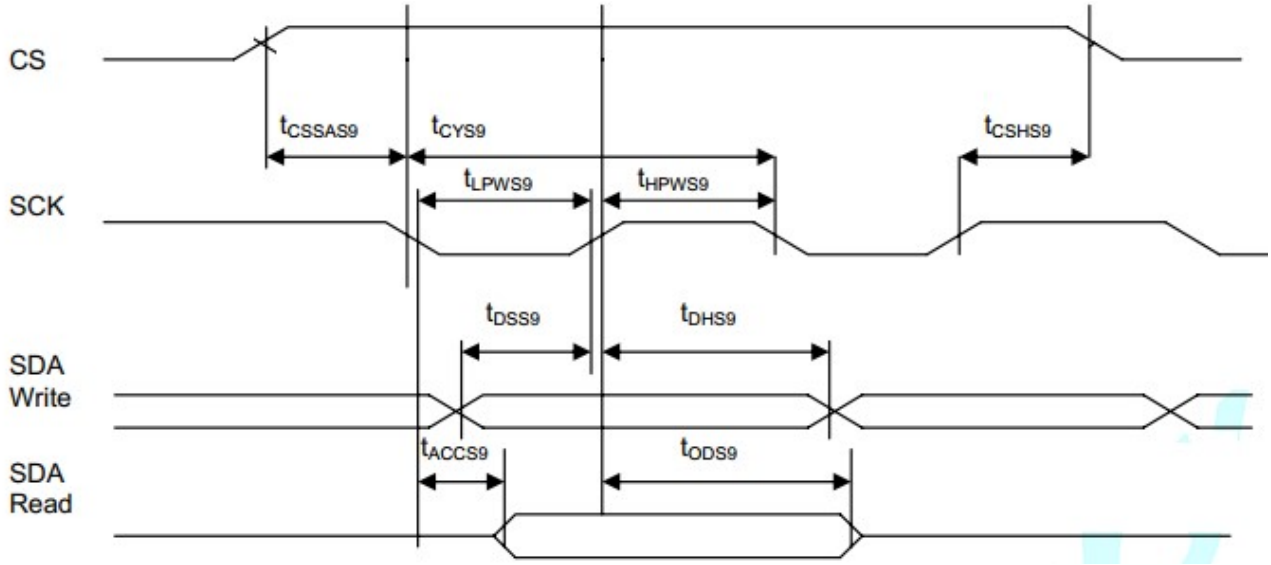


V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time (D/C)	Tas8	5	-	-	ns
Address hold time (D/C)	Tah8	15	-	-	ns
Chip select setup time	Tcssa8	5	-	-	ns
Chip select hold time	Tcshs8	15	-	-	ns
System cycle time	Tcy8	250	-	-	ns
Data setup time	tdss8	20	-	-	ns
Data hold time	Tdhs8	25	-	-	ns
Read access time	Taccs8	-	-	110	ns
Output disable time	Tods8	80	-	-	ns

Note:
*1. Input signal rise/fall time should be less than 15ns .
*2. CL=100pF
*3.All timing is using 20% and 80% of VDD as the reference.

3.3.4 3-Wire SPI Timing

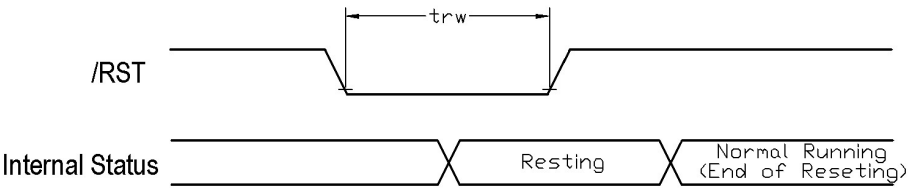


V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time (D/C)	Tas9	5	-	-	ns
Address hold time (D/C)	Tah9	15	-	-	ns
System cycle time	Tcy9	250	-	-	ns
Data setup time	Tdss9	20	-	-	ns
Data hold time	Tdhs9	25	-	-	ns
Read access time	Taccs9	-	-	110	ns
Output disable time	Tods9	80	-	-	ns

Note:
*1. Input signal rise/fall time should be less than 15ns .
*2. CL=100pF
*3.All timing is using 20% and 80% of VDD as the reference.

3.3.5 Reset Timing



V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset LOW pulse width	trw	1.3	-	-	μs

Note:
*1.All timing is using 20% and 80% of VDD as the reference.

4. Function specifications

4.1 Adjusting the Display Contrast

- This LCD module equipped with latest digital contrast adjustment function.
- Its display contrast could be adjusted by MCU command. (please see the command tables for details)
- It is recommended to provide a contrast adjustment interface for end-user, where the best display result could meet the individual preference in mass production.

4.2 Resetting the LCD module

The LCD module should be initialized by using /RST terminal.
While turning on the VDD and VSS power supply, maintain /RST terminal at LOW level. After the power supply stabilized, release the reset terminal (/RST=HIGH)

4.2.1 Display Memory Map

Page address	data	LCD Display (front view)
0	DB0 : DB7	240x120 pixels
1	DB0 : DB7	
2	DB0 : DB7	
: :	DB0 : DB7	
	DB0 : DB7	
12	DB0 : DB7	
13	DB0 : DB7	
14	DB0 : DB7	
Column Address		0Fh → FEh

Note:
*1. MUX Rate, duty =1/120,Bias=1/11;
*2. SEG mirror, MX=0 (normal X direction)
*3. COM mirror, MY=1 (mirror Y direction)

4.3 Display Commands

The LCD module contains register, which control the operation. These register can be modified by commands. The following table is a summary of the control registers, their meaning and their default value.

4.3.1 Register Table

Name	Bits	Default	Description
SL	6	00H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (127– 2xFL). Setting SL outside of this range causes undefined effect on the displayed image.
FL	4	0H	Fixed Lines. The first FLx2 lines of each frame are fixed and are not affected by scrolling (SL). When FL is non-zero, the screen is effectively separated into two regions: one scrollable, one non-scrollable.
CR	8	00H	Return Column Address. Useful for cursor implementation.
CA	8	00H	Display Data RAM Column Address (Used in Host to Display Data RAM access)
PA	4	0H	Display Data RAM Page Address (Used in Host to Display Data RAM access)
BR	2	2H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b= 10.7 01b= 11.3 **10b= 12.0** 11b= 12.7
TC	2	0H	Temperature Compensation (per °C). **00b: 0.0%** 01b: -0.05% 10b: -0.1% 11b: -0.2%
GN	2	3H	Gain, coarse setting of V_{BIAS} and V_{LCD}
PM	6	00H	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
MR	1	1H	Multiplexing Rate: Number of pixel rows: 0b: 96 **1b: 128**
OM	2	–	Operating Modes (Read Only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
BZ	1	–	Busy with internal processes (reset, changing mode, etc.) OK for Display RAM read/write access.
RS	1	–	Reset in progress, Host Interface not ready
PC	3	5H	Power Control. PC[1:0]: Panel Loading 00b: LCD < 26nF **01b: 26nF < LCD < 43nF** 10b: 43nF < LCD < 60nF 11b: 60nF < LCD < 90nF For COG module, the ITO substrate for SEG plate and COM routing: 15Ω/Sq - 15nF < LCD < 35nF. 10Ω/Sq - 35nF < LCD < 50nF 7Ω/Sq - 50nF < LCD < 75nF PC[2]: Pump Control 0b: External V_{LCD} **1b: Internal V_{LCD}**
DC	3	0H	Display Control: DC[0]: PXV: Pixels Inverse (Default **0 : OFF**) DC[1]: APO: All Pixels ON (Default **0 : OFF**) DC[2]: Display ON/OFF (Default **0 : OFF**).
AC	4	1H	Address Control: AC[0]: WA: Automatic column/page Wrap Around (Default **1 : ON**) AC[1]: Reserved (always set to **0**) AC[2]: PID: PA (page address) auto increment direction (**0: +1,** 1: -1) AC[3]: CUM: Cursor update mode, (Default **0:OFF**) when CUM=1, CA increment on write only, wrap around suspended
LC	4	0H	LCD Mapping Control: LC[0]: MSF: MSB First mapping Option (Default **0 : OFF**) LC[1]: Reserved (always set to **0**) LC[2]: MX, Mirror X (Column sequence inversion) (Default **0 : OFF**) LC[3]: MY, Mirror Y (Row sequence inversion) (Default **0 : OFF**)
APC0	8	2AH	Advanced Product Configuration. For UltraChip only. Please do not use.
APC1	4	EH	Advanced Product Configuration. For UltraChip only. Please do not use.

Note: Please refer to UC1618 data sheet for details

4.3.2 Command Table

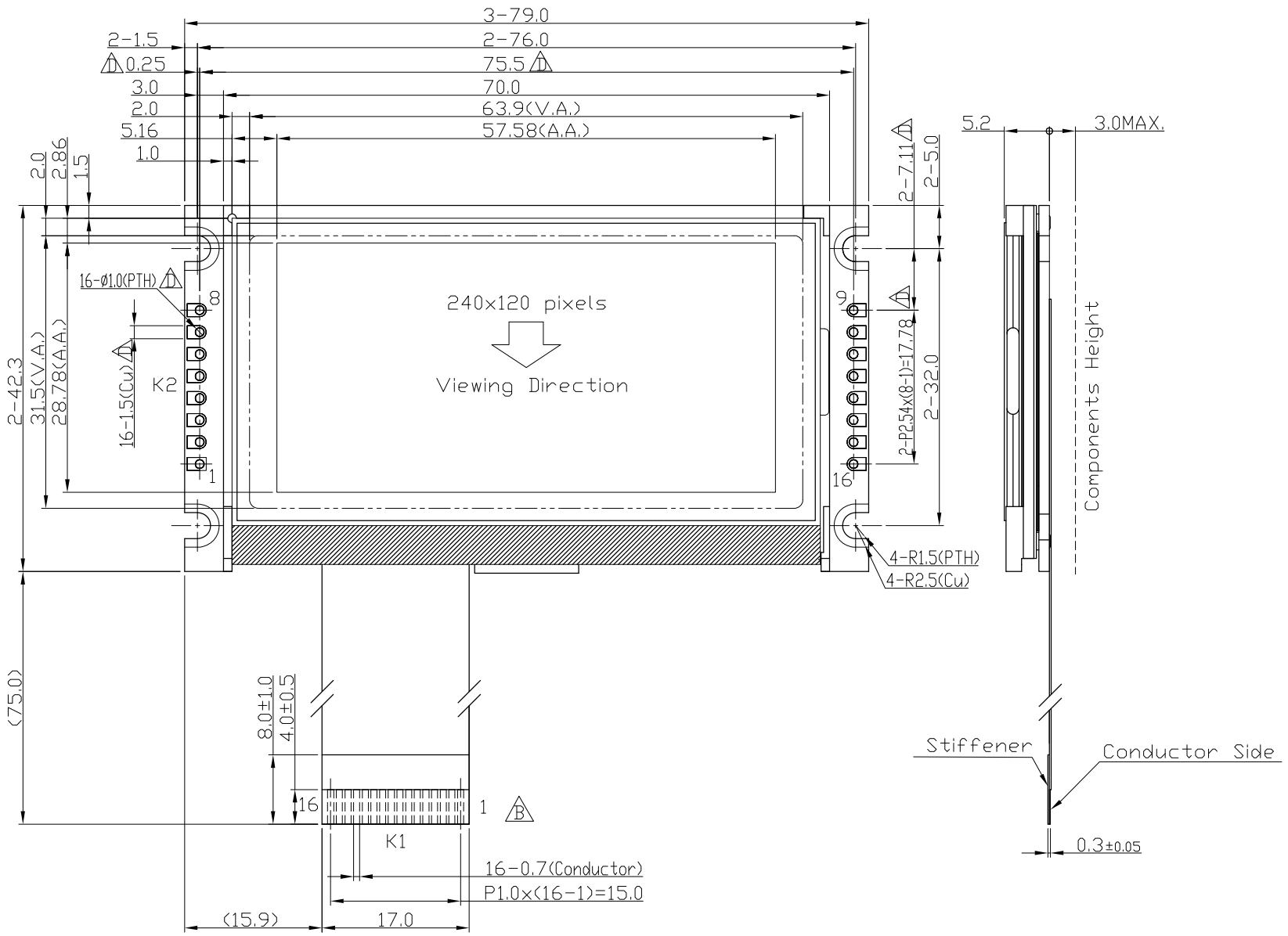
The following is the list of host command supported.

No	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3.	Get Status	0	1	0	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Prod, PID}	N/A
				Ver[1:0]		PMO[5:0]							
				Prod		PID	0	0	0	0	0		
4.	Set Column Address	0	0	0	0	0	0	0	0	0	0	Set CA[8:0]	000H
				#	#	#	#	#	#	#	#		
				-	-	-	-	-	-	-	#		
5.	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
6.	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7.	Set Pump Control	0	0	0	0	1	0	1	1	0	#	Set PC[2]	1b
8.	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	R	R	Set APC[R][7:0], R = 0~3	N/A
		0	0	#	#	#	#	#	#	#	#		
9.	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0H
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0H
10.	Set Page Address LSB	0	0	0	1	1	0	#	#	#	#	Set PA[3:0]	0H
	Set Page Address MSB	0	0	0	1	1	1	-	-	-	#	Set PA[4]	0H
11.	Set V_{BIAS} Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	C3H
				#	#	#	#	#	#	#	#		
12.	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[9]	0b: Disable
13.	Set COM Scan Function	0	0	1	0	0	0	0	1	1	#	Set CSF[0]	0b
14.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
15.	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set FLT[3:0], FLB[3:0]	00H
				#	#	#	#	#	#	#	#		
16.	Set Display mode	0	0	1	0	0	1	0	1	#	#	Set DC[5:4]	00b
17.	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
18.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
19.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
20.	Set Display Enable	0	0	1	0	1	0	1	1	#	#	Set DC[3:2]	10b
21.	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b
22.	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[6:0]	00H
				-	#	#	#	#	#	#	#		
23.	Set LCD Gray Shade 1	0	0	1	1	0	1	0	0	#	#	Set LC[6:5]	01b
24.	Set LCD Gray Shade 2	0	0	1	1	0	1	0	1	#	#	Set LC[8:7]	10b
25.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
26.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
27.	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
				#	#	#	#	#	#	#	#		
28.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 11
29.	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[4]=0, CA=CR	N/A
30.	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[4]=1, CR=CA	N/A
31.	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	127
				-	#	#	#	#	#	#	#		
32.	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
				-	#	#	#	#	#	#	#		
33.	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	127
				-	#	#	#	#	#	#	#		

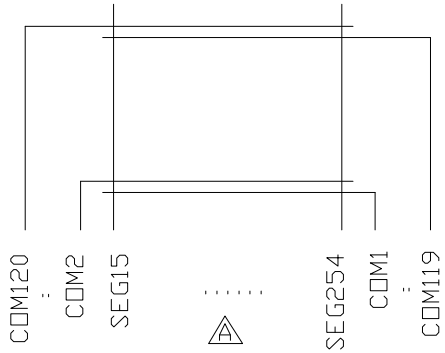
Note:
Please refer to UC1618 data sheet for details
R/W=0 means it is a write function, R/W=1 means it is a read function
D/C=0 means it is a control data, D/C=1 means it is a display data

5. Design and Handling Precaution

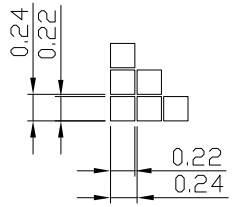
Please refer to "LCD-Module-Design-Handling-Precaution.pdf".



K1/K2 Terminal	
No.	Pin Name
1	VSS
2	VDD
3	DB7
4	DB6
5	DB5
6	DB4
7	DB3
8	DB2
9	DB1
10	DB0
11	/RD
12	/WR
13	D/C
14	/RST
15	CS
16	BLA



Wiring Details
Scale=free



Pixels Details
Scale=20/1

Note:
*1. Display Type : STN-Blue, Negative, Transmissive
*2. Viewing Direction : 12H
*3. Duty : 1/120 ; Bias : 1/11
*4. Operating Voltage : 3.3V
*5. Backlight Color : White
*6. Backlight Supply : 3.3V TYP.
*7. Operating Temperature : -30°C~80°C C
*8. Storage Temperature : -40°C~85°C

Rev	Note	Date
D	Add Dimension	Luo Lin 2019-02-21
C	Revise Top	Zhou 2014-02-11
B	Add FFC	Zhou 2014-01-23
A	Revise Wiring	Deng Junjie 2013-01-03

Dwg Title	LM240120HFW Outline Dwg		
Dwg No.	MK-004214d-1-1		Date 2012-10-24
Scale 2/1	Tol. ±0.5	Unit mm	Paper Size A3
Approved	Checked	Drawn Zhou	

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