

# LM3033DFW-0B

## LCD Module User Manual

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0.1	Preliminary New release	18-Dec-2007

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# 1. Basic Specifications

## 1.1 Display Specifications

- 1) LCD Display Mode : STN, Negative, Transmissive
- 2) Display Color : Display Data = "1" : Light Gray (\*1)  
: Display Data = "0" : Deep Blue (\*2)
- 3) Viewing Angle : 6 H
- 4) Driving Method : 1/33 duty, 1/5bias
- 5) Back Light : White LED backlight

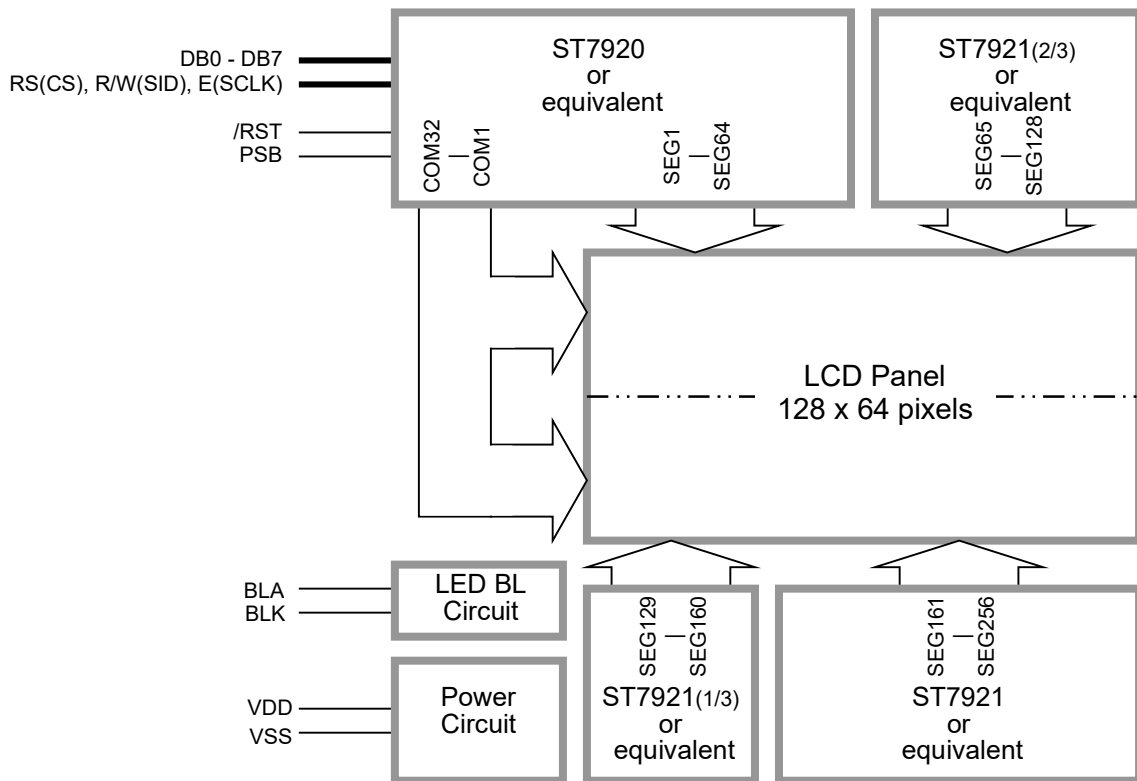
Note:

- \*1. Color tone may slightly change by Temperature and Driving Condition
- \*2. The Color is defined as the inactive / background color

## 1.2 Mechanical Specifications

- 1) Outline Dimension : 93.0 x 70.0 x 12.1MAX  
(see attached Outline Drawing for details)

## 1.3 Block Diagram



## 1.4 Terminal Functions

Pin No.	Pin Name	I/O	Descriptions	
			Parallel mode (PSB=H)	Serial Mode (PSB=L)
1	VSS	Power	Negative Power Supply, Ground (0V)	
2	VDD	Power	Positive Power Supply	
3	NC	-	No Connection (keep open)	
4	RS (CS)	Input	Register Select RS=H; data read or write RS=L; Instruction data write or status busy flag read	Chip Select (*1) CS=H, enable the data transfer. CS=L, reset the serial data counter
5	R/W (SID)	Input	Read write control R/W=H; data or status read R/W=L; data or command write	Chip Select SID=serial data line
6	E (SCLK)	Input	E=Enable trigger	SCLK=Serial Clock
7	DB0	I/O	Three state I/O terminal for display data or instruction data In 4 bit mode, DB3~DB0 could leave open or pull-up	In serial mode, these terminal could leave open or pull-up
:	:	:		
14	DB7	I/O		
15	PSB	Input	Interface selection: PSB=L; serial mode PSB=H; 8 or 4 bit parallel bus mode	
16	NC	-	No Connection (keep open)	
17	/RST	Input	System reset; low active	
18	NC	-	No Connection (keep open)	
19	BLA	Power	Positive Power for LED backlight	
20	BLK	Power	Negative Power for LED backlight	

Note:

- \*1. In serial mode, the CS is for resetting the serial data shifting counter, It could not disable the data shifting into the LCD module.

## 2. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	$V_{DD}$	-0.3	5.5	V	$V_{SS} = 0V$
Input Voltage	$V_{IN}$	-0.3	$V_{DD}+0.3$	V	$V_{SS} = 0V$
Operating Temperature	$T_{OP}$	-20	70	°C	No Condensation
Storage Temperature	$T_{ST}$	-30	80	°C	No Condensation

Cautions:

Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

## 3. Electrical Characteristics

### 3.1 DC Characteristics

$V_{SS}=0V, V_{DD} =5.0V, T_{OP} =25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Operating Voltage	$V_{DD}$	4.8	5.0	5.2	V	VDD
Input High Voltage	$V_{IH1}$	$0.8V_{DD}$	-	$V_{DD}$	V	RS, R/W, E, PSB, /RST, DB0-DB7
Input Low Voltage	$V_{IL1}$	$V_{SS}$	-	0.4	V	DB0-DB7
Output High Voltage	$V_{OH1}$	$0.7V_{DD}$	-	$V_{DD}$	V	DB0-DB7 ( $I_{OH} = -0.1mA$ )
Output Low Voltage	$V_{OL1}$	$V_{SS}$	-	0.6	V	DB0-DB7 ( $I_{OL} = 0.1mA$ )
Operating Current	$I_{DD}$	-	2.3	5.5	mA	VDD, VSS

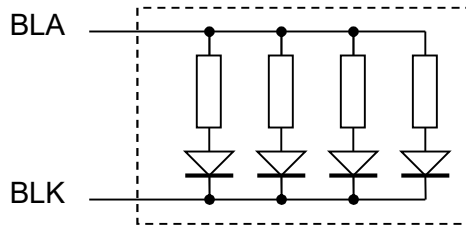
### 3.2 LED Backlight Circuit Characteristics

$BLK=0V, I_{f_{BLA}}=80mA, T_{OP} =25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Forward Voltage	$V_{fA}$	-	5.0	-	V	BLA
Forward Current	$I_{fA}$	-	80	100	mA	BLA

Cautions:

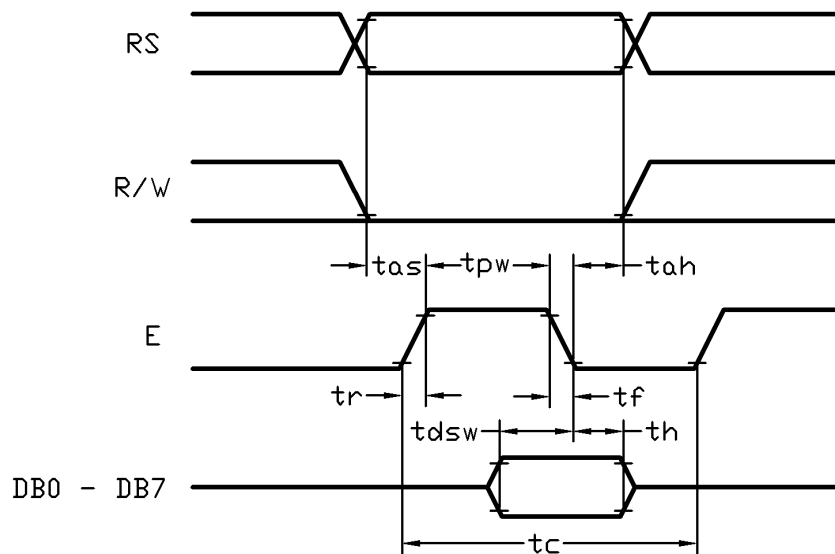
Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.



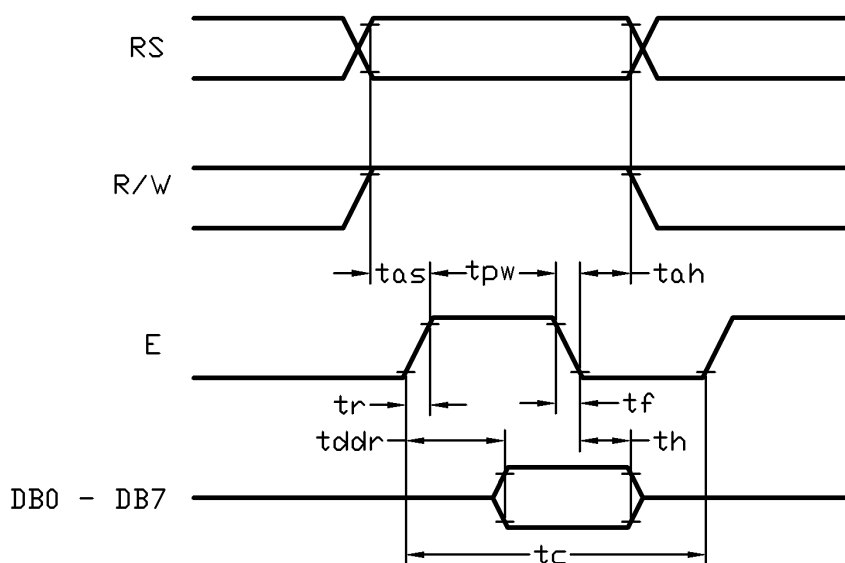
**3.3 AC Characteristics (Parallel Mode Interface)**

$V_{SS}=0V, V_{DD}=5V, T_{OP}=25^{\circ}C$

Item	Symbol	MIN.	TYP.	MAX.	Unit
E cycle time	tc	1500	-	-	ns
E high level width	tpw	175	-	-	ns
E rise time	tr	-	-	20	ns
E fall time	tf	-	-	20	ns
Address set-up time	tas	13	-	-	ns
Address hold time	tah	25	-	-	ns
Data set-up time	tdsw	50	-	-	ns
Data delay time	tddr	-	-	125	ns
Data hold time	th	25	-	-	ns



**Host Write Timing Diagram (Parallel Mode)**

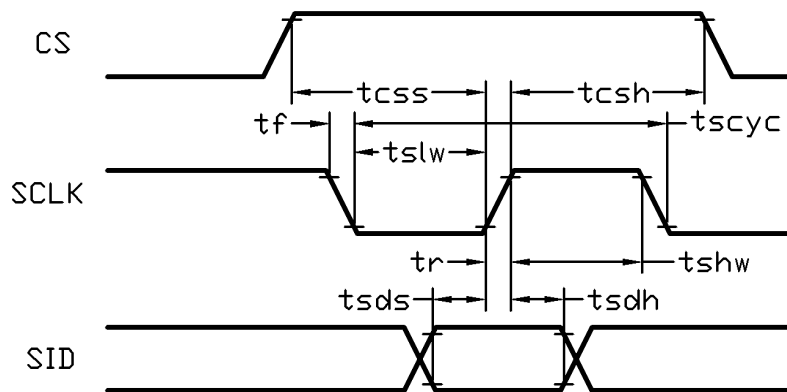


**Host Read Timing Diagram (Parallel Mode)**

**3.4 AC Characteristics (Serial Mode Interface)**

$V_{SS}=0V, V_{DD}=5V, T_{OP}=25^{\circ}C$

Item	Symbol	MIN.	TYP.	MAX.	Unit
Clock Cycle	tscyc	500	-	-	ns
SCLK high pulse width	tshw	250	-	-	ns
SCLK low pulse width	tslw	250	-	-	ns
SCLK rise time	tr	-	-	20	ns
SCLK fall time	tf	-	-	20	ns
SID data setup time	tsds	50	-	-	ns
SID data hold time	tsdh	50	-	-	ns
CS setup time	tcss	75	-	-	ns
CS hold time	tcsh	75	-	-	ns

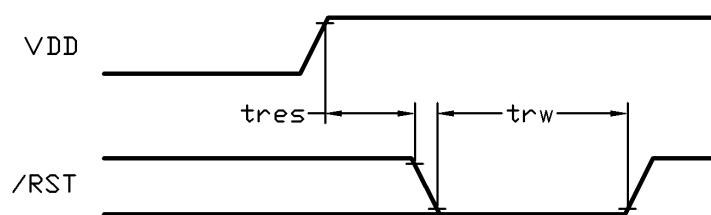


**Host Write Timing Diagram (Serial Mode)**

**3.5 Reset Timing**

$V_{SS}=0V, V_{DD}=5V, T_{OP}=25^{\circ}C$

Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset Pulse width	trw	2.0	-	-	us
Reset Start time	tres	-	-	100	ns



**Reset Timing Diagram**

## 4. Function Specifications

### 4.1 Resetting the LCD module

The LCD module should be initialized by setting /RST terminal at low level when turning the power on. See the reset timing section for details.

The initialized status is as follow:

Functions	Initialized Status
ENTER MODE SET	I/D=1 cursor move to right S=0 DDRAM address counter (AC) plus 1
DISPLAY STATUS	D=0 display = OFF C=0 cursor = OFF B=0 cursor position blink = OFF
FUNCTION SET	DL=1 8bit Interface RE=0 Basic Instruction Set
SCROLL OR RAM ADDR. SELECT	SR=0 CGRAM address access is enabled
REVERSE	R1=0, R0=0 First line normal
EXTENDED FUNCTION SET	G=0 Graphic Display OFF

### 4.2 Using Parallel interface

When PSB=H, the LCD module is in parallel interface mode. 8-bit or 4-bit bus interface could be selected by FUNCTION SET instruction DL bit.

In 4-bit bus interface, every 8-bit instruction/data is separated into two parts. First, transfer the higher 4-bit (D7~D4). Then transfer the lower 4-bit (D3~D0). They are transferred via DB7~DB4 terminals, where DB3~DB0 are not in used (leave open or pull high)

### 4.3 Using Serial interface

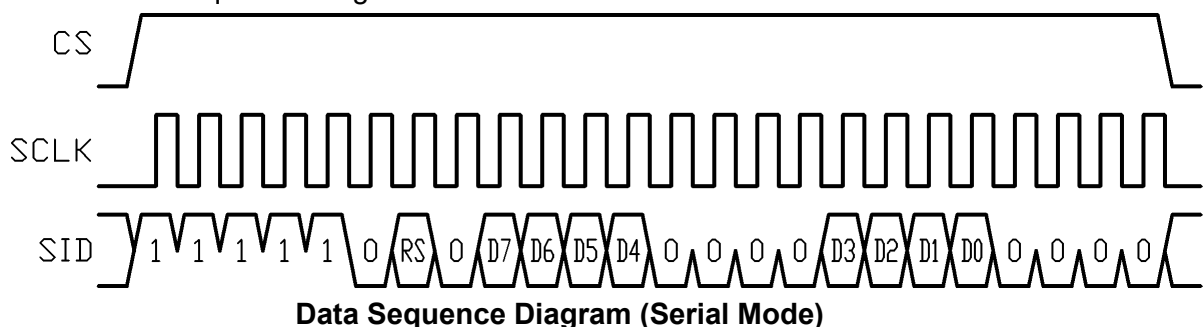
When PSB=L, the LCD module is in serial interface mode (write only).

In this mode, CS pin should be used. CS=H, enable the data transfer. CS=L, reset the serial data counter, terminate the data transition and clear the data buffer.

As the controller IC have no instruction buffer area, it must wait for the previous instruction to finish before sending the next one. Thus transferring multiple instruction/data, execution time must be considered.

Starting a transmission, a start byte is required. It consists 5 consecutive "1" follow with a "0", a RS bit (Register Select bit) and a "0".

Then the 8bit instruction/data should be separated into 2 groups. First group is DB7 to DB4, followed by 4 consecutive "0". The second group is DB3 to DB0 with 4 consecutive "0". See the Data Sequence Diagram for details.





**4.4 Display Memory Map**

There are three main memory-areas in the LCD module for display.

- Character Generator RAM (CGRAM)
- Graphic Display RAM (GDRAM)
- Display Data RAM (DDRAM)

**4.4.1 Character Generator RAM (CGRAM)**

Character Generator RAM is for storing the User-defined Characters (a 16x16 dots font). There are only four characters could be defined. The User-defined Character Codes are 0000h and 0002h. They could be called into DDRAM as normal character.

User-defined Character Code	CGRAM Address	CGRAM data	
		D15 ~ D8	D7 ~ D0
0000h	00h : 0Fh	16 x 16 dot font	
0002h	10h : 1Fh	16 x 16 dot font	
0004h	20h : 2Fh	16 x 16 dot font	
0006h	30h : 3Fh	16 x 16 dot font	

**CGRAM Address Map**

**4.4.2 Graphics Display RAM (GDRAM)**

GDRAM is for full graphics display. It could be displayed when G=1 (set by EXTENDED FUNCTION SET in Extended Instruction Set)

		Horizontal Address (X)					
		00h	01h	~	06h	07h	
		D15 ~ D0	D15 ~ D0	~	D15 ~ D0	D15 ~ D0	
Vertical Address (Y)	00h						
	01h						
	⋮						
	1Eh						
	1Fh						
	00h						
	01h						
	⋮						
	1Eh						
	1Fh						
			D15 ~ D0	D15 ~ D0	~	D15 ~ D0	D15 ~ D0
			08h	09h	~	0Eh	0Fh
		Horizontal Address (X)					

**GDRAM Address Map**

Note:

- \*1. The mapping is based on Vertical Scroll Displacement Address=0.
- \*2. Another 128x64 Graphics Display RAM space is not showed. They could be displayed by adjusting the Vertical Scroll Displacement Address value.

**4.4.3 Display Data RAM (DDRAM)**

GB Character Code (16bit, A1A0h~F7FFh) could write into DDRAM for displaying the Simplified Chinese Character (16x16 dots font). User Characters (16bit, 0000h or 0002h) defined by user that stored in CGRAM could also be used. The display character should be on grid only.

		DDRAM Address (Lower 4bit)															
		00h		01h		02h		03h		04h		05h		06h		07h	
		H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
DDRAM Address (Upper 4bit)	80h	<div style="border: 1px solid black; padding: 10px; display: inline-block;"> <b>8 x 4 Characters (16x16 dots font)</b> </div>															
	90h																
	80h																
	90h																
		H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
		08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh								
		DDRAM Address (Lower 4bit)															

**DDRAM Address Map with 16x16 dots font**

Note:

- \*1. The mapping is based on Vertical Scroll Displacement Address=0.
- \*2. Another 8x4(Characters) Display Data RAM space is not showed. They could be displayed by adjusting the Vertical Scroll Displacement Address value.

Standard ASCII code (8bit, 00h~7Fh) could write into DDRAM for displaying the Standard ASCII Character (8x16 dots font). The display character should be on grid only, and two characters should be written in each write operation.

		DDRAM Address (Lower 4bit)															
		00h		01h		02h		03h		04h		05h		06h		07h	
		H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
DDRAM Address (Upper 4bit)	80h	<div style="border: 1px solid black; padding: 10px; display: inline-block;"> <b>16 x 4 Characters (8x16 dots font)</b> </div>															
	90h																
	80h																
	90h																
		H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
		08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh								
		DDRAM Address (Lower 4bit)															

**DDRAM Address Map with 8x16 dots font**

Note:

- \*1. The mapping is based on Vertical Scroll Displacement Address=0.
- \*2. Another 16x4(Characters) Display Data RAM space is not showed. They could be displayed by adjusting the Vertical Scroll Displacement Address value.

**4.5 Display Control Instructions**

**4.5.1 Basic Instruction Set**

RE=0, basic instruction set

Instructions	Code										Function	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
CLEAR	0	0	0	0	0	0	0	0	0	1	Fill DDRAM with "20h", and set DDRAM address counter (AC) to "00h"	
HOME	0	0	0	0	0	0	0	0	0	1	X	Set DDRAM address counter (AC) to "00h" and put cursor to origin. DDRAM content no changed.
ENTRY MODE	0	0	0	0	0	0	0	0	1	I/D	S	Set cursor position and display shift when doing write or read operation I/D=1, cursor move right AC increased by 1 I/D=0, cursor move left, AC decreased by 1 S=1, toggle the shift of the entire display (based on I/D defined direction)
DISPLAY ON/OFF	0	0	0	0	0	0	0	1	D	C	B	D=1, display ON D=0, display OFF C=1, cursor ON C=0, cursor OFF B=1, blink ON B=0, blink OFF
CURSOR DISPLAY CONTROL	0	0	0	0	0	0	1	S/C	R/L	X	X	Cursor position and display shift control. DDRAM content no changed.
FUNCTION SET	0	0	0	0	0	1	DL	X	RE	X	X	DL=1, 8bit interface DL=0, 4bit interface RE=1, extended instruction RE=0; basic instruction
SET CGRAM ADDR	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0		Set CGRAM address to address counter (AC) Make sure that in extended instruction SR=0 (scroll or RAM address selected)
SET DDRAM ADDR	0	0	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Set DDRAM address to address counter (AC), where AC7 =1, AC6=0
READ BF & ADDR	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Read busy flag (BF) for completion of the internal operation, also read out the value of AC
WRITE RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0		Write data to internal RAM (DDRAM, CGRAM,GDRAM) For 16bit data, write two byte consecutively, high byte first, then low byte
READ RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0		Read data from internal RAM (DDRAM, CGRAM,GDRAM)

Note:

\*1. For the details of the Display Control Instructions, please refer to Sitronix ST7920 series datasheet.

\*2. RE is the selection byte of basic and extended instruction set. Each time altering the value of RE, it will remain. Thus, it is not necessary to set RE every time when using the same group of instruction set

**4.5.2 Extended Instruction Set**

RE=1, extended instruction set

Instructions	Code										Function
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
SCROLL or RAM ADDR SELECT	0	0	0	0	0	0	0	0	1	SR	SR=1, enable vertical scroll position SR=0, enable CGRAM address (basic instruction)
REVERSE	0	0	0	0	0	0	0	1	R1	R0	Toggle 1 out of 4 line (in DDRAM) of the display to be reversed (initial value is R1 ,R0 = 0, 0
EXTENDED FUNCTION SET	0	0	0	0	1	DL	X	RE	G	0	DL=1, 8bit interface DL=0, 4bit interface RE=1, extended instruction RE=0; basic instruction G=1, graphics display ON G=0, graphics display OFF
SET SCROLL ADDR	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set the address of vertical scroll Make sure extended instruction SR=1, enable vertical scroll position.
SET GRAPHICS RAM ADDR	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set the GDRAM address to address counter (AC) Dual byte command should write consecutively First byte set the Vertical address AC6~AC0 Second byte set the Horizontal address AC3~AC0
	0	0	1	0	0	0	AC3	AC2	AC1	AC0	

Note:

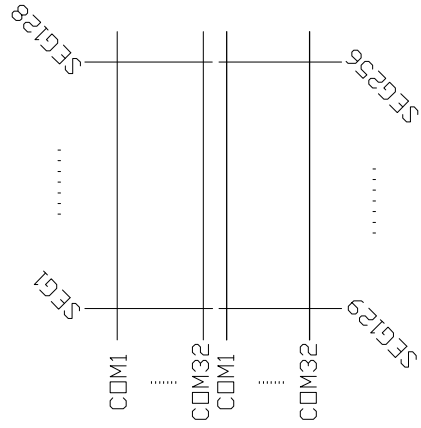
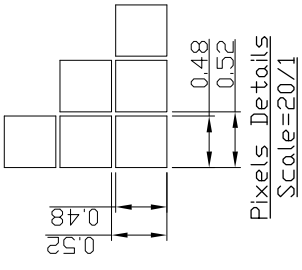
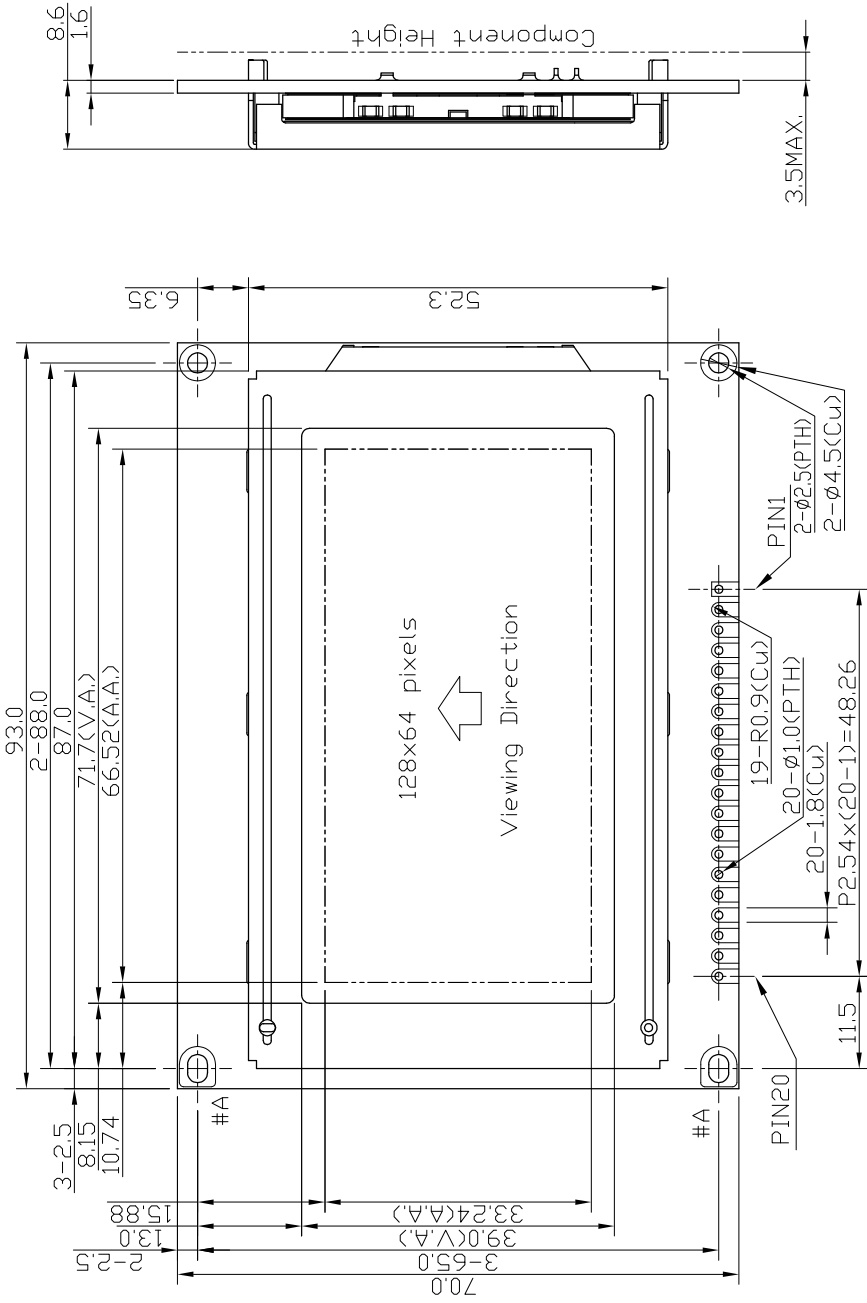
\*1. For the details of the Display Control Instructions, please refer to Sitronix ST7920 series datasheet.

\*2. RE is the selection byte of basic and extended instruction set. Each time altering the value of RE, it will remain. Thus, it is not necessary to set RE every time when using the same group of instruction set

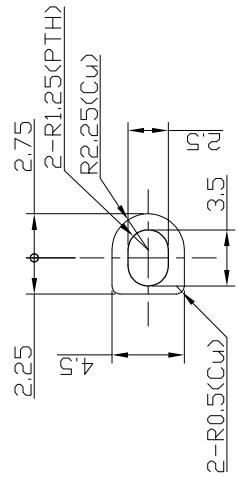
## **5. Design and Handling Precaution**

Please refer to "LCD-Module-Design-Handling-Precaution.pdf".

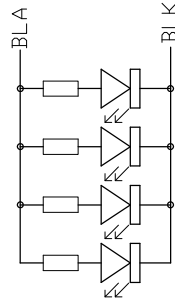
Terminal No.	Pin Name
1	VSS
2	VDD
3	NC
4	RS(CS)
5	R/W(STD)
6	E(SCLK)
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	PSB
16	NC
17	/RST
18	NC
19	BLA
20	BLK



Wiring Details  
Scale=free



#A Details  
Scale=3/1



Backlight Circuit  
(No. of LEDs = 4pcs)  
Scale=free

- Note:
- \*1. LCD Display Type : STN, Negative, Transmissive
  - \*2. Viewing Direction : 6H
  - \*3. LCD Driving Duty : 1/33
  - \*4. Operating Voltage : 5.0V
  - \*5. Backlight Color : White
  - \*6. Operating Temperature : -20°C ~ 70°C
  - \*7. Storage Temperature : -30°C ~ 80°C

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