深圳市拓普微科技开发有限公司
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LMT056DIDFWD-AEA

LCD Module User Manual

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Lu jianhui		
Date: 2018-02-07	Date:	Date:

Rev.	Descriptions	Release Date
0.1	Preliminary	2016-12-28
0.2	Update section 2,7	2018-2-7

Table of Content

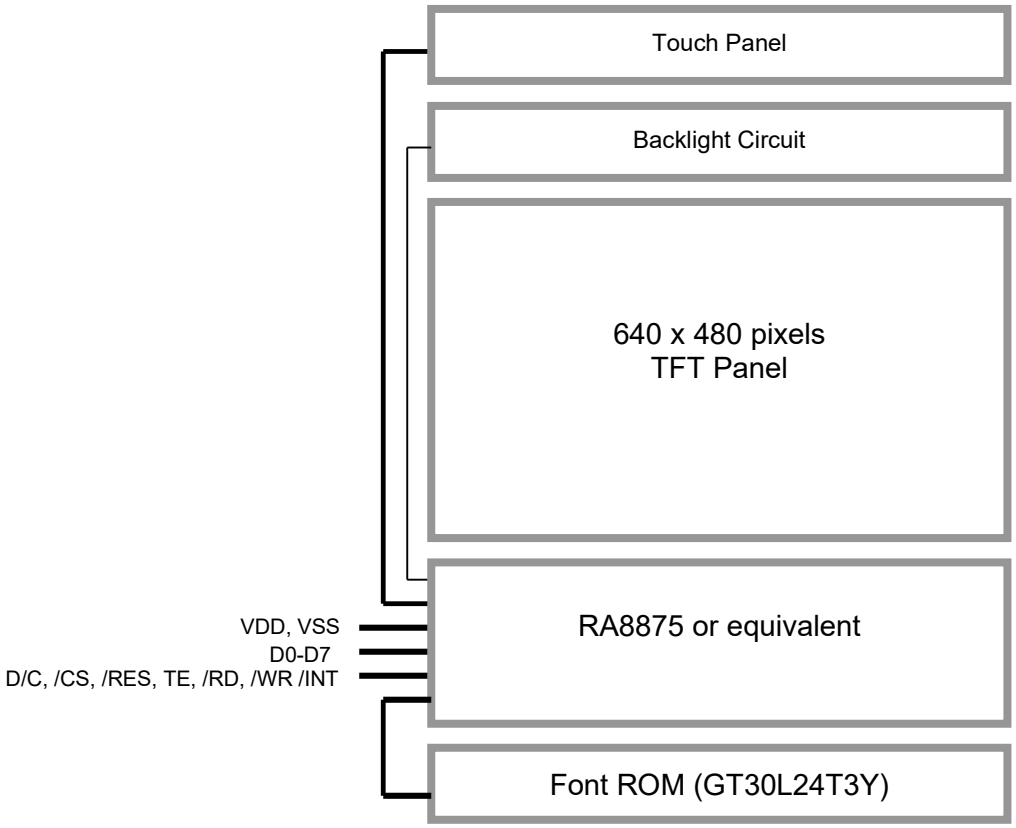
1. General Specification

Screen Size(Diagonal) :	5.6”
Outline Dimension :	155.2 x 109.0 x 15.4max (mm) (see attached drawing for details)
Active Area :	112.896 x 84.672 (mm)
Color Depth:	65k
Number of dots :	640 x 3(RGB) x 480
Pixel Pitch :	0.0588 x 0.1764 (mm)
Pixel Configuration :	RGB Stripe
Backlight :	LED
Surface Treatment :	Anti-Glare Treatment
Viewing Direction :	12H (gray scale inverse)(*2) 6H(*3)
Operating Temperature :	-20 ~ +70°C
Storage Temperature :	-30 ~ +80°C

Note:
*1 Color tune may slightly changed by temperature and driving voltage.
*2. For saturated color display content (eg. pure-red, pure-green, pure-blue, or pure-colors-combinations)
*3. For "color scales" display content

2. Block Diagram

3.



Terminal Functions

3.1 Interface

Pin No.	Pin Name	I/O	Descriptions
1	VSS	P	Power Ground
2	VSS		
3	VDD	P	Positive Power Supply
4	VDD		
5	D/C	I	Register Select D/C = H, status read/command write cycle is selected. D/C = L, data Read/Write cycle is selected.
6	/CS	I	Chip Select /CS=L, enable access to the LCD interface /CS=H, disable access to the LCD interface
7	/RES	I	Reset signal /RES = L, Initialization is executed /RES = H, Normal running.
8	D0	I/O	Data BUS
:	:	:	
15	D7	I/O	
16	TE	O	Controller busy signal output,It is active low and could be used for MCU to pull busy status by connecting it to I/O port, MCU should poll this signal before accessing the LCD module
17	/RD	I	/WR=H, /RD=L; Data or Status read form the LCD module
18	/WR	I	/WR=L→H, RD=H; Data or Instruction latch into the LCD module
19	NC	--	No Connection
20	NC	--	No Connection
21	/INT	O	Interrupt signal output
22	NC	--	No Connection
:	:	:	:
28	NC	--	No Connection

4. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	-0.3	+6.0	V	GND = 0V
Operating Temperature	T_{OP}	-20	+70	°C	No Condensation
Storage Temperature	T_{ST}	-30	+80	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

5. Electrical Characteristics

5.1 DC Characteristics (MCU terminal)

VDD=5.0V, VSS=0V, T_{OP} =25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Operating Voltage	VDD	4.8	5.0	5.2	V	VDD
Input High Voltage	V_{IH}	3.0	-	VDD	V	/RD, /WR, D/C, /CS, D0~D7, /RES
Input Low Voltage	V_{IL}	0	-	0.6	V	
Output Signal High Voltage	V_{OH}	3.0	-	3.6	V	D0~D7, TE
Output Signal Low Voltage	V_{OL}	0	-	0.6	V	
Operating Current	I_{DD}	-	450	-	mA	Backlight (100%PWM)
		-	349	-	mA	Backlight (70%PWM)

6. AC Characteristics

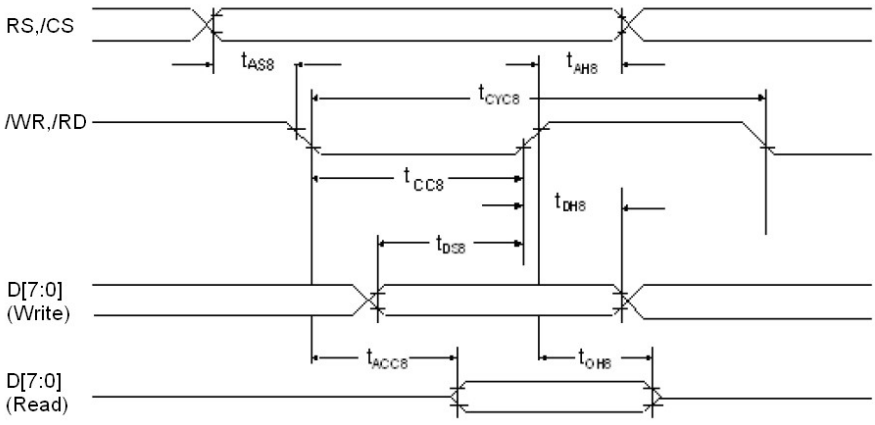
6.1 AC Timing

VDD=5.0V, VSS=0V, TOP =25°C

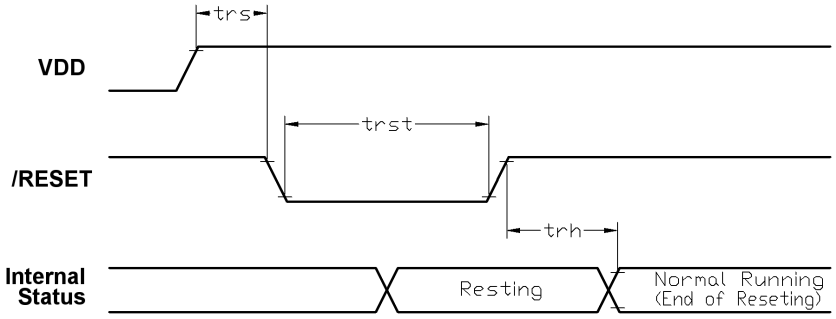
Parameter	Symbol	Spec.			Unit	Description
		Min.	Typ	Max.		
Cycle time	t_{CYC8}	71	-	-	ns	tc is one system clock period: tc = 1/SYS_CLK
Strobe Pulse width	t_{CCC8}	28	-	-		
Address setup time	t_{AS8}	5	-	-		
Address hold time	t_{AH8}	14	-	-		
Data setup time	t_{DS8}	28	-	-		
Data hold time	t_{DH8}	14	-	-		
Data output access time	t_{ACC8}	0	-	28		
Data output hold time	t_{OH8}	0	-	28		

Note:1. Refer to the RA8875 datasheet for more details.
2. SYS_CLK (System clock) = 30MHz

Register Write/Read timing (for CPU 8 Bit)



6.2 TFT Controller Reset Timing

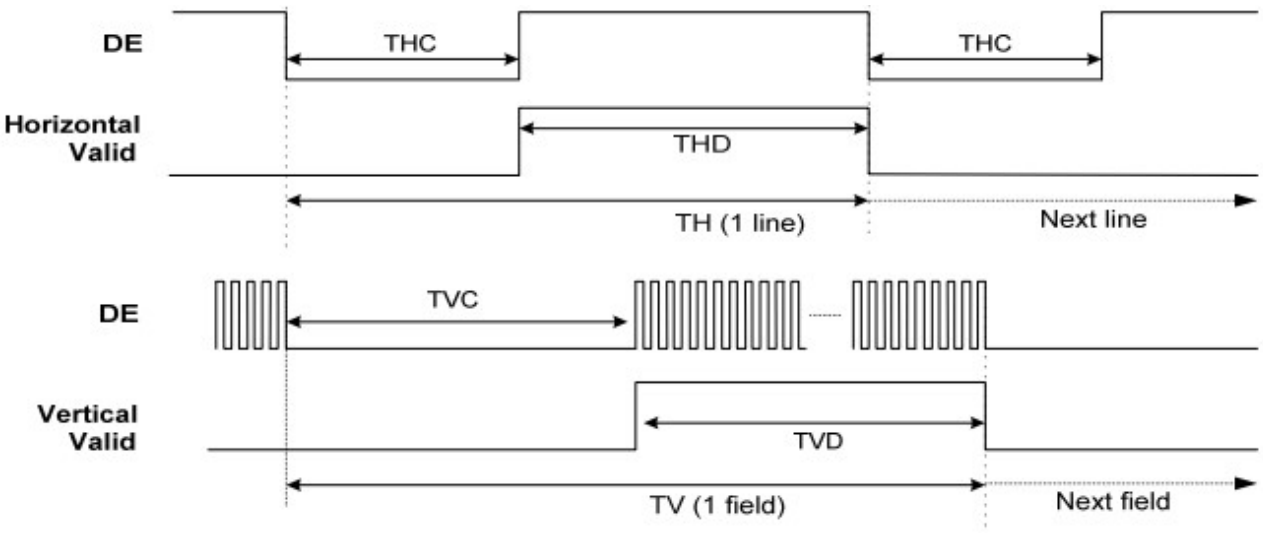


VSS=0V, VDD=5.0V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset setup time	trs	2	-	-	ms
Reset pulse	trst	0.2	-	-	ms
Reset hold time	trh	2	-	-	ms

6.3 Panel Setting of Timing

DE Mode	Values			Unit	Remark
	Min.	Typ.	Max.		
THC	48	160	765	tclk	
THD	640	640	640	tclk	
TH	688	800	1405	tclk	1TH=1line
TVC	6	45	255	line	
TVD	480	480	480	line	
TV	486	525	735	line	1TV=1field



7. Commands

REG[01h] Power and Display Control Register (PWRR)

Bit	Description	Default	Access
7	LCD Display Off 0:display off. 1:display on.	0	RW
6-2	NA	0	RO
1	**Sleep Mode** 0:Normal mode. 1:Sleep mode. **Note:** 1.There are 3 ways to wake up from sleep mode: Touch Panel wake up,Key Scan wake up,Software wake up. 2. When using IIC, this function is not supported. 3. When using SPI, it has its particular steps to use this function, refer to section 6-1-2-3 please.	0	RW
0	**Software Reset** 0 : No action. 1 : Software Reset. **Note:**The bit must be set to 1 and then set to 0 to complete a software reset	0	WO

REG[02h] Memory Read/Write Command (MRWC)

Bit	Description	Default	Access
7-0	**Write Function : Memory Write Data** Data to write in memory corresponding to the setting of MWCR1[3:2].Continuous data write cycle can be accepted in bulk data write case. **Read Function : Memory Read Data** Data to read from memory corresponding to the setting of MWCR1[3:2]. Continuous data read cycle can be accepted in bulk data read case. Note that the first data read cycle is dummy read and need to be ignored.	--	RW

REG[04h] Pixel Clock Setting Register (PCSR)

Bit	Description	Default	Access
7	**PCLK Inversion** 0 : PDAT is fetched at PCLK rising edge. 1 : PDAT is fetched at PCLK falling edge.	0	RW
6-2	NA	0	RO
1-0	**PCLK Period Setting** pixel clock (PCLK) period setting. 00b: PCLK period = System Clock period. 01b: PCLK period = 2 times of System Clock period. 10b: PCLK period = 4 times of System Clock period. 11b: PCLK period = 8 times of System Clock period.	0	RW

REG[05h] Serial Flash/ROM Configuration Register (SROC)

Bit	Description	Default	Access
7	**Serial Flash/ROM I/F # Select** 0: Serial Flash/ROM 0 I/F is selected. 1: Serial Flash/ROM 1 I/F is selected.	0	RW
6	**Serial Flash/ROM Address Mode** 0: 24 bits address mode This bit must set to 0 for serial flash .	0	RW
5	**Serial Flash/ROM Waveform Mode** Mode 0. Mode 3.	0	RW
4-3	**Serial Flash /ROM Read Cycle** 00b: 4 bus ➔ no dummy cycle 01b: 5 bus ➔1 byte dummy cycle 1xb: 6 bus ➔2 byte dummy cycle	0	RW
2	**Serial Flash /ROM Access Mode** 0: Font mode 1: DMA mode	0	RW
1-0	**Serial Flash /ROM I/F Data Latch Mode Select** 0xb: Single Mode 10b: Dual Mode 0. 11b: Dual Mode 1.	0	RW

REG[06h] Serial Flash/ROM CLK Setting Register(SFCLR)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**Serial Flash/ROM Clock Frequency Setting** 0xb: SFCL frequency = System clock frequency (When DMA enable and Color depth = 256 color) SFCL frequency = System clock frequency /2) 10b: SFCL frequency = System clock frequency / 2 11b: SFCL frequency = System clock frequency / 4	0	RW

REG[10h] System Configuration Register (SYSR)

Bit	Description	Default	Access
7-4	N/A	0	RO
3-2	**Color Depth Setting** 00b : 8-bpp generic TFT, i.e. 256 colors. 1xb : 16-bpp generic TFT, i.e. 65K colors.	0	RW
1-0	**MCUIF Selection** 00b : 8-bit MCU Interface. 1xb : 16-bit MCU Interface.	0	RW

REG[12h] GPI

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	**GPI[4:0] : General Purpose Input.** KEY_EN = 0: General Purpose Input from pin KIN[4:0] KEY_EN = 1: NC	NA	RO

Note:KEY_EN : REG[C0h] bit 7

REG[13h] GPO

Bit	Description	Default	Access
7-4	NA	0	RO
3-0	**GPO[3:0] : General Purpose Output** KEY_EN = 0: General Purpose Output to KOUT[3:0] KEY_EN = 1: NC	0	RW

Note: KxY_EN : REG[C0h] bit 7

REG[14h] LCD Horizontal Display Width Register (HDWR)

Bit	Description	Default	Access
7	NA	0	RO
6-0	**Horizontal Display Width Setting Bit[6:0]** The register specifies the LCD panel horizontal display width in the unit of 8 pixels resolution. Horizontal display width(pixels) = (HDWR + 1)x8	0	RW

Note : HDWR must be set less than 64h because that the maximum horizontal display width is 800 pixels.

REG[15h] Horizontal Non-Display Period Fine Tuning Option Register (HNDFTR)

Bit	Description	Default	Access
7	**DE Polarity** 0 : high active. 1 : low active.	0	RW
6-4	NA	0	RO
3-0	**Horizontal Non-Display Period Fine Tuning(HNDFT) [3:0]** This register specifies the fine tuning for horizontal non-display period; it is used to support the SYNC mode panel. Each level of this modulation is 2-pixel.	0	RW

REG[16h] LCD Horizontal Non-Display Period Register (HNDR)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	**Horizontal Non-Display Period(HNDP) Bit[4:0]** This register specifies the horizontal non-display period. Horizontal Non-Display Period (pixels) =(HNDR + 1)x8+(HNDFTR/2+1)x2 + 2	0	RW

REG[17h] HSYNC Start Position Register (HSTR)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	**HSYNC Start Position[4:0]** The starting position from the end of display area to the beginning of HSYNC. Each level of this modulation is 8-pixel. HSYNC Start Position(pixels) = (HSTR + 1)x8	0	RW

REG[18h] HSYNC Pulse Width Resister (HPWR)

Bit	Description	Default	Access
7	**HSYNC Polarity** 0 : Low active. 1 : High active.	0	RW
6-5	NA	0	RO
4-0	**HSYNC Pulse Width(HPW) [4:0]** The period width of HSYNC. HSYNC Pulse Width(pixels) = (HPW + 1)x8	0	RW

REG[19h] LCD Vertical Display Height Register (VDHR0)

Bit	Description	Default	Access
7-0	**Vertical Display Height Bit[7:0]** Vertical display Height(Line) = VDHR + 1	0	RW

REG[1Ah] LCD Vertical Display Height Register0 (VDHR1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	**Vertical Display Height bit[8]** Vertical Display Height(Line) = VDHR + 1	0	RW

Note **:** The VDHR must be set less than 1E0h, because the maximum vertical display height is 480.

REG[1Bh] LCD Vertical Non-Display Period Register (VNDR0)

Bit	Description	Default	Access
7-0	**Vertical Non-Display Period Bit[7:0]** Vertical Non-Display Period(Line) = (VNDR + 1)	0	RW

REG[1Ch] LCD Vertical Non-Display Period Register (VNDR1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	**Vertical Non-Display Period bit[8]** Vertical Non-Display Period(Line) = (VNDR + 1)	0	RW

REG[1Dh] VSYNC Start Position Register (VSTR0)

Bit	Description	Default	Access
7-0	**VSYNC Start Position[7:0]** The starting position from the end of display area to the beginning of VSYNC. VSYNC Start Position(Line) = (VSTR + 1)	0	RW

REG[1Eh] VSYNC Start Position Register (VSTR1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	**VSYNC Start Position[8]** The starting from the end of display area to the beginning of VSYNC. VSYNC Start Position(Line) = (VSTR + 1)	0	RW

REG**[1Fh] VSYNC Pulse Width Register (VPWR)**

Bit	Description	Default	Access
7	**VSYNC Polarity** 0 : Low active. 1 : High active.	0	RW
6-0	**VSYNC Pulse Width[6:0]** The pulse width of VSYNC in lines. VSYNC Pulse Width(Line) = (VPWR + 1)	0	RW

REG[20h] Display Configuration Register (DPCR)

Bit	Description	Default	Access
7	**Layer Setting Control** 0 : One layer configuration is selected. 1 : Two layers configuration is selected.	0	RW
6-4	NA	0	RO
3	**HDIR** Horizontal Scan Direction, for n = SEG number. 0 : SEG0 to SEG(n-1). 1 : SEG(n-1) to SEG0.	0	RW
2	**VDIR** Vertical Scan direction, for n = COM number 0 : COM0 to COM(n-1). 1 : COM(n-1) to COM0.	0	RW
1-0	NA	0	RO

REG[21h] Font Control Register 0 (FNCR0)

Bit	Description	Default	Access
7	**CGRAM/CGROM Font Selection Bit in Text Mode** 0 : CGROM font is selected. 1 : CGRAM font is selected. **Note:** 1. The bit is used to select the bit-map source when text-mode is active(REG[40h] bit 7 is 1), when CGRAM is writing(REG[41h] bit 3-2 =01b), the bit must be set as "0". 2. When CGRAM font is select, REG[21h] bit 5 must be set as 1.	0	RW
6	NA	0	RO
5	**External/Internal CGROM Selection Bit** 0 : Internal CGROM is selected.(REG[2Fh] must bx set 00h) 1 : External CGROM is selected. (REG[2Eh] bit6 &bit7 must be set 0)	0	RW
4-2	NA	0	RO
1-0	**Font Selection for internal CGROM** When FNCR0 B7 = 0 and B5 = 0, Internal CGROM supports the 8x16 character sets with the standard coding of ISO/IEC 8859- 1~4, which supports English and most of European country languages. 00b : ISO/IEC 8859-1. 01b : ISO/IEC 8859-2. 10b : ISO/IEC 8859-3. 11b : ISO/IEC 8859-4.	0	RW

REG[22h] Font Control Register1 (FNCR1)

Bit	Description	Default	Access
7	**Full Alignment Selection Bit** 0 : Full alignment is disable. 1 : Full alignment is enable.	0	RW
6	**Font Transparency** 0 : Font with background color. 1 : Font with background transparency.	0	RW
5	NA	0	RO
4	**Font Rotation** 0 : Normal. 1 : 90 degree display.	0	RW
3-2	**Horizontal Font Enlargement** 00b : X1. 01b : X2. 10b : X3. 11b : X4.	0	RW
1-0	**Vertical Font Enlargement** 00b : X1. 01b : X2. 10b : X3. 11b : X4.	0	RW

REG[23h] CGRAM Select Register (CGSR)

Bit	Description	Default	Access
7-0	**CGRAM No.** The setting of the number of the character in CGRAM. It's used to write the user-defined character bitmap data into CGRAM. 16 continuous data write cycles compete the bitmap writing of a 8x16 character. Note that the MWCR1 bit 3-2 must be set as 01b(CGRAM) first. And more than 16 data write cycles will loop back to the 1st data and cover the bitmap.	0	RW

REG[24h] Horizontal Scroll Offset Register 0 (HOFS0)

Bit	Description	Default	Access
7-0	**Horizontal Display Scroll Offset [7:0]** The display offset of the horizontal direction, changing the value will cause the effect of scrolling at horizontal direction.	0	RW

REG[25h] Horizontal Scroll Offset Register 1 (HOFS1)

Bit	Description	Default	Access
7-3	NA	0	RO
2-0	**Horizontal Display Scroll Offset [10:8]** The display offset of the horizontal direction, changing the value will cause the effect of scrolling at horizontal direction.	0	RW

REG[26h] Vertical Scroll Offset Register 0 (VOFS0)

Bit	Description	Default	Access
7-0	**Vertical Display Scroll Offset [7:0]** The display offset of the vertical direction, changing the value will cause the effect of scrolling at vertical direction.	0	RW

REG[27h] Vertical Scroll Offset Register 1 (VOFS1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**Vertical Display Scroll Offset [9:8]** The display offset of the vertical direction, changing the value will cause the effect of scrolling at vertical direction.	0	RW

REG[29h] Font Line Distance Setting Register (FLDR)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	**Font Line Distance Setting** Setting the font character line distance when setting memory font write cursor auto move. (Unit: pixel)	0	RW

REG[2Ah] Font Write Cursor Horizontal Position Register 0 (F_CURXL)

Bit	Description	Default	Access
7-0	**Font Write Cursor Horizontal Position[7:0]** The setting of the horizontal cursor position for font writing.	0	RW

REG[2Bh] Font Write Cursor Horizontal Position Register 1 (F_CURXH)

Bit	Description	Default	Access
7-2	**NA**	0	RO
1-0	**Font Write Cursor Horizontal Position[9:8]** The setting of the horizontal cursor position for font writing.	0	RW

REG[2Ch] Font Write Cursor Vertical Position Register 0 (F_CURYL)

Bit	Description	Default	Access
7-0	**Font Write Cursor Vertical Position[7:0]** The setting of the vertical cursor position for font writing.	0	RW

REG[2Dh] Font Write Cursor Vertical Position Register 1 (F_CURYH)

Bit	Description	Default	Access
7-1	**NA**	0	RO
0	**Font Write Cursor Vertical Position[8]** The setting of the vertical cursor position for font writing.	0	RW

REG[2Eh] Font Write Type Setting Resister

<table>
<tr><th>Bit</th><th>Description</th><th>Default</th><th>Access</th></tr>
<tr><td>7-6</td><td>Font Size Setting(* 1)
<table>
<tr><th></th><th>Full Size</th><th>Half-Size</th><th>Variable Width</th></tr>
<tr><td>00b</td><td>16x16</td><td>8x16</td><td>NX16</td></tr>
<tr><td>01b</td><td>24x24</td><td>12x24</td><td>NX24</td></tr>
<tr><td>1Xb(* 2)</td><td>32x32</td><td>16x32</td><td>NX32</td></tr>
</table>
Note:
* 1The font width indicated by “N” depends on the character code of the FONT.
* 2 The command is invalid , GT30L24T3Y does not support size of 32x32 .</td><td>0</td><td>RW</td></tr>
<tr><td>5-0</td><td>Font to Font Width Setting
00h : Font width off
01h : Font to Font width = 1 pixel
02h : Font to Font width = 2 pixels
:
3Fh : Font to Font width = 63 pixels</td><td>0</td><td>RW</td></tr>
</table>

REG[2Fh] Serial Font ROM Setting

<table>
<tr><th>Bit</th><th>Description</th><th>Default</th><th>Access</th></tr>
<tr><td>7-5</td><td>GT Serial Font ROM Select
000b: GT21L16TW / GT21H16T1W
001b: GT30L16U2W
010b: GT30L24T3Y / GT30H24T3Y
011b: GT30L24M1Z
100b: GT30L32S4W / GT30H32S4W</td><td>0</td><td>RW</td></tr>
<tr><td>4-2</td><td>FONT ROM Coding Setting
For specific GT serial Font ROM, the coding method must be set for decoding.
000b: GB2312
001b: GB12345/GB18030
010b: BIG5
011b: UNICODE
100b: ASCII
101b: UNI-Japanese
110b: JIS0208
111b: Latin/Greek/ Cyrillic / Arabic</td><td>0</td><td>RW</td></tr>
<tr><td>1-0</td><td>ASCII / Latin/Greek/ Cyrillic / Arabic Latin
<table>
<tr><th></th><th>ASCII</th><th>Latin/Greek/ Cyrillic</th><th>Arabic Latin</th></tr>
<tr><td>00b</td><td>Normal</td><td>Normal</td><td>NA</td></tr>
<tr><td>01b</td><td>Arial</td><td>Variable Width</td><td>Presentation forms-A</td></tr>
<tr><td>10b</td><td>Roman</td><td>NA</td><td>Forms-B</td></tr>
<tr><td>11b</td><td>Bold</td><td>NA</td><td>NA</td></tr>
</table></td><td>0</td><td>RW</td></tr>
</table>

REG[30h] Horizontal Start Point 0 of Active Window (HSAW0)

Bit	Description	Default	Access
7-0	**Horizontal Start Print of active Window [7:0]**	0	RW

REG[31h] Horizontal Start Point 1 of active Window (HSAW1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**Horizontal Start Point of Active Window [9:8]**	0	RW

REG[32h] Vertical Start Point 0 of Active Window (VSAW0)

Bit	Description	Default	Access
7-0	**Vertical Start Point of Active Window [7:0]**	0	RW

REG[33h] Vertical Start Point 1 of Active Window (VSAW1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	**Vertical Start Point of Active Window [8]**	0	RW

REG[34h] Horizontal End Point 0 of Active Window (HEAW0)

Bit	Description	Default	Access
7-0	**Horizontal End Point of Active Window [7:0]**	0	RW

REG[35h] Horizontal End Point 1 of Active Window (HEAW1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**Horizontal End Point of Active Window [9:8]**	0	RW

REG[36h] Vertical End Point of Active Window 0 (VEAW0)

Bit	Description	Default	Access
7-0	**Vertical End Point of Active Window [7:0]**	0	RW

REG[37h] Vertical End Point of Active Window 1 (VEAW1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	**Vertical End Point of Active Window [8]**	0	RW

REG[38h] Horizontal Start Point 0 of Scroll Window (HSSW0)

Bit	Description	Default	Access
7-0	**Horizontal Start Point of Scroll Window [7:0]**	0	RW

REG[39h] Horizontal Start Point 1 of Scroll Window (HSSW1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**Horizontal Start Point of Scroll Window [9:8]**	0	RW

REG[3Ah] Vertical Start Point 0 of Scroll Window (VSSW0)

Bit	Description	Default	Access
7-0	**Vertical Start Point of Scroll Window [7:0]**	0	RW

REG[3Bh] Vertical Start Point 1 of Scroll Window (VSSW1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	**Vertical Start Point of Scroll Window [8]**	0	RW

REG[3Ch] Horizontal End Point 0 of Scroll Window (HESW0)

Bit	Description	Default	Access
7-0	**Horizontal End Point of Scroll Window [7:0]**	0	RW

REG[3Dh] Horizontal End Point 1 of Scroll Window (HESW1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**Horizontal End Point of Scroll Window [9:8]**	0	RW

REG[3Eh] Vertical End Point 0 of Scroll Window (VESW0)

Bit	Description	Default	Access
7-0	**Vertical End Point of Scroll Window [7:0]**	0	RW

REG[3Fh] Vertical End Point 1 of Scroll Window (VESW1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	**Vertical End Point of Scroll Window [8]**	0	RW

REG[40h] Memory Write Control Register 0 (MWCR0)

Bit	Description	Default	Access
7	**Text Mode enable** 0 : Graphic mode. 1 : Text mode.	0	RW
6	**Font Write Cursor/ Memory Write Cursor Enable** 0 : Font write cursor/ Memory Write Cursor is not visible. 1 : Font write cursor/ Memory Write Cursor is visible.	0	RW
5	**Font Write Cursor/ Memory Write Cursor Blink Enable** 0 : Normal display. 1 : Blink display.	0	RW
4	**NA**	0	RO
3-2	**Memory Write Direction (Only for Graphic Mode)** 00b : Left → Right then Top → Down. 01b : Right → Left then Top → Down. 10b : Top → Down then Left → Right. 11b : Down → Top then Left → Right.	0	RW
1	**Memory Write Cursor Auto-Increase Disable** 0 : Cursor auto-increases when memory write. 1 : Cursor doesn't auto-increases when memory write.	0	RW
0	**Memory Read Cursor Auto-Increase Disable** 0 : Cursor auto-increases when memory read. 1 : Cursor doesn't auto-increases when memory read.	0	RW

REG[41h] Memory Write Control Register 1 (MWCR1)

Bit	Description	Default	Access
7	**Graphic Cursor Enable** 0 : Graphic Cursor disable. 1 : Graphic Cursor enable.	0	RW
6-4	**Graphic Cursor Selection Bit** Select one from eight graphic cursor types.(000b to 111b) 000b : Graphic Cursor Set 1. 001b : Graphic Cursor Set 2. 010b : Graphic Cursor Set 3. : : 111b : Graphic Cursor Set 8.	0	RW
3-2	**Write Destination Selection** 00b : Layer 1~2. 01b : CGRAM. 10b : Graphic Cursor. 11b : Pattern. **Note** *:* When CGRAM is selected (01b), REG[21h] bit 7 must be set as "0".	0	RW
1	**NA**	0	RO
0	**Layer No. for Read/Write Selection** **When resolution =< 480x400 or color depth = 8bpp:** 0 : Layer 1. 1 : Layer 2. **When resolution > 480x400 and color depth > 8bpp:** NA, always writing to Layer 1.	0	RW

REG[44h] Blink Time Control Register (BTCR)

Bit	Description	Default	Access
7-0	**Text Blink Time Setting (Unit: Frame)** 00h : 1 frame time. 01h : 2 frames time. 02h : 3 frames time. : : : FFh : 256 frames time.	0	RW

REG[45h] Memory Read Cursor Direction (MRCD)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**Memory Read Direction (Only for Graphic Mode)** 00b : Left → Right then Top → Down. 01b : Right → Left then Top → Down. 10b : Top → Down then Left → Right. 11b : Down → Top then Left → Right.	0	RW

REG[46h] Memory Write Cursor Horizontal Position Register 0 (CURH0)

Bit	Description	Default	Access
7-0	**Memory Write Cursor Horizontal Location[7:0]**	0	RW

REG[47h] Memory Write Cursor Horizontal Position Register 1 (CURH1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**Memory Write Cursor Horizontal Location[9:8]**	0	RW

REG[48h] Memory Write Cursor Vertical Position Register 0 (CURV0)

Bit	Description	Default	Access
7-0	**Memory Write Cursor Vertical Location[7:0]**	0	RW

REG[49h] Memory Write Cursor Vertical Position Register 1 (CURV1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	**Memory Write Cursor Vertical Location[8]**	0	RW

REG[4Ah] Memory Read Cursor Horizontal Position Register 0 (RCURH0)

Bit	Description	Default	Access
7-0	**Memory Read Cursor Horizontal Location[7:0]**	0	RW

REG[4Bh] Memory Read Cursor Horizontal Position Register 1 (RCURH01)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**Memory Read Cursor Horizontal Location[9:8]**	0	RW

REG[4Ch] Memory Read Cursor Vertical Position Register 0 (RCURV0)

Bit	Description	Default	Access
7-0	**Memory Read Cursor Vertical Location[7:0]**	0	RW

REG[4Dh] Memory Read Cursor Vertical Position Register 1 (RCURV1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	**Memory Read Cursor Vertical Location[8]**	0	RW

REG[4Eh] Font Write Cursor and Memory Write Cursor Horizontal Size Register (CURHS)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	**Font Write Cursor Horizontal Size Setting[4:0]** Unit : Pixel **Note** *:* When font is enlarged, the cursor setting will multiply the same times as the font enlargement.	7h	RW

REG[4Fh] Font Write Cursor Vertical Size Register (CURVS)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	**Font Write Cursor Vertical Size Setting[4:0]** Unit : Pixel **Note** *:* When font is enlarged, the cursor setting will multiply the same times as the font enlargement.	0	RW

REG[50h] BTE Function Control Register 0 (BECR0)

Bit	Description	Default	Access
7	**BTE Function Enable / Status** **Write** 0 : No action. 1 : BTE function enable. **Read** 0 : BTE function is idle. 1 : BTE function is busy.	0	RW
6	**BTE Source Data Select** 0 : Block mode,the Source BTE is stored as a rectangular region of memory. 1 : Linear mode, the Source BTE is stored as a continuous block of memory.	0	RW
5	**BTE Destination Data Type Select** 0 : Block mode, the Destination BTE is stored as a rectangular region of memory. 1 : Linear mode, the Destination BTE is stored as a continuous block of memory.	0	RW
4-0	NA	0	RO

REG[51h] BTE Function Control Register1 (BECR1)

Bit	Description	Default	Access
7-5	**BTE ROP Code Bit[3:0]** ROP is the acronym for Raster Operation. Some of BTE operation code has to collocate with ROP for the detailed function. (Please refer to the Section 7-6)	0	RW
4-0	**BTE Operation Code Bit[3:0]** RA8875 includes a 2D BTE Engine, it can execute 13 BTE functions, the operation code range is from 1100b to 0000b and 1111b to 1101b are not used. Some of BTE Operation Code has to collocate with the ROP code for the advance function. (Please refer to the Section 7-6)	0	RW

REG[68h] Background Color Register for Transparent 1 (BGTR1)

Bit	Description	Default	Access
7-6	**NA**	0	RO
5-0	**Foreground Color Green[5:0]** If REG[10h] Bit[3:2] is set to 256 colors, the register only uses Bit[2:0]. If REG[10h] Bit[3:2] is set to 65K colors, the register uses Bit[5:0].	0	RW

REG[69h] Background Color Register for Transparent 2 (BGTR2)

Bit	Description	Default	Access
7-5	**NA**	0	RO
4-0	**Foreground Color Blue[4:0]** If REG[10h] Bit[3:2] is set to 256 colors, the register only uses Bit[1:0]. If REG[10h] Bit[3:2] is set to 65K colors, the register uses Bit[4:0].	0	RW

REG[70h] Touch Panel Control Register 0 (TPCR0)

Bit	Description	Default	Access
7	**Touch Panel Enable Bit** 0 : Disable 1 : Enable	0	RW
6-4	**TP Sample Time Adjusting** 000b : Wait 512 system clocks period for ADC data ready. 001b : Wait 1024 system clocks period for ADC data ready. 010b : Wait 2048 system clocks period for ADC data ready. 011b : Wait 4096 system clocks period for ADC data ready. 100b : Wait 8192 system clocks period for ADC data ready. 101b : Wait 16384 system clocks period for ADC data ready. 110b : Wait 32768 system clocks period for ADC data ready. 111b : Wait 65536 system clocks period for ADC data ready.	0	RW
3	**Touch Panel Wakeup Enable** 0 : Disable the Touch Panel wake-up function. 1 : Touch Panel can wake-up the sleep mode.	0	RW
2-0	**ADC Clock Setting** 000b : System CLK 001b : (System CLK) / 2. 010b : (System CLK) x 4. 011b : (System CLK) / 8. 100b : (System CLK) x 16. 101b : (System CLK) / 32. 110b : (System CLK) / x64. 111b : (System CLK) / 128.	0	RW

REG[71h] Touch Panel Control Register 1 (TPCR1)

Bit	Description	Default	Access
7	N/A	0	RO
6	**TP Manual Mode Enable** 0 : Auto mode. 1 : Using the manual mode.	0	RW
5	**TP ADC Reference Voltage Source** 0 : Vref generated from internal circuit. No external voltage is needed. 1 : Vref from external source, 1/2 VDD is needed for ADC.	0	RW
4-3	NA	0	RO
2	**De-bounce Circuit Enable for Touch Panel Interrupt** 0: De-bounce circuit disable. 1: De-bounce circuit enable.	0	RW
1-0	**Mode Selection for TP Manual Mode** 00b : IDLE mode: Touch Panel in idle mode. 01b : Wait for TP event, Touch Panel event could cause the interrupt or be read from REG[F1h] Bit2. 10b : Latch X data, in the phase, X Data can be latched in REG[72h] and REG[74h]. 11b : Latch Y data, in the phase, Y Data can be latched in REG[73h] and REG[74h].	0	RW

REG[72h] Touch Panel X High Byte Data Register (TPXH)

Bit	Description	Default	Access
7-0	Touch Panel X Data Bit[9:2]	0	RW

REG[73h] Touch Panel Y High Byte Data Register (TPYH)

Bit	Description	Default	Access
7-0	**Touch Panel Y Data Bit[9:2]**	0	RW

REG[74h] Touch Panel X/Y Low Byte Data Register (TPXYL)

Bit	Description	Default	Access
7	ADET **Touch Event Detector** 0 : Touch Panel is touched. 1 : Touch Panel is not touched.	1	RO
6-4	NA	0	RO
3-2	**Touch Panel Y Data Bit[1:0]**	0	RW
1-0	**Touch Panel X Data Bit[1:0]**	0	RW

REG[80h] Graphic Cursor Horizontal Position Register 0 (GCHP0)

Bit	Description	Default	Access
7-0	**Graphic Cursor Horizontal Location[7:0]**	0	RW

REG[81h] Graphic Cursor Horizontal Position Register 1 (GCHP1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**Graphic Cursor Horizontal Location[9:8]**	0	RW

REG[82h] Graphic Cursor Vertical Position Register 0 (GCVP0)

Bit	Description	Default	Access
7-0	**Graphic Cursor Vertical Location[7:0]**	0	RW

REG[83h] Graphic Cursor Vertical Position Register 1 (GCVP1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	**Graphic Cursor Vertical Location[8]**	0	RW

REG[84h] Graphic Cursor Color 0 (GCC0)

Bit	Description	Default	Access
7-0	**Graphic Cursor Color 0 with 256 colors** RGB Format [7:0] = RRRGGGBB.	0	RW

REG[85h] Graphic Cursor Color 1 (GCC1)

Bit	Description	Default	Access
7-0	**Graphic Cursor Color 1 with 256 Colors** RGB Format [7:0] = RRRGGGBB.	0	RW

REG[88h] PLL Control Register 1 (PLLC1)

Bit	Description	Default	Access
7	**PLLDIVM** PLL Pre-driver parameter. 0 : divided by 1. 1 : divided by 2.	0	RW
6-5	NA	0	RO
4-0	**PLLDIVN[4:0]** PLL input parameter, the value should be 1~31. (i.e. value 0 is forbidden).	0	RW

REG[89h] PLL Control Register 2 (PLLC2)

Bit	Description	Default	Access
7-3	NA	0	RO
2-0	**PLLDIVK[2:0]** PLL Output divider 000b : divided by 1. 001b : divided by 2. 010b : divided by 4. 011b : divided by 8. 100b : divided by 16. 101b : divided by 32. 110b : divided by 64. 111b : divided by 128.	03h	RW

REG[8Ah] PWM1 Control Register (P1CR)

Bit	Description	Default	Access
7	**PWM1 Enable** 0 : Disable, PWM1_OUT level depends on P1CR bit6. 1 : Enable.	0	RW
6	**PWM1 Disable Level** 0 : PWM1_OUT is Normal L when PWM disable or Sleep mode. 1 : PWM1_OUT is Normal H when PWM disable or Sleep mode. The bit is only usable when P1CR bit 4 is 0	0	RW
5	Reserved	0	RO
4	**PWM1 Function Selection** 0 : PWM1 function. 1 : PWM1 output a fixed frequency signal and it is equal to 1 /16 oscillator clock. PWM1 = FOSC / 16(**Note**)	0	RW
3-0	**PWM1 Clock Source Divide Ratio** 0000b : SYS_CLK / 1 | 1000b : SYS_CLK / 256 0001b : SYS_CLK / 2 | 1001b : SYS_CLK / 512 0010b : SYS_CLK / 4 | 1010b : SYS_CLK / 1024 0011b : SYS_CLK / 8 | 1011b : SYS_CLK / 2048 0100b : SYS_CLK / 16 | 1100b : SYS_CLK / 4096 0101b : SYS_CLK / 32 | 1101b : SYS_CLK / 8192 0110b : SYS_CLK / 64 | 1110b : SYS_CLK / 16384 0111b : SYS_CLK / 128 | 1111b : SYS_CLK / 32768 For example, if the system clock is 20MHz and Bit[3:0] =0001b, when the clock source of PWM1 is 10MHz.	0	RW

Note : FOSC is the frequency of external oscillator.

REG[8Bh] PWM1 Duty cycle Register (P1DCR)

Bit	Description	Default	Access
7-0	**PWM Cycle Duty Selection Bit** 00h → 1 / 256 Duty with PWM1 clock source. 01h → 2 / 256 Duty with PWM1 clock source. 02h → 3 / 256 Duty with PWM1 clock source. : : FEh → 255 / 256 Duty with PWM1 clock source. FFh → 256 / 256 Duty with PWM1 clock source.	0	RW

REG[8Ch] PWM2 Control Register (P2CR)

Bit	Description	Default	Access
7	**PWM2 Enable** 0 : Disable, PWM_OUT level depends on P2CR bit6. 1 : Enable.	0	RW
6	**PWM2 Disable Level** 0 : PWM2_OUT is Normal L when PWM disable or Sleep mode. 1 : PWM2_OUT is Normal H when PWM disable or Sleep mode. The bit is only usable when P2CR bit 4 is 0	0	RW
5	Reserved	0	RO
4	**PWM2 Function Selection** 0 : PWM2 function. 1 : PWM2 output a signal which is the same with system clock. PWM2 = SYS_CLK / 16 .	0	RW
3-0	**PWM2 Clock Source Divide Ratio** 0000b : SYS_CLK / 1 | 1000b : SYS_CLK / 256 0001b : SYS_CLK / 2 | 1001b : SYS_CLK / 512 0010b : SYS_CLK / 4 | 1010b : SYS_CLK / 1024 0011b : SYS_CLK / 8 | 1011b : SYS_CLK / 2048 0100b : SYS_CLK / 16 | 1100b : SYS_CLK / 4096 0101b : SYS_CLK / 32 | 1101b : SYS_CLK / 8192 0110b : SYS_CLK / 64 | 1110b : SYS_CLK / 16384 0111b : SYS_CLK / 128 | 1111b : SYS_CLK / 32768 For example, if the system clock is 20MHz and Bit[3:0] =0010b,then the clock source of PWM2 is 5MHz.	0	RW

REG[8Dh] PWM2 Control Register (P2DCR)

Bit	Description	Default	Access
7-0	**PWM Cycle Duty Selection Bit** 00h → 1 / 256 Duty with PWM2 clock source. 01h → 2 / 256 Duty with PWM2 clock source. 02h → 3 / 256 Duty with PWM2 clock source. : : FEh → 255 / 256 Duty with PWM2 clock source. FFh → 256 / 256 Duty with PWM2 clock source.	0	RW

REG[8Eh] Memory Clear Control Register (MCLR)

Bit	Description	Default	Access
7	**Memory Clear Function** 0 : End or Stop. When write 0 to this bit RA8875 will stop the Memory clear function. Or if read back this bit is 0, it indicates than Memory clear function is complete. 1 : Start the memory clear function.	0	RW
6	**Memory Clear Area Setting** 0 : Clear the full window. (Please refer to the setting of REG[14h], [19h], [1Ah]) 1 : Clear the active window(Please refer to the setting of REG[30h~37h]). The layer to be cleared is according to the setting REG[41h] Bit0.	0	RW
5-0	NA	0	RO

REG[90h] Draw Line/Circle/Square Control Register (DCR)

Bit	Description	Default	Access
7	**Draw Line/Square/Triangle Start Signal** **Write Function** 0 : Stop the drawing function. 1 : Start the drawing function. **Read Function** 0 : Drawing function complete. 1 : Drawing function is processing.	0	RW
6	**Draw Circle Start Signal** **Write Function** 0 : Stop the circle drawing function. 1 : Start the circle drawing function. **Read Function** 0 : Circle drawing function complete. 1 : Circle drawing function is processing.	0	RW
5	**Fill the Circle/Square/Triangle Signal** 0 : Non fill. 1 : Fill.	0	RW
4	**Draw Line or Square Select Signal** 0 : Draw line. 1 : Draw square.	0	RW
3-1	NA	0	RO
0	**Draw Triangle or Line/Square Select Signal** 0 : Draw Line or square 1 : Draw Triangle	0	RW

REG[91h] Draw Line/square Horizontal Start Address Register0 (DLHSR0)

Bit	Description	Default	Access
7-0	**Draw Line/Square Horizontal Start Address[7:0]**	0	RW

REG[92h] Draw Line/Square Horizontal Start Address Register1 (DLHSR1)

Bit	Description	Default	Access
7-2	**NA**	0	RO
1-0	**Draw Line/Square Horizontal Start Address[9:8]**	0	RW

REG[93h] Draw Line/Square Vertical Start Address Register0 (DLVSR0)

Bit	Description	Default	Access
7-0	**Draw Line/Square Vertical Start Address[7:0]**	0	RW

REG[94h] Draw Line/Square Vertical Start Address Register1 (DLVSR1)

Bit	Description	Default	Access
7-1	**NA**	0	RO
0	**Draw Line/square Vertical Start Address[8]**	0	RW

Note: start point and end point cannot equal.

REG[95h] Draw Line/Square Horizontal End Address Register0 (DLHER0)

Bit	Description	Default	Access
7-0	**Draw Line/Square Horizontal End Address[7:0]**	0	RW

REG[96h] Draw Line/Square Horizontal End Address Register1 (DLHER1)

Bit	Description	Default	Access
7-2	**NA**	0	RO
1-0	**Draw Line/Square Horizontal End Address[9:8]**	0	RW

REG[97h] Draw Line/Square Vertical End Address Register0 (DLVER0)

Bit	Description	Default	Access
7-0	**Draw Line/Square Vertical End Address[7:0]**	0	RW

REG[98h] Draw Line/Square Vertical End Address Register1 (DLVER1)

Bit	Description	Default	Access
7-1	**NA**	0	RO
0	**Draw Line/Square Vertical End Address[8]**	0	RW

Note: start point and end point cannot equal.

REG[99h] Draw Circle Center Horizontal Address Register0 (DCHR0)

Bit	Description	Default	Access
7-0	**Draw Circle Center Horizontal Address[7:0]**	0	RW

REG[9Ah] Draw Circle Center Horizontal Address Register1 (DCHR1)

Bit	Description	Default	Access
7-2	**NA**	0	RO
1-0	**Draw Circle Center Horizontal Address[9:8]**	0	RW

REG[9Bh] Draw Circle Center Vertical Address Register0 (DCVR0)

Bit	Description	Default	Access
7-0	**Draw Circle Center Vertical Address[7:0]**	0	RW

REG[9Ch] Draw Circle Center Vertical Address Register1 (DCVR1)

Bit	Description	Default	Access
7-1	**NA**	0	RO
0	**Draw Circle Center Vertical Address[8]**	0	RW

REG[9Dh] Draw Circle Radius Register (DCRR)

Bit	Description	Default	Access
7-0	**Draw Circle Radius[7:0]**	0	RW

REG[A0h] Draw Ellipse/Ellipse Curve/Circle Square Control Register

Bit	Description	Default	Access
7	**Draw Ellipse/Circle Square start Signal** **Write Function** 0 : Stop the drawing function. 1 : Start the drawing function. **Read Function** 0 : Drawing function complete. 1 : Drawing function is processing.	0	RW
6	**Fill the Ellipse/Circle Square Signal** 0 : Non fill. 1 : fill.	0	RW
5	**Draw Ellipse/ Ellipse Curve or Circle Square Select Signal** 0 : Draw Ellipse/ Ellipse curve.(Depend on bit4) 1 : Draw Circle Square.	0	RW
4	**Draw Ellipse or Ellipse Curve Select Signal** 0 : Draw Ellipse 1 : Draw Ellipse Curve	0	RW
3-2	**NA**	0	RO
1-0	**Draw Ellipse Curve Part Select(DECP)**	0	RW

REG[A1h] Draw Ellipse/Circle Square Long axis Setting Register (ELL_A0)

Bit	Description	Default	Access
7-0	**Draw Ellipse/Circle Square Long axis[7:0]**	0	RW

REG[A2h] Draw Ellipse/Circle Square Long axis Setting Register (ELL_A1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**Draw Ellipse/Circle Square Long axis[9:8]**	0	RW

REG[A3h] Draw Ellipse/Circle Square Short axis Setting Register (ELL_B0)

Bit	Description	Default	Access
7-0	**Draw Ellipse/Circle Square Short axis[7:0]**	0	RW

REG[A4h] Draw Ellipse/Circle Square Short axis Setting Register (ELL_B1)

Bit	Description	Default	Access
7-1	**NA**	0	RO
0	**Draw Ellipse/Circle Square Short axis[8]**	0	RW

REG[A5h] Draw Ellipse/Circle Square Center Horizontal Address Register0 (DEHR0)

Bit	Description	Default	Access
7-0	**Draw Ellipse/Circle Square Center Horizontal Address[7:0]**	0	RW

REG[A6h] Draw Ellipse/Circle Square Center Horizontal Address Register1 (DEHR1)

Bit	Description	Default	Access
7-2	**NA**	0	RO
1-0	**Draw Ellipse/Circle Square Center Horizontal Address[9:8]**	0	RW

REG[A7h] Draw Ellipse/Circle Square Center Vertical Address Register0 (DEVR0)

Bit	Description	Default	Access
7-0	**Draw Ellipse/Circle Square Center Vertical Address[7:0]**	0	RW

REG[A8h] Draw Ellipse/Circle Square Center Vertical Address Register1 (DEVR1)

Bit	Description	Default	Access
7-1	**NA**	0	RO
0	**Draw Ellipse/Circle Square Center Vertical Address[8]**	0	RW

REG[A9h] Draw Triangle Point 2 Horizontal Address Register0 (DTPH0)

Bit	Description	Default	Access
7-0	**Draw Triangle Point 2 Horizontal Address[7:0]**	0	RW

REG[AAh] Draw Triangle Point 2 Horizontal Address Register1 (DTPH1)

Bit	Description	Default	Access
7-2	**NA**	0	RO
1-0	**Draw Triangle Point 2 Horizontal Address[9:8]**	0	RW

REG[ABh] Draw Triangle Point 2 Vertical Address Register0 (DTPV0)

Bit	Description	Default	Access
7-0	**Draw Triangle Point 2 Vertical Address [7:0]**	0	RW

REG[ACh] Draw Triangle Point 2 Vertical Address Register1 (DTPV1)

Bit	Description	Default	Access
7-1	**NA**	0	RO
0	**Draw Triangle Point 2 Vertical Address [8]**	0	RW

REG[B0h] Source Starting Address REG0 (SSAR0)

Bit	Description	Default	Access
7-0	**DMA Source START ADDRESS [7:0]**	0	RW

REG[B1h] Source Starting Address REG 1 (SSAR1)

Bit	Description	Default	Access
7-0	**DMA Source START ADDRESS [15:8]**	0	RW

REG[B2h] Source Starting Address REG 2 (SSAR2)

Bit	Description	Default	Access
7-0	**DMA Source START ADDRESS [23:16]**	0	RW

REG[B4h] Block Width REG 0(BWR0) / DMA Transfer Number REG 0 (DTNR0)

Bit	Description	Default	Access
7-0	**When REG[BFh] bit 1 = 0 (Continuous Mode)** DMA Transfer Number [7:0] **When REG[BFh] bit 1 = 1 (Block Mode)** DMA Block Width [7:0]	0	RW

REG[B5h] Block Width REG 1 (BWR1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**DMA Block Width [9:8]**	0	RW

REG[B6h] Block Height REG 0(BHR0) /DMA Transfer Number REG 1 (DTNR1)

Bit	Description	Default	Access
7-0	**When REG[BFh] bit 1 = 0 (Continuous Mode)** DMA Transfer Number [15:8] **When REG[BFh] bit 1 = 1 (Block Mode)** DMA Block Height [7:0]	0	RW

REG[B7h] Block Height REG 1 (BHR1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**DMA Block Height [9:8]**	0	RW

REG[B8h] Source Picture Width REG 0(SPWR0) / DMA Transfer Number REG 2(DTNR2)

Bit	Description	Default	Access
7-3	**DMA Source Picture Width [7:3]**	0	RW
2-0	**When REG[BFh] bit 1 =** 0 **(Continuous Mode)** DMA Transfer Number [18:16] **When REG[BFh] bit 1 =** 1 **(Block Mode)** DMA Source Picture Width [2:0]	0	RW

REG[B9h] Source Picture Width REG 1 (SPWR1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	DMA Source Picture Width [9:8]	0	RW

REG[BFh] DMA Configuration REG (DMACR)

Bit	Description	Default	Access
7-2	**NA**	0	RO
1	**DMA Continuous or Block Read/Write Select Bit** 0: Continuous / 1: Block	0	RW
0	**Write Function➔ DMA Start Bit** Set to 1 by MCU and reset to 0 automatically **Read Function➔ DMA Busy Check Bit** 0:Idle / 1:Busy	0	RW

Registers REG [D0h] Floating Windows Start Address XA 0 (FWSAXA0)

Bit	Description	Default	Access
7-0	**Floating Windows Start Address XA [7:0]**	0	RW

REG [D1h] Floating Windows Start Address XA 1 (FWSAXA1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**Floating Windows Start Address XA [9:8]**	0	RW

REG [D2h] Floating Windows Start Address YA 0 (FWSAYA0)

Bit	Description	Default	Access
7-0	**Floating Windows Start Address YA [7:0]**	0	RW

REG [D3h] Floating Windows Start Address YA 1 (FWSAYA1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	**Floating Windows Start Address YA [8]**	0	RW

REG [D4h] Floating Windows Width 0 (FWW0)

Bit	Description	Default	Access
7-0	**Floating Windows Width Setting [7:0]**	0	RW

REG [D5h] Floating Windows Width 1 (FWW1)

Bit	Description	Default	Access
7-2	**NA**	0	RO
1-0	**Floating Windows Width Setting [9:8]**	0	RW

REG [D6h] Floating Windows Height 0 (FWH0)

Bit	Description	Default	Access
7-0	**Floating Windows Height Setting[7:0]**	0	RW

REG [D7h] Floating Windows Height 1 (FWH1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**Floating Windows Height Setting [9:8]**	0	RW

REG [D8h] Floating Windows Display X Address 0 (FWDXA0)

Bit	Description	Default	Access
7-0	**Floating Windows Display X Address [7:0]**	0	RW

REG [D9h] Floating Windows Display X Address 1 (FWDXA1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	**Floating Windows Display X Address [9:8]**	0	RW

REG [DAh] Floating Windows Display Y Address 0 (FWDYA0)

Bit	Description	Default	Access
7-0	**Floating Windows Display X Address [7:0]**	0	RW

REG [DBh] Floating Windows Display Y Address 1 (FWDYA1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	**Floating Windows Display Y Address [8]**	0	RW

SACS_MODE REG [E0h] Serial Flash/ROM Direct Access Mode

Bit	Description	Default	Access
7-1	NA	0	RO
0	0: direct access mode disable, then user can use for FONT/DMA mode. 1: direct access mode enable, then FONT/DMA mode disable	0	RW

SACS_ADDR REG [E1h] Serial Flash/ROM Direct Access Mode Address

Bit	Description	Default	Access
7-0	Direct access mode Address Serial Flash/ROM have 24 bit address data, user must be write 3 times E1 for address setting.	0	WO

SACS_DATA [E2h] Serial Flash/ROM Direct Access Data Read

Bit	Description	Default	Access
7-0	Direct access mode Read Data buffer	0	RO

REG[F0h] Interrupt Control Register1 (INTC1)

Bit	Description	Default	Access
7-5	NA	0	RO
4	**KEYSCAN Interrupt Enable Bit** 0 : Disable KEYSCAN interrupt. 1 : Enable KEYSCAN interrupt.	0	RW
3	**DMA Interrupt Enable Bit** 0 : Disable DMA interrupt. 1 : Enable DMA interrupt.	0	RW
2	**Touch Panel Interrupt Enable Bit** 0 : Disable Touch interrupt. 1 : Enable Touch interrupt.	0	RW
1	**BTE Process complete Interrupt Enable Bit** 0 : Disable BTE process complete interrupt. 1 : Enable BTE process complete interrupt.	0	RW
0	**When MCU-relative BTE operation is selected(*1) and BTE Function is Enabled(REG[50h] Bit7 = 1), this bit is used to Enable the BTE Interrupt for MCU R/W:** 0 : Disable BTE interrupt for MCU R/W. 1 : Enable BTE interrupt for MCU R/W. **When the BTE Function is disabled, this bit is used to Enable the Interrupt of Font Write Function:** 0 : Disable font write interrupt. 1 : Enable font write interrupt.	0	RW

Note : 1. MCU-relative BTE operations include “Write BTE with ROP”, “Read BTE”, “Transparent Write BTE”, “Color Expand”, “Color Expand with Transparency”.
2. Font Write Interrupt indicates the completion of the font character writing to the DDRAM.

REG[F1h] Interrupt Control Register2 (INTC2)

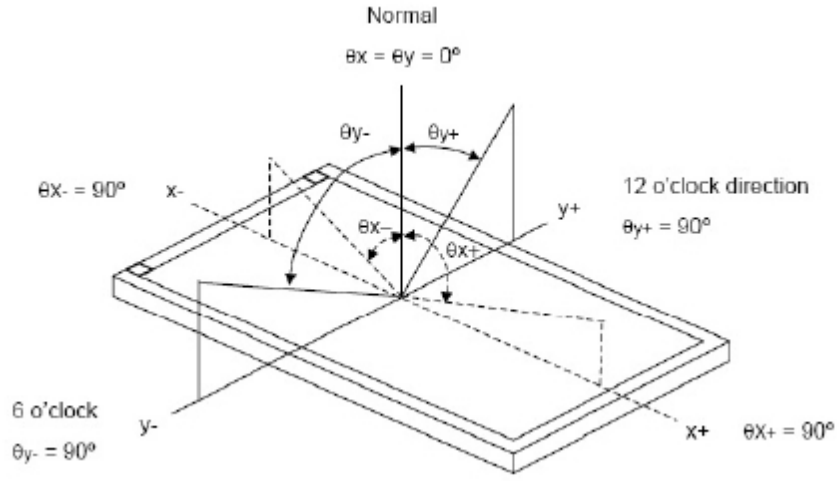
Bit	Description	Default	Access
7-5	NA	0	RO
4	**Write Function KEYSCAN Interrupt Clear Bit** 0 : No operation. 1 : Clear the keyscan interrupt. **Read Function ➔ KEYSCAN Interrupt Status** 0 : No keyscan interrupt happens. 1 : Keyscan interrupt happens.	0	RW
3	**Write Function➔ DMA Interrupt Clear Bit** 0 : No operation. 1 : Clear the DMA interrupt. **Read Function ➔ DMA Interrupt Status** 0 : No DMA interrupt happens. 1 : DMA interrupt happens.	0	RW
2	**Write Function➔ Touch Panel Interrupt Clear Bit** 0 : No operation. 1 : Clear the touch interrupt. **Read Function ➔ Touch Panel Interrupt Status** 0 : No Touch Panel interrupt happens. 1 : Touch Panel interrupt happens.	0	RW
1	**Write Function➔ BTE Process Complete Interrupt Clear Bit** 0 : No operation. 1 : Clear BTE process complete interrupt. **Read Function➔BTE Interrupt Status** 0: No BTE process complete interrupt happens. 1: BTE process complete interrupt happens.	0	RW
0	**When MCU-relative BTE operation is selected (*1) and BTE Function is Enabled (REG[50h] Bit7 = 1)** **Write Function➔ BTE Interrupt for MCU R/W Enable Bit** 0 : No operation. 1 : Clear BTE MCU R/W interrupt. **Read Function ➔ BTE R/W Interrupt Status** 0: No BTE interrupt for MCU R/W happens. 1: BTE interrupt for MCU R/W happens. **When BTE is not Enable and Text Mode is Enable Write Function➔ Font Write Interrupt (*2) Enable Bit** 0 : No operation. 1 : Clear font write interrupt. **Read Function ➔ Font Write Interrupt Status** 0: No font write interrupt happens. 1: Font write interrupt happens.	0	RW

Note:
Please refer to RA8875 data sheet for details

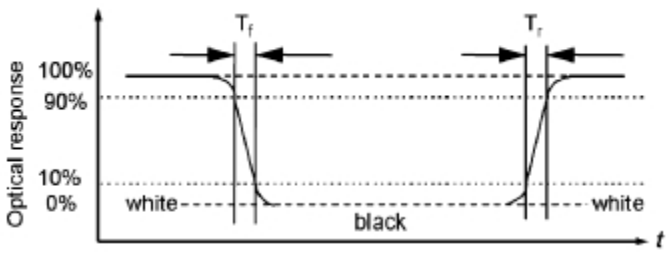
8. Optical Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	UNIT	Note.
Viewing angle (CR≥10)	θ_L	9 o'clock	60	70	-	degree	*2
	θ_R	3 o'clock	60	70	-		
	θ_T	12 o'clock	40	50	-		
	θ_B	6 o'clock	60	70	-		
Response Time	T_f	Normal θ=0°	-	10	20	msec	*3
	T_r		-	15	30	msec	
Contrast ratio	CR		400	500	-	-	*1
Color chromaticlty	W_X		0.26	0.31	0.36	-	
	W_Y		0.28	0.33	0.38	-	
Luminance	L		-	160	-	cd/m^2	*4
Luminance uniformity	Y_U		70	75	-	%	*4

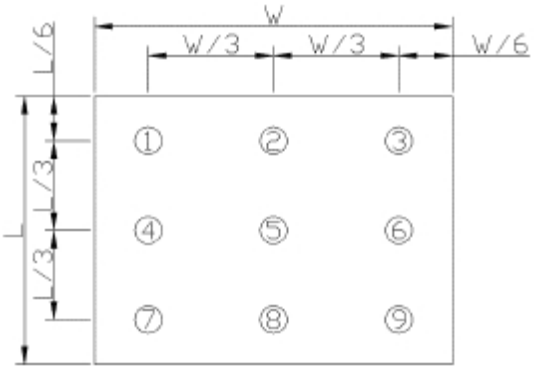
Note:
*1. Definition of Contrast Ratio
The contrast ratio could be calculate by the following expression:
Contrast Ratio (CR) = Luminanc with all pixels white / Luminance with all pixels black
*2 Definition of Viewing Angle



*3 Definition of response time



*4 Definition of Luminance Uniformity
Luminance uniformity (Lu)=
Min. Luminance form pt1~pt9 / Max Luminance form Pt1~pt9



9. Precautions of using LCD Modules

Please refer to "LCD-Module-Design-Handling-Precaution.pdf".

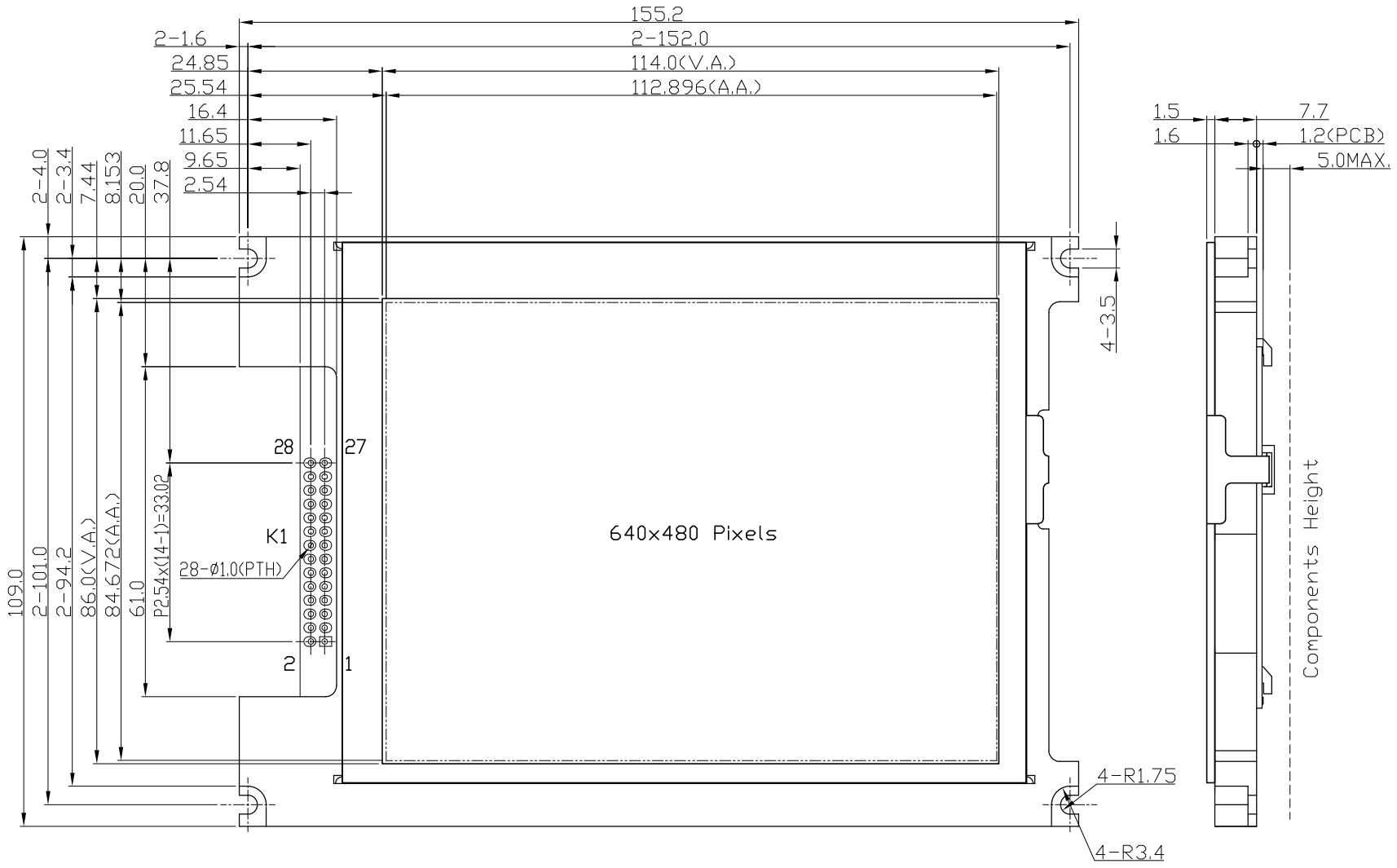
10. Appendix <Inspection items and criteria for appearance defect>

Bright/Dark Dots:

Defect Type	Specification	Major	Minor
Bright Dots	N≤ 2		●
Dark Dots	N≤ 3		●
Total Bright and Dark Dots	N≤ 4		●

Note: 1. **The definition of dot:** The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.

2. **Bright dot:** Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
3. **Dark dot:** Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue pattern.



K1 Terminal	
No	Pin Name
1	VSS
2	VSS
3	VDD
4	VDD
5	D/C
6	/CS
7	/RES
8	D0
9	D1
10	D2
11	D3
12	D4
13	D5
14	D6
15	D7
16	TE
17	/RD
18	/WR
19	NC
20	NC
21	/INT
22	NC
23	NC
24	NC
25	NC
26	NC
27	NC
28	NC

Note:
*1. LCD Display Type: TFT,Transmissive
*2. Pixel Arrangment: RGB-STRIPE
*3. Interface : MCU (8bit)
*4. Color Depth : 65K colors
*5. Operating Voltage : 5.0V
*6. Backlight : LEDs
*7. Operating Temperature : -20°C~70°C
*8. Storage Temperature : -30°C~80°C

C		
B		
A		
Rev	Note	Date

Dwg Title	LMT056DIDFWD-AEA Outline Dwg			
Dwg No.	MK-005942-1-1			Date 2016-12-22
Scale 6/5	Tol. ±0.5	Unit mm	Paper Size A3	
Approved		Checked	Drawn Luo Lin	

TOPWAY