深圳市拓普微科技开发有限公司
SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LMT070DICFWD-NSD-1

LCD Module User Manual

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Yu		
Date: 2019-08-21	Date:	Date:

Rev.	Descriptions	Release Date
0.1	Preliminary release	2019-08-21

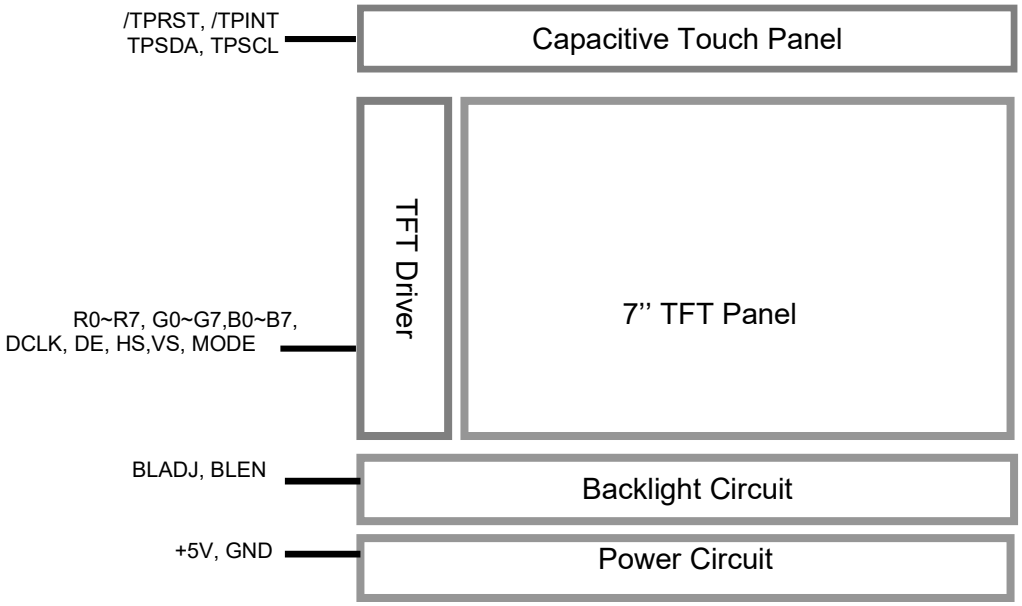
Table of Content

General Specification

Signal Interface :	Digital 24-bits RGB
Display Technology :	a-Si TFT active matrix
Display Mode :	TN Type Full Color / Transmissive / Normal White
Screen Size(Diagonal) :	7.0”
Outline Dimension :	164.9 x 100.0 x 10.88 MAX (mm) (see attached drawing for details)
Active Area :	154.08 x 85.92 (mm)
Number of dots :	800 x 480
Pixel Pitch :	0.1926 x 0.179 (mm)
Pixel Configuration :	RGB Stripe
Backlight :	LED
Viewing Direction :	12 o’clock(Gray scale Inversion) (*1) 6 o’clock (*2)
Touch Panel Type:	Capacitive Touch Panel
Operating Temperature :	-20 ~ +70°C
Storage Temperature :	-30 ~ +80°C

Note:
*1. For saturated color display content (eg. pure-red, pure-green, pure-blue or pure-colors-combinations).
*2. For “color scales” display content.
*3. Color tone may slightly change by temperature and driving condition.

Block Diagram



Terminal Function (Input Terminal)

Pin No.	Pin Name	I/O	Descriptions
1	5V	Power	5V power supply
:	:		
5	5V		
6	GND	Power	0V power supply
:	:		
10	GND		
11	BLADJ	Input	Backlight brightness PWM signal (active low)
12	BLEN	Input	Backlight enable signal (active high)
13	MODE	Input	when MODE = "1": DE mode (default). when MODE = "0": SYNC mode, DE must be grounded.
14	DE	Input	Data Input Enable
15	VS	Input	Vertical sync signal
16	HS	Input	Horizontal sync signal
17	B7	Input	Blue data line
:	:		
23	B1	Input	Blue data line(*1)
24	B0	Input	Blue data line(*1)
25	G7	Input	Green data line
:	:		
31	G1	Input	Green data line(*1)
32	G0	Input	Green data line(*1)
33	R7	Input	Red data line
:	:		
39	R1	Input	Red data line(*1)
40	R0	Input	Red data line(*1)
41	GND	Power	Ground, 0V
42	DCLK	Input	Pixel clock(*2)
43	GND	Power	Ground, 0V
44	NC	NC	No Connection
45	GND	Power	Ground, 0V
46	/TPRST	Input	Reset signal, active low reset
47	/TPINT	Output	Interrupt signal, active low interrupt
48	TPSDA	I/O	I2C data (*3)
49	TPSCL	Input	I2C clock (*3)
50	GND	Power	Ground

Note:

*1. When input 18bits RGB data, the two low bits of R,G and B data must be grounded.

*2. Data shall be latched at the falling edge of DCLK.

*3. With internal resister(4.7k) pull up.

Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Power Voltage	V_{5V}	-0.3	+5.5	V	GND = 0V
Operating Temperature	T_{OP}	-20	+70	℃	No Condensation
Storage Temperature	T_{ST}	-30	+80	℃	No Condensation

Cautions:

Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

DC Characteristics

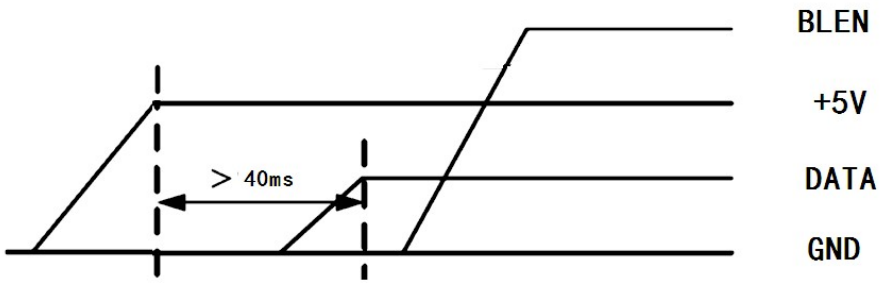
GND=0V, V_{5V} =5.0V, T_{OP} =25℃

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Power Voltage	V_{5V}	4.5	5.0	5.5	V	5V
Operating Current (*1)	I_{5V}	-	510	1020	mA	
Input High Voltage	V_{IH}	3.0	-	3.6	V	Input pins
Input Low Voltage	V_{IL}	0	-	0.3	V	Input pins
Output Signal High Voltage	V_{oH}	3.0	-	3.6	V	
Output Signal Low Voltage	V_{oL}	0	-	0.6	V	

Note:
*1. For different LCM, the value may have a bit of difference.
*2. To test the current dissipation, use “all Black Pattern”.

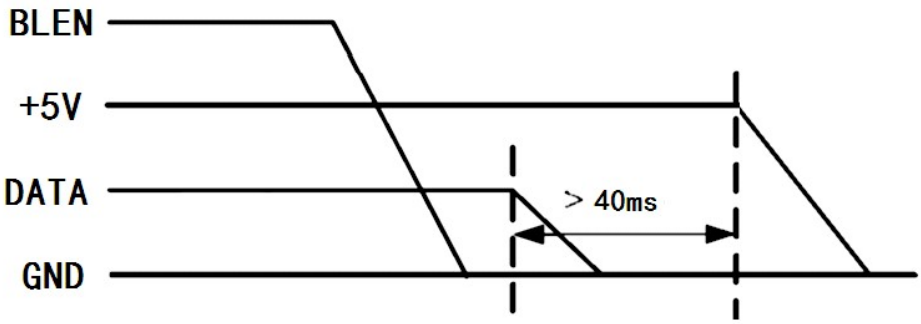
Power Sequence

Power on:



+5V →DATA→BLEN

Power off:



BLEN →DATA→+5V

Note :Data include R0~R7,B0~B7,G0~G7, DCLK, HS, VS, DE, MODE, /TPRST, /TPINT, TPSDA, TPSCL.

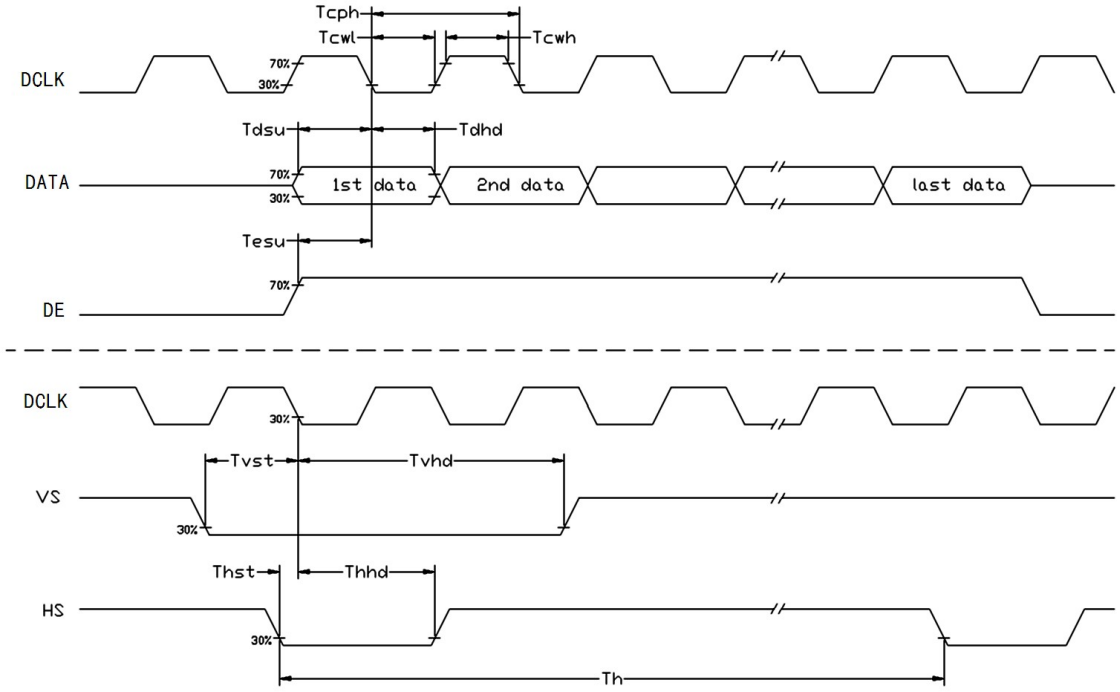
AC Characteristics

Timing Characteristics

Item	Symbol	MIN.	TYP.	MAX.	Unit	Remark
HS setup time	Thst	8	-	-	ns	
HS hold time	Thhd	8	-	-	ns	
VS setup time	Tvst	8	-	-	ns	
VS hold time	Tvhd	8	-	-	ns	
Data setup time	Tdsu	8	-	-	ns	
Data hole time	Tdhd	8	-	-	ns	
DE setup time	Tesu	8	-	-	ns	
DV_{DD} Power On Slew rate	TPOR	-	-	20	ms	From 0 to 90% DV_{DD}
DCLK cycle time	Tcph	20	-	-	ns	
DCLK pulse duty	Tcwh	40	50	60	%	

Note: For the details of the timing, please see the Driver IC data sheet.

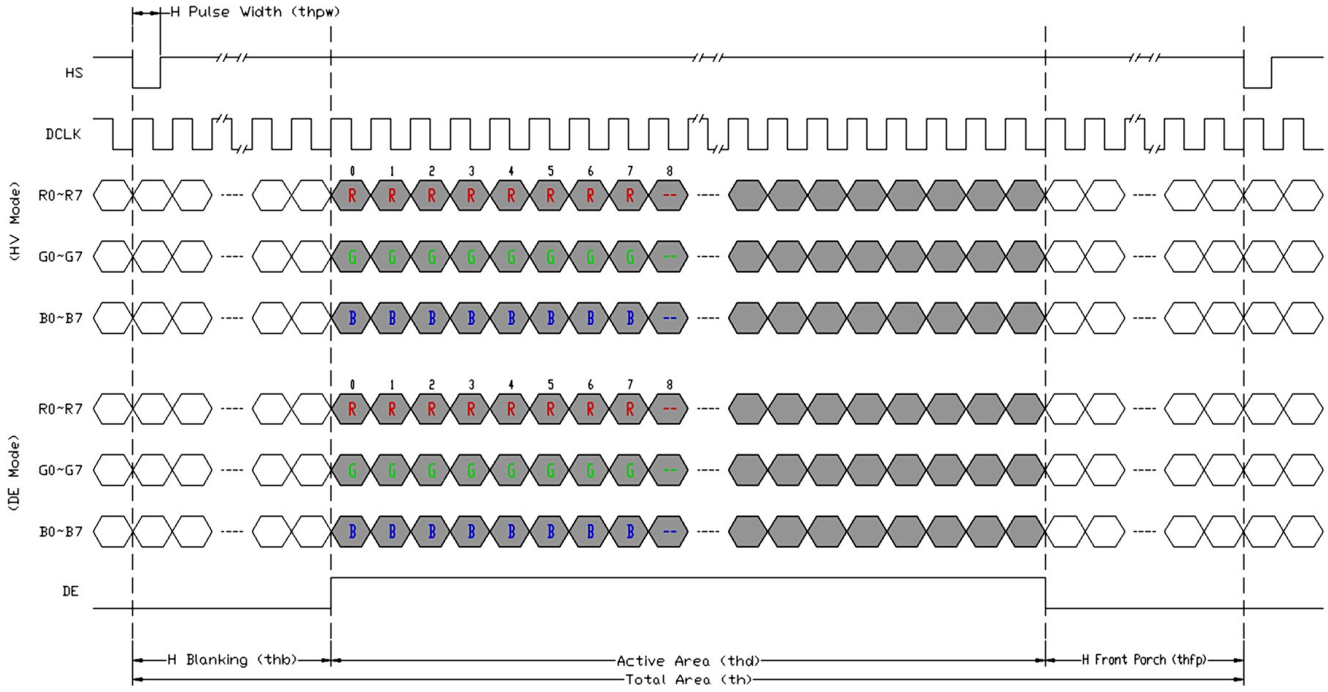
Input Clock and Data Timing Diagram



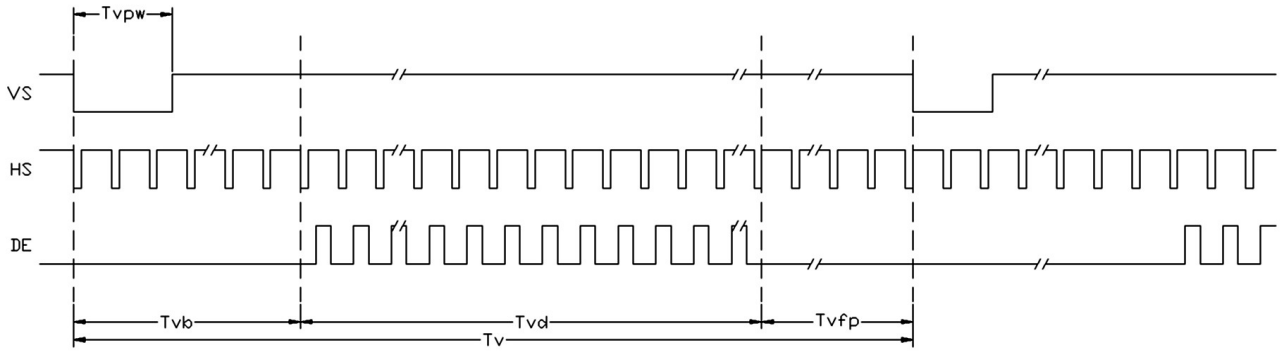
AC Timing

Item	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Horizontal Display Area	thd	-	800	-	DCLK	
DCLK Frequency	fclk	26.4	33.3	46.8	MHz	
One Horizontal Line	th	862	1056	1200	DCLK	
HS pulse width	thpw	1	-	40	DCLK	
HS Blanking	thb	46	46	46	DCLK	
HS Front Porch	thfp	16	210	354	DCLK	
Vertical Display Area	tvd	-	480	-	TH	
VS period time	tv	510	525	650	TH	
VS pulse width	tvpw	1	-	20	TH	
VS Blanking	tvb	23	23	23	TH	
VS Front Porch	tvfp	7	22	147	TH	

Data Input Format



Horizontal input timing diagram.



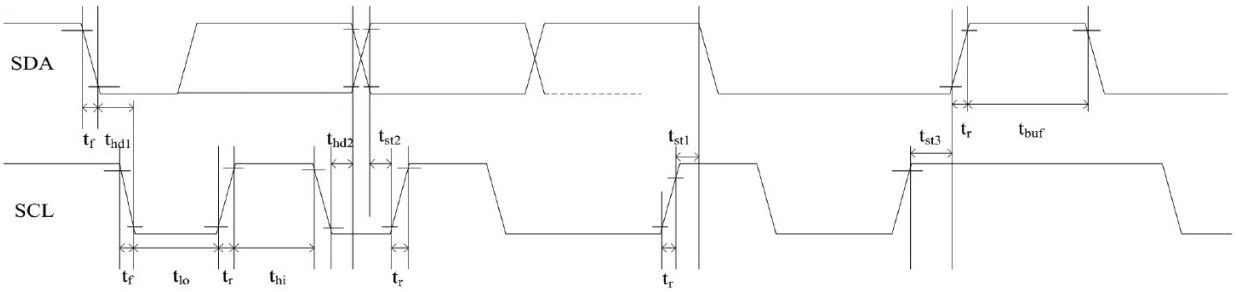
Vertical input timing diagram.

CTP Function Characteristics

I²C Communication

CTP provides standard I²C interface for communication. In the system, CTP always works in slave mode, all communications are initiated by master, and the baud rate can be up to 400Kbps. The definition of I²C timing is as following:

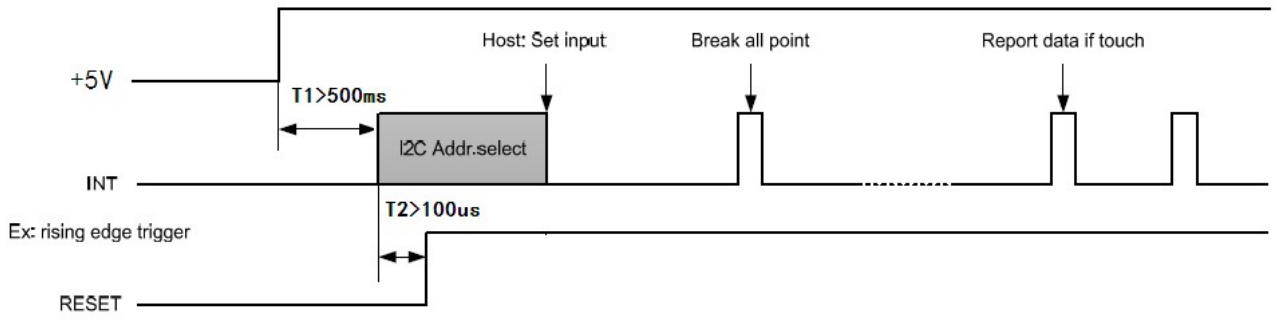
Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for start condition	t_{st1}	0.6	-	us
SCL setup time for stop condition	t_{st3}	0.6	-	us
SCL hold time for start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us



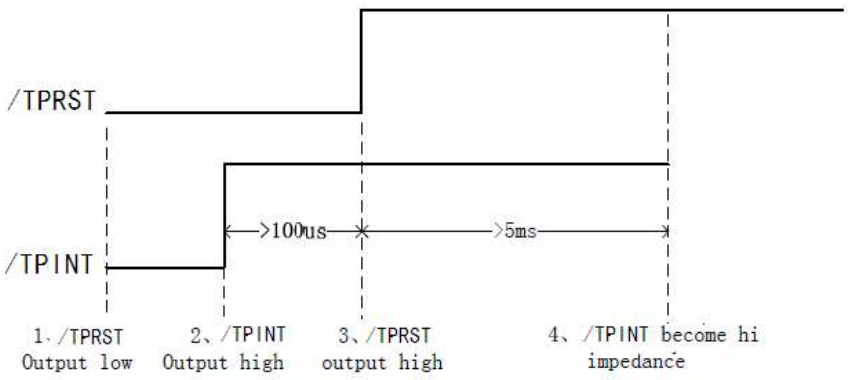
I²C Timing

CTP has 2 sets of slave address 0xBA/0xBB & 0x28/29. Master can control Reset & INT pin to configure the slave address in power on initial state like following:

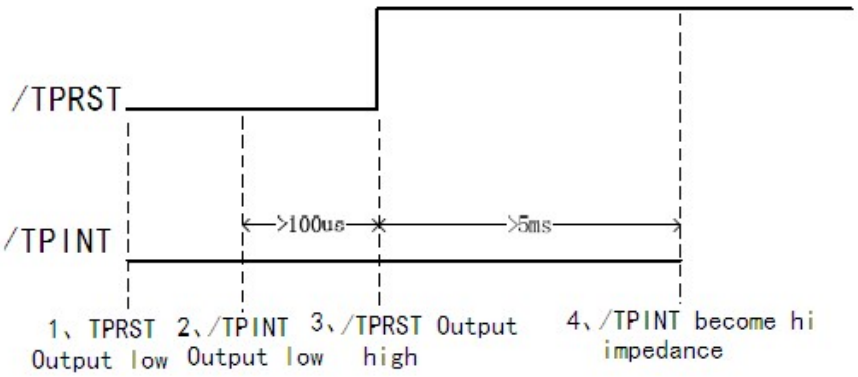
Power on diagram:



Timing of setting slave address to 0x28/0x29:



Timing of setting slave address to 0xBA/0xBB:



Data Transmission

(ex: slave address is 0xBA/0xBB)

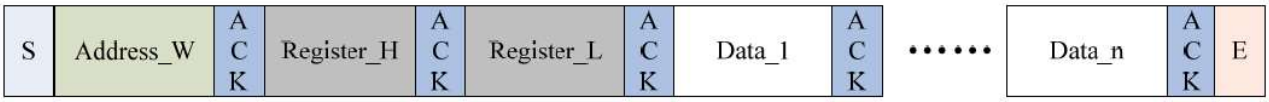
Communication is always initiated by master, A high-to-low transition of SDA with SCL high is a start condition.

All addressing signal are serially transmitted to and from on bus in 8-bit word. CTP sends a“0” to acknowledge when the addressing word is 0xBA/BB (or 0x28/0x29). This happens during the ninth clock cycle. If the slave address is not matched, CTP will stay in idle state.

The data words are serially transmitted to and from in 9-bit formation: 8-bit data + 1-bit ACK or NACK sent by CTP. Data changes during SCL low periods & keeps valid during SCL high.

A low-to-high transition of SDA with SCL high is a stop condition.

Write Data to CTP



Write Operations

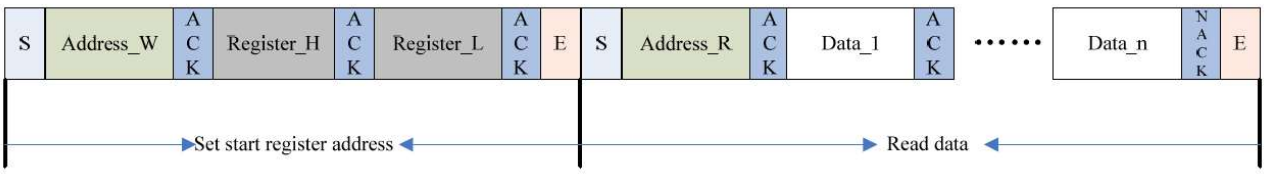
Please check the above figure, master start the communication first, and then sends device address 0XBA preparing for a write operation.

After receiving ACK from CTP, master sends out 16-bit register address, and then the data word in 8-bit, which is going to be wrote into CTP.

The address pointer of CTP will automatically increase one after one byte writing, so master can sequentially write in one operation. When operation finished, master stop the communication.

Read Data from CTP

(ex: slave address is 0xBA/0xBB)



Read Operations

Please check the above figure, master start the communication first, and then sends device address 0xBA for a write operation.
After receiving ACK from CTP, master sends out 16-bit register address, to set the address pointer of

CTP. After receiving ACK, master produce start signal once again & send device address 0xBB , then read data word from CTP in 8-bit.

CTP also supports sequential read operation, and the default setting is sequential read mode. Master shall send out ACK after every byte reading successfully but NACK after the last one. Then sends stop signal to finish the communication.

Register Information of CTP

Real Time Order(Write Only)

Addr	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x8040	Command	0：read coordinate 1：read diff data or raw data 2：software reset3:baseline update 4: baseline calibration 5: screen off 3&4 are still internal test							

Configuration Information(R/W)

	Config Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x8047	Config_ Version	Version of the configuration							
0x8048	X Output Max (Low Byte)	Resolution of X axis							
0x8049	X Output Max (High Byte)								
0x804A	Y Output Max (Low Byte)	Resolution of Y axis							
0x804B	Y Output Max (High Byte)								
0x804C	Touch Number	Reserved				Touch number：1~5			
0x804D	Module_ Switch1	Reserved		Stretch_rank		X2Y	Reserved	INT trigger method 00：rising edge trigger 01：falling edge trigger 02：low level enquiry 03：high level enquiry	
0x804E	Module_ switch2	Reserved							
0x804F	Shake_Count	Reserved				Finger shake count			
0x8050	Filter	First_Filter		Normal_Filter (filtering value of original coordinate					

			window, coefficiency is 1)
0x8051	Large_Touch	Number of touch in large area	
0x8052	Noise_ Reduction	Reserved	Value of noise elimination (coefficient is 1, 0~15)
0x8053	Screen_ Touch_Level	Threshold of touch grow out of nothing	
0x8054	Screen_ Leave_Level	Threshold of touch grow out of nothing	
0x8055	Low_Power_ Control	Reserved	Time to low power consumption (0~15s)
0x8056	Refresh_Rate	Reserved	Coordinate report rate (Cycle: 5+N ms)
0x8057	x_threshold	Reserved	
0x8058	y_threshold		
0x8059	X_Speed_Limit	Reserved	
0x805A	Y_Speed_Limit		
0x805B	Space	Blank area of boarder-top (coefficient is 32)	Blank area of Boarder-bottom (coefficient is 32)
0x805C		Blank area of boarder-left (coefficient is 32)	Blank area of Boarder-right (coefficient is 32)
0x805D	Stretch_Rate	Reserved	Level of weak stretch (Stretch X/16 Pitch) （beta version is valid，published version is not）
0x805E	Stretch_R0	Interval 1 coefficient	
0x805F	Stretch_R1	Interval 2 coefficient	
0x8060	Stretch_R2	Interval 3 coefficient	
0x8061	Stretch_RM	All intervals base number	
0x8062	Drv_GroupA_ Num	All_Driving / Reserved	Driver_Group_A_number
0x8063	Drv_GroupB_ Num	Reserved	Driver_Group_B_number
0x8064	Sensor_Num	Sensor_Group_B_Number	Sensor_Group_A_Number
0x8065	FreqA_factor	Driver frequency double frequency coefficient of Driver group A GroupA_Frequence = Multiplier factor * baseband	
0x8066	FreqB_factor	Driver frequency double frequency coefficient of Driver group B GroupB_Frequence = Multiplier factor * baseband	
0x8067	Pannel_ BitFreqL	Baseband of Driver group A\B (1526HZ<baseband<14600Hz)	
0x8068	Pannel_ BitFreqH		

0x8069	Pannel_Sensor_TimeL	Time interval of the neibouring two driving signal (Unit: us), Reserved.			
0x806A	Pannel_Sensor_TimeH				
0x806B	Pannel_Tx_Gain	Reserved		Pannel_Drv_output_R 4 gears	Pannel_DAC_Gain 0:Gain maximum 7: Gain minimum
0x806C	Pannel_Rx_Gain	Pannel_PGA_C	Pannel_PGA_R	Pannel_Rx_Vcmi (4 gears)	Pannel_PGA_Gain (8 gears)
0x806D	Pannel_Dump_Shift	Reserved		Magnification coefficient of original value (The Nth power of 2)	
0x806E	Drv_Frame_Control	Reserved	SubFrame_DrvNum		Repeat_Num
0x806F	NC	Reserved			
0x8070	NC	Reserved			
0x8071	NC	Reserved			
0x8072	NC	Reserved			
0x8073	NC	Reserved			
0x8074	NC	Reserved			
0x8075	NC	Reserved			
0x8076	NC	Reserved			
0x8077	NC	Reserved			
0x8078	NC	Reserved			
0x8079	NC	Reserved			
0x807A	Freq_Hopping_Start	Frequency hopping start frequency (Unit: 2KHz, 50 means 100KHz)			
0x807B	Freq_Hopping_End	Frequency hopping stop frequency (Unit: 2KHz, 150 means 300KHz)			
0x807C	Noise_Detect_Times	Detect_Stay_Times	Detect_Confirm_Times		
0x807D	Hopping_Flag	Hopping_En	Reserved	Detect_Time_Out	

0x807E	Hoppging_ Threshold	Large_Noise_Threshold	Hopping_Hit_Threshold
0x807F	Noise_ Threshold	Threshold of noise level	
0x8080	NC	Reserved	
0x8081	NC	Reserved	
0x8082	Hopping_seg1_ BitFreqL	Frequency hopping segment band 1 central frequency (for driver A/B)	
0x8083	Hopping_seg1_ BitFreqH		
0x8084	Hopping_seg1_ Factor	Frequency hopping segment 1 central frequency coefficient	
0x8085	Hopping_seg2_ BitFreqL	Frequency hopping segment band 2 central frequency (for driver A/B)	
0x8086	Hopping_seg2_ BitFreqH		
0x8087	Hopping_seg2_ Factor	Frequency hopping segment 2 central frequency coefficient	
0x8088	Hopping_seg3_ BitFreqL	Frequency hopping segment band 3 central frequency (for driver A/B)	
0x8089	Hopping_seg3_ BitFreqH		
0x808A	Hopping_seg3_ Factor	Frequency hopping segment 3 central frequency coefficient	
0x808B	Hopping_seg4_ BitFreqL	Frequency hopping segment band 4 central frequency (for driver A/B)	
0x808C	Hopping_seg4_ BitFreqH		
0x808D	Hopping_seg4_ Factor	Frequency hopping segment 4 central frequency coefficient	
0x808E	Hopping_seg5_ BitFreqL	Frequency hopping segment band 5 central frequency (for driver A/B)	
0x808F	Hopping_seg5_ BitFreqH		
0x8090	Hopping_seg5_ Factor	Frequency hopping segment 5 central frequency coefficient	
0x8091	NC	Reserved	
0x8092	NC	Reserved	
0x8093	Key 1	Key 1 Position: 0-255 valid (0 means no touch, it means independent touch key when 4 of the keys are 8 multiples, Reserved	
0x8094	Key 2	Key 2 position, Reserved	

0x8095	Key 3	Key 3 position, Reserved	
0x8096	Key 4	Key 4 position, Reserved	
0x8097	Key_Area	Time limit for long press(1~16 s) , Reserved	Touch valid interval setting: 0-15 valid, Reserved
0x8098	Key_Touch_Level	Key threshold of touch key, Reserved	
0x8099	Key_Leave_Level	Key threshold of touch key, Reserved	
0x809A	Key_Sens	KeySens_1(sensitivity coefficient of key 1, same below) , Reserved	KeySens_2, Reserved
0x809B	Key_Sens	KeySens_3, Reserved	KeySens_4, Reserved
0x809C	Key_Restrain	Finger from screen left after inhibition of key time(Unit:100ms,0 means 600ms) , Reserved	The independent button pro key inhibition parameters, Reserved
0x809D	NC	Reserved	
0x809E	NC	Reserved	
0x809F	NC	Reserved	
0x80A0	NC	Reserved	
0x80A1	NC	Reserved	
0x80A2	NC	Reserved	
0x80A3	NC	Reserved	
0x80A4	NC	Reserved	
0x80A5	NC	Reserved	
0x80A6	NC	Reserved	
0x80A7	NC	Reserved	
0x80A8	NC	Reserved	
0x80A9	NC	Reserved	
0x80AA	NC	Reserved	
0x80AB	NC	Reserved	
0x80AC	NC	Reserved	
0x80AD	NC	Reserved	
0x80AE	NC	Reserved	
0x80AF	NC	Reserved	
0x80B0	NC	Reserved	
0x80B1	NC	Reserved	
0x80B2	NC	Reserved	
0x80B3	NC	Reserved	
0x80B4	NC	Reserved	
0x80B5	NC	Reserved	
0x80B6	NC	Reserved	
0x80B7	Sensor_CH0~	ITO Sensor corresponding chip channel number	

~ 0x80C4	Sensor_CH13	
0x80C5 ~ 0x80D4	NC	Reserved
0x80D5 ~ 0x80EE	Driver_CH0~ Driver_CH25	ITO Driver corresponding chip channel number
0x80EF ~ 0x80FE	NC	Reserved
0x80FF	Config_Chksum	configuration information verify (the complement number of total byte from 0x8047 to 0x80FE)
0x8100	Config_Fresh	signal of updated configuration (the host writes)

Coordinates Information

Addr	Access	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x8140	R	Product ID (first byte，ASCII)							
0x8141	R	Product ID (second byte，ASCII)							
0x8142	R	Product ID (third byte，ASCII)							
0x8143	R	Product ID (forth byte，ASCII)							
0x8144	R	Firmware version (HEX.low byte)							
0x8145	R	Firmware version (HEX.high byte)							
0x8146	R	x coordinate resolution (low byte)							
0x8147	R	x coordinate resolution (high byte)							
0x8148	R	y coordinate resolution (low byte)							
0x8149	R	y coordinate resolution (high byte)							
0x814A	R	Vendor_id (current module option information)							
0x814B	R	Reserved							
0x814C	R	Reserved							
0x814D	R	Reserved							
0x814E	R/W	buffer status		large detect		Reserved		number of touch points	
0x814F	R	track id							
0x8150	R	point 1 x coordinate (low byte)							
0x8151	R	point 1 x coordinate (high byte)							
0x8152	R	point 1 y coordinate (low byte)							
0x8153	R	point 1 y coordinate (high byte)							
0x8154	R	Point 1 size (low byte)							
0x8155	R	point 1 size (high byte)							
0x8156	R	Reserved							
0x8157	R	track id							

0x8158	R	point 2 x coordinate (low byte)
0x8159	R	point 2 x coordinate (high byte)
0x815A	R	point 2 y coordinate (low byte)
0x815B	R	point 2 y coordinate (high byte)
0x815C	R	point 2 size (low byte)
0x815D	R	point 2 size (high byte)
0x815E	R	Reserved
0x815F	R	track id
0x8160	R	point 3 x coordinate (low byte)
0x8161	R	point 3 x coordinate (high byte)
0x8162	R	point 3 y coordinate (low byte)
0x8163	R	point 3 y coordinate (high byte)
0x8164	R	point 3 size (low byte)
0x8165	R	point 3 size (high byte)
0x8166	R	Reserved
0x8167	R	track id
0x8168	R	point 4 x coordinate (low byte)
0x8169	R	point 4 x coordinate (high byte)
0x816A	R	point 4 y coordinate (low byte)
0x816B	R	point 4 y coordinate (high byte)
0x816C	R	point 4 size (low byte)
0x816D	R	point 4 size (high byte)
0x816E	R	Reserved
0x816F	R	track id
0x8170	R	point 5 x coordinate (low byte)
0x8171	R	point 5 x coordinate (high byte)
0x8172	R	point 5 y coordinate (low byte)
0x8173	R	point 5 y coordinate (high byte)
0x8174	R	point 5 size (low byte)
0x8175	R	point 5 size (high byte)
0x8176	R	Reserved
0x8177	R	Reserved

Note:

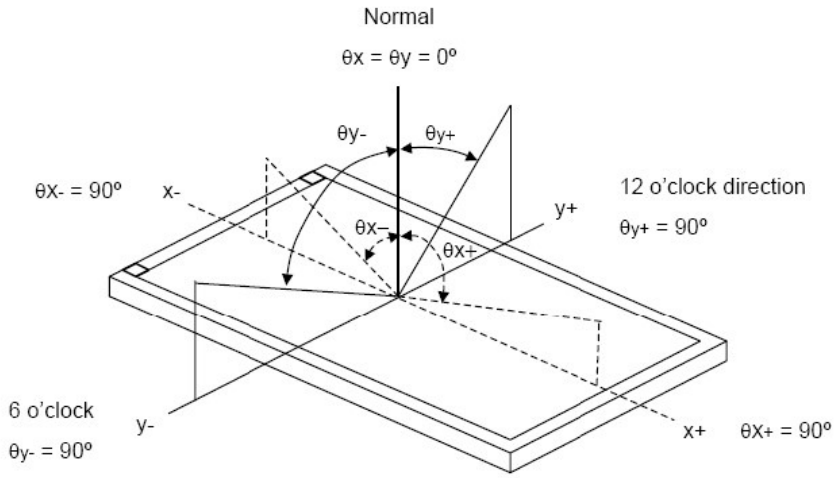
Please refer to GT911 IC datasheet for details.

Optical Characteristics

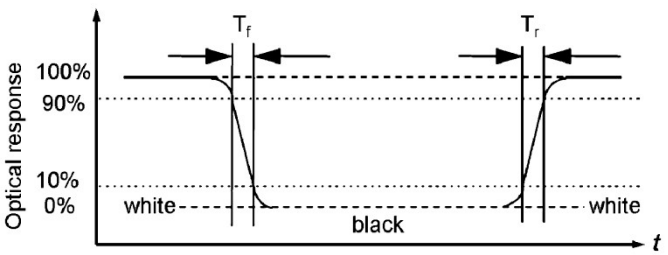
Item	Symbol	Condition	MIN.	TYP.	MAX.	UNIT	Note.
Viewing angle (CR⩾10)	θ_R	3 o'clock	60	70	-	degree	*2
	θ_L	9 o'clock	60	70	-		
	θ_B	6 o'clock	40	50	-		
	θ_T	12 o'clock	60	70	-		
Response Time	T_f	Normal θ=0°	-	10	20	msec	*3
	T_r		-	15	30	msec	
Contrast ratio	CR		400	500	-	-	*1
Color chromaticity	W_X		0.26	0.31	0.26	-	
	W_Y		0.28	0.33	0.38	-	
Luminance	L		-	400	-	cd/m²	*4
Luminance uniformity	Y_U		70	75	-	%	*4

Note:
*1. Definition of Contrast Ratio
The contrast ratio could be calculate by the following expression:
Contrast Ratio (CR) = Luminance with all pixels white / Luminance with all pixels black

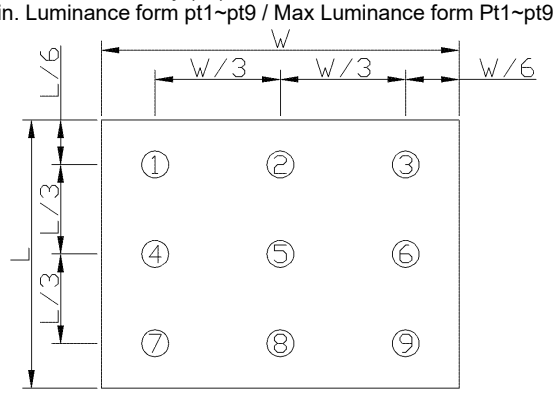
*2 Definition of Viewing Angle



*3 Definition of response time



*4 Definition of Luminance Uniformity
Luminance uniformity (Lu)=
Min. Luminance form pt1~pt9 / Max Luminance form Pt1~pt9



Precautions of using LCD Modules

Please refer to "LCD-Module-Design-Handling-Precaution.pdf".

附录一：

CTP Application Precautions

1. CTP Mounting Precaution

1.1 Bezel Mounting (Figure 1)

- The bezel window should be bigger than the CTP active area. It should be≥0.5mm each side.
- Gasket should be installed between the bezel and the CTP surface. The final gap should be about 0.5~1.0mm.
- It is recommended to provide an additional support bracket for backside support when necessary (e.g. slim type TFT module without mounding structure). They should only provide appropriate support and keep the module in place.
- The mounting structure should be strong enough to prevent external uneven force or twist act onto the module.

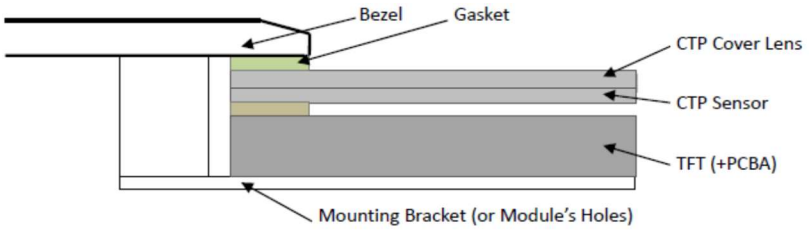


Figure 1

1.2 Surface Mounting (Figure 2)

- As the CTP assembling on the countersink area with double side adhesive. The countersink area should be flat and clean to ensure the double side adhesive installation result.
- The Bezel is recommend to keep a gap (≥0.3mm each side) around the cover lens for tolerance.
- It is recommended to provide an additional support bracket with gasket for backside support when necessary (e.g. TFT module without mounding structure). They should only provide appropriate support and keep the module in place.
- The mounting structure should be strong enough to prevent external uneven force or twist act onto the module.

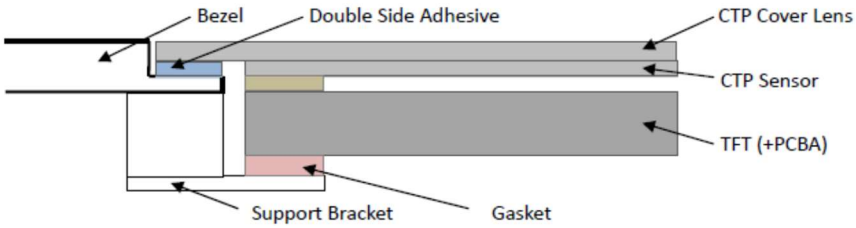


Figure 2

1.3 Additional Cover Lens Mounting (Figure 3)

- For the case of additional cover Lens mounting, it is necessary to recheck with the CTP specification about the material and thickness to ensure the functionality.
- It should keep a 0.2~0.3mm gap between the cover lens and the CTP surface..
- The cover lens window should be bigger than the active area of the CTP. It should be≥0.5mm each side.
- It is recommended to provide an additional support bracket for backside support when necessary (e.g. slim type TFT module without mounding structure). They should only provide appropriate support and keep the module in place.
- The mounting structure should be strong enough to prevent external uneven force or twist act onto the module.

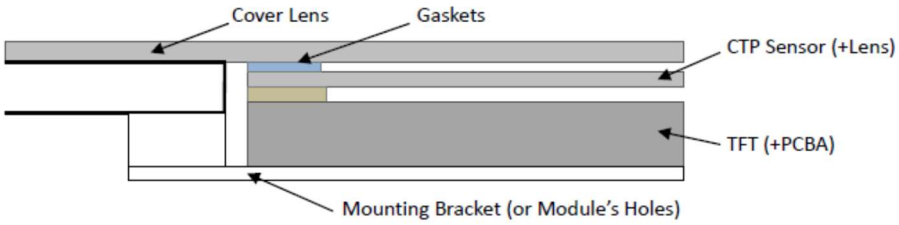


Figure 3

2. Handling Precautions

2.1 The product made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

2.2 Do not apply excessive or uneven force to the product since this may damage to the performance.

2.3 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with Isopropyl alcohol or Ethyl alcohol solvents. Solvents other than those mentioned above may damage the product. Especially, do not use Water, Ketone, Aromatic solvents.

2.4 Do not attempt to disassemble the CTP Module.

2.5 If the logic circuit power is off, do not apply the input signals.

2.6 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the CTP Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

d. The CTP Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

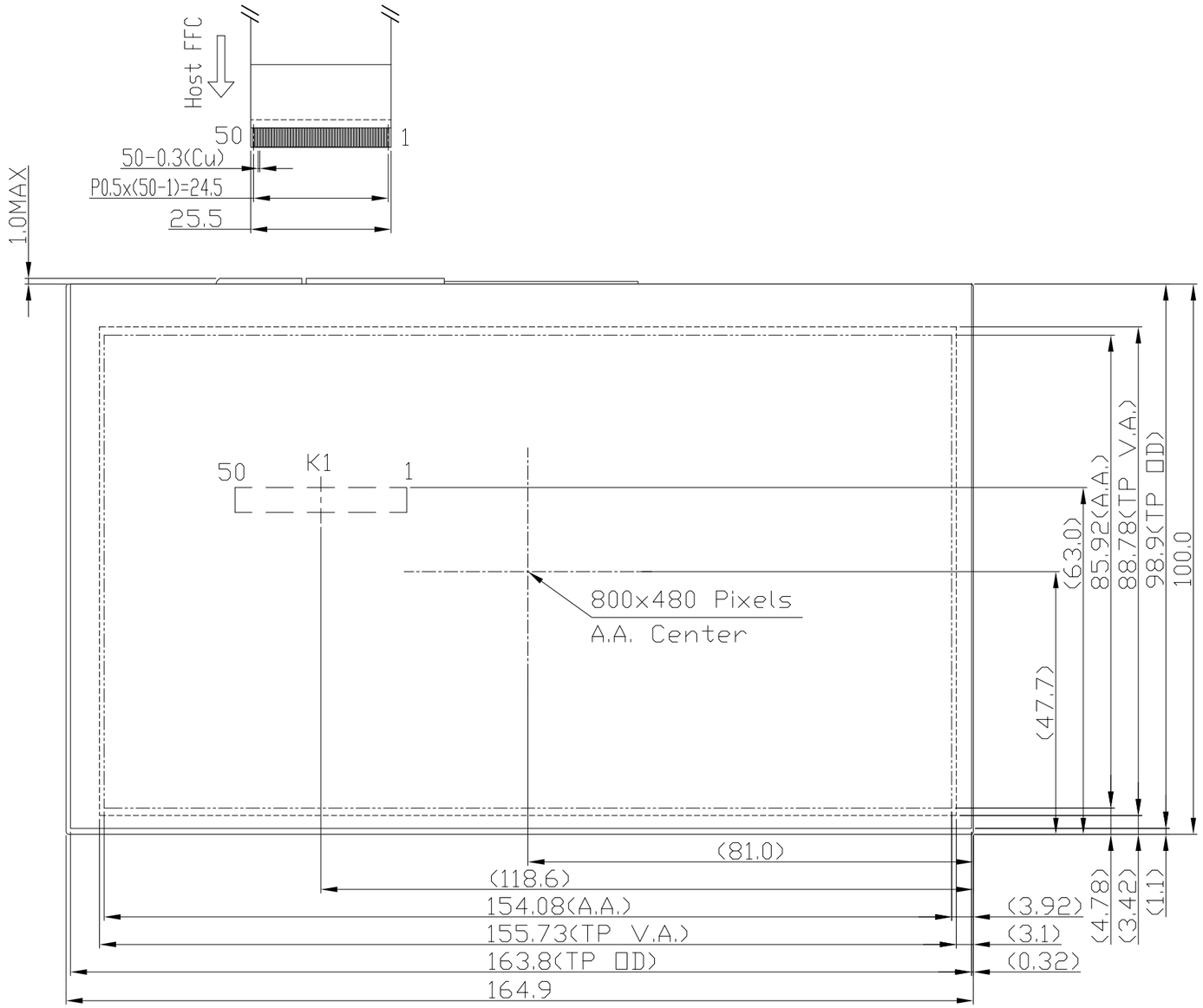
3. Storage and Transportation Precautions

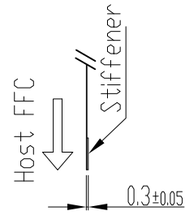
3.1 When storing the CTP modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

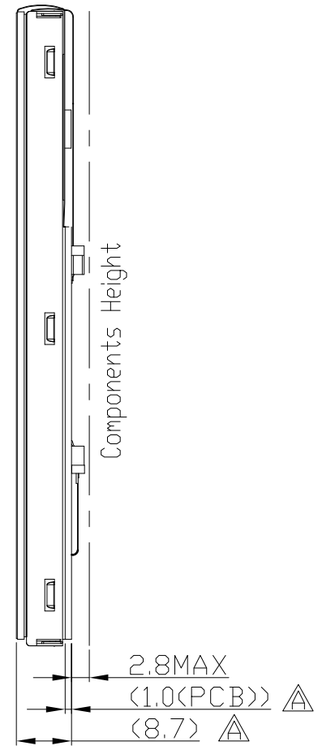
3.2 The CTP modules should be stored the required temperature range. If the CTP modules will be stored for a long time, the recommend condition is the temperature of 0~40 ℃ and relative humidity of ≤80%.

3.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

3.4 The CTP modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.







K1 Terminal	
No	Pin Name
1	5V
:	:
5	5V
6	GND
:	:
10	GND
11	BLADJ
12	BLEN
13	MODE
14	DE
15	VS
16	HS
17	B7
:	:
24	B0
25	G7
:	:
32	G0
33	R7
:	:
40	R0
41	GND
42	DCLK
43	GND
44	NC
45	GND
46	/TPRST
47	/TPINT
48	TPSDA
49	TPSCL
50	GND

Note:
*1. LCD Display Type: TFT,Transmissive
*2. Operating Voltage : 5.0V
*3. Logic Voltage : 3.3V
*4. Backlight : White LED
*5. Pixel Arrangment: RGB-STRIPE
*6. Color Depth : 16.7M (24bit)
*7. Interface : RGB_24bit
*8. Touch Panel Type : Capacitive Touch Panel
*9. K1 : FFC Socket (P0.5X50) or equivalent
*10. Operating Temperature : -20°C~70°C
*11. Storage Temperature : -30°C~80°C
*12, Unmarked Tolerace : ≤150,±0.3; >150,±0.5
*13. Applicable cover panel/cover glass thickness = 2.0MAX.(Without air gap)

Rev	Note	Date
C		
B		
A	Revise outline	yangwukun 2019-09-07

Dwg Title: LMT070DICFWD-NSD-1 Outline Dwg

Dwg No.: MK-006712a-1-1 Date: 2019-08-19

Scale: 1/1 | Tol. | Unit: mm | Paper Size: A3

Approved | Checked | Drawn: yangwukun

TOPWAY