深圳市拓普微科技开发有限公司
SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LMT121DNGFWD

LCD Module User Manual

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Date: 2014-11-13	Date:	Date:

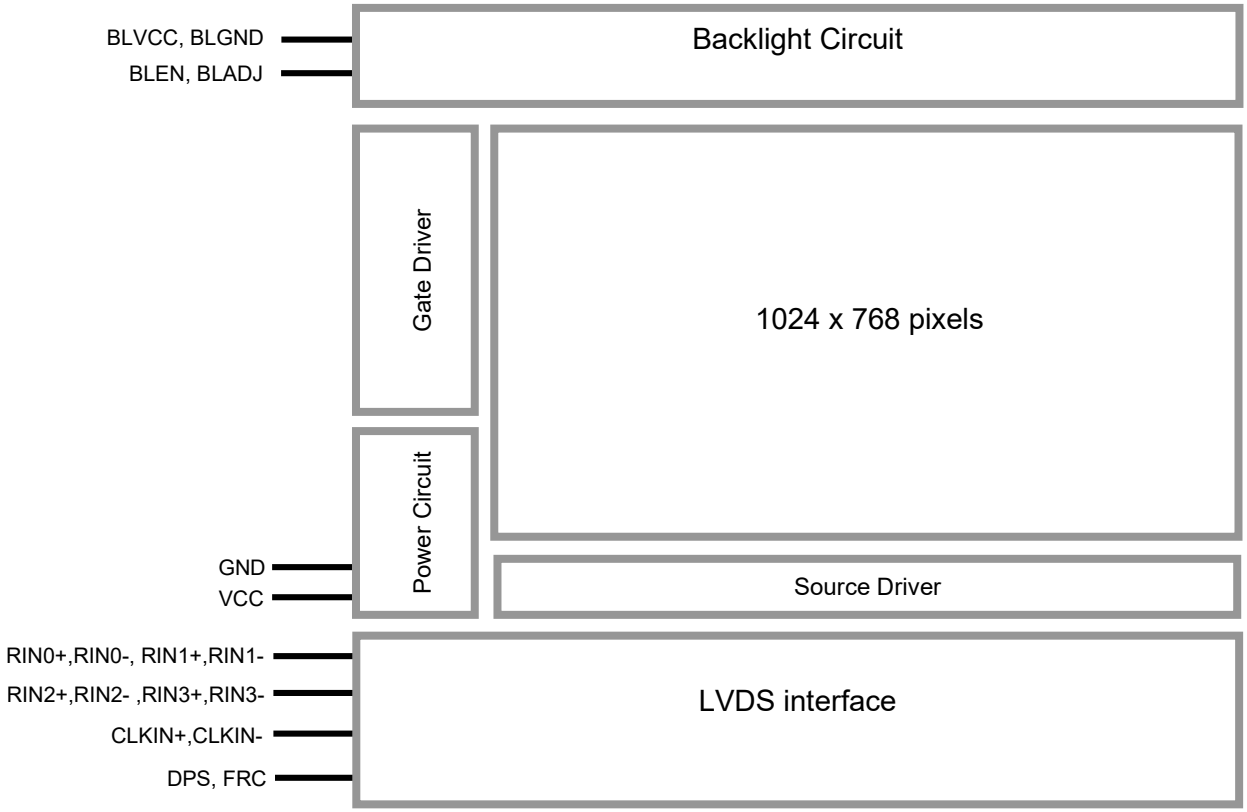
Rev.	Descriptions	Release Date
0.1	Preliminary	2014-11-13

Table of Content

1. General Specification

Signal Interface :	LVDS
Display Technology :	a-Si TFT active matrix
Display Mode :	TN Type Full Color / Transmissive / Normal White
Screen Size :	12.1 inch (Diagonal)
Outline Dimension :	279.0x209.0x9.0 (mm) (see Outline DWG for details)
Active Area :	245.76 x184.32 (mm)
Number of dots :	1024 x 768
Dot Pitch :	0.240 x 0.240(mm)
Pixel Configuration :	R.G.B. Vertical Stripe
Backlight :	White LED
Surface Treatment :	Anti-Glare
Viewing Direction :	6 o'clock
Operating Temperature :	-20 ~ +70°C
Storage Temperature :	-30 ~ +80°C

2. Block Diagram



3. Input/Output Terminals

3.1 K1 TFT Terminals

Pin No.	Pin Name	IO	Descriptions	
			24Bit Mode	18Bit Mode
1 2	VCC	Power	Power Supply	
3	GND	Power	Ground	
4	FRC	Input	H:8Bits LVDS Input (24bit mode)	L/NC: 6Bits LVDS Input (18bit mode)
5	RIN0-	Input	LVDS receiver negative signal channel 0	
6	RIN0+	Input	LVDS receiver positive signal channel 0	
7	GND	Power	Ground	
8	RIN1-	Input	LVDS receiver negative signal channel 1	
9	RIN1+	Input	LVDS receiver positive signal channel 1	
10	GND	Power	Ground	
11	RIN2-	Input	LVDS receiver negative signal channel 2	
12	RIN2+	Input	LVDS receiver positive signal channel 2	
13	GND	Power	Ground	
14	CLKIN-	Input	LVDS receiver negative signal clock	
15	CLKIN+	Input	LVDS receiver positive signal clock	
16	GND	Power	Ground	
17	RIN3-	Input	LVDS receiver negative signal channel 3.(Used for 8Bits LVDS Input; GND for 6Bits)	
18	RIN3+	Input	LVDS receiver positive signal channel 3.(Used for 8Bits LVDS Input; GND for 6Bits)	
19	DPS	Input	Display Reversed Function (H: Display Reverse; L/NC: Normal Display)	
20	NC	--	No Connection	

3.2 K2 BackLight Terminals

Pin No.	Pin Name	IO	Descriptions
1	NC	-	No Connection
2	BLADJ	Input	Backlight dimming control PWM may be used to adjust the output brightness
3	BLEN	Input	Backlight Driver Control BLEN=Hi, Backlight Driving Booster enable BLEN=Lo, Backlight Driving Booster disable
4	BLGND	Power	Power Supply GND (0V)
5	BLVCC	Power	Positive Power Supply

4. Absolute Maximum Ratings

GND=0V, T_{OP}=25°C

Items		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board	VCC	-0.3 to +3.96	V	Ta= 25℃
	LED driver	BLVCC	-0.3 to (+15.0)		
Input voltage for signals	Display signals ,Note1	VD	-0.5 to 3.96	V	
	Function signals ,Note2	VF	-0.5 to 3.96		
	Function signal for LED driver	BLADJ	-0.3 to (+15.0)	V	
		BLEN	-0.3 to (+15.0)	V	
Storage temperature		Tst	-30 to +80	℃	-
Operating temperature	Front surface	TopF	-20 to +70	℃	Note3
	Rear surface	TopR	-20 to +70	℃	Note4
Relative humidity Note5		RH	90	%	Ta ≤ 40℃
			85	%	40℃ < Ta ≤ 50℃
Absolute humidity ,Note5		AH	70,Note6	g/m3	Ta > 50℃

Note1:RIN0±,RIN1±,RIN2±,RIN3± and CLKIN±;
Note2:DPS and FRC;
Note3:Measured at LCD panel surface (including self-heat);
Note4:Measured at LCD module's rear shield surface (including self-heat);
Note5:No condensation;
Note6:Water amount at Ta= 50°C and RH= 85%.

5. Electrical Characteristics

5.1 Driving TFT LCD Panel

GND=0V, VCC=3.3V, T_{OP}=25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Note
Power supply voltage	VCC	3.0	3.3	3.96	V	
Power supply current	ICC	-	300	480	mA	*1
Permissible ripple voltage	VRP	-	-	300	mV	
Differential input threshold voltage for LVDS receiver	VTL	-100	-	-	mV	VCM=1.25V,*2
	VTH	-	-	100	mV	
Terminating resistor	RT	-	100	-	Ω	
Input voltage for DPS and FRC signals	VFH	0.7VCC	-	VCC	V	
	VFL	0	-	0.3VCC	V	

*1: All black pattern
*2: Common mode voltage for LVDS receiver

5.2 LED Backlight Circuit Characteristics

BLGND=0V ,T_{OP}=25°C

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Power supply voltage	BLVCC	10.8	12.0	12.6	V	Note 1
Power supply voltage	I_{BLVCC}	-	430	650 Note2	mA	At the maximum luminance control
Permissible ripple voltage	VRPD	-	-	200	mVp-p	For BLVCC,Note3
Input voltage for PWM signal	VDFH1	2.0	-	BLVCC	V	
	VDFL1	0	-	0.8	V	
Input voltage for BLEN signal	VDFH2	2.0	-	BLVCC	V	
	VDFL2	0	-	0.8	V	
PWM Input Frequency	f_{PWM}	200	-	20k	Hz	Note4,Note5
PWM duty ratio	DR_{PWM}	1	-	100	%	Note6,Note7
PWM pulse width	tPWH	5	-	-	us	

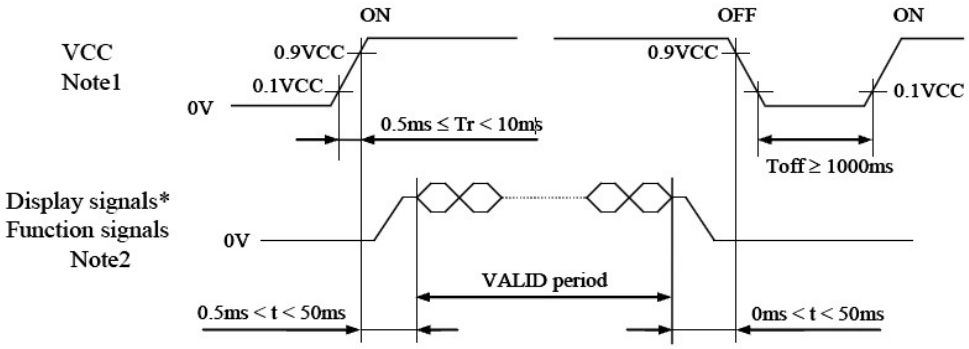
Note1:When designing of the power supply ,take the measures for the prevention of surge voltage.
Note2:This value excludes peak current such as overshoot current.
Note3:This power supply lines(BLVCC and GND)may have ripple voltage during luminance control of LED.There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on.Put a capacitor between the power supply lines(BLVCC and GND) to reduce the noise is necessary .
Note4:A recommended fPWM value is as follows.

$$f_{PWM} = \frac{2n-1}{4} \times fv$$

(n =integer,fv =frame frequency of LCD module)
Note5:Depending on the frequency used ,some noise may appear on the screen,please conduct a thorough evaluation,
Note6:While the BLEN signal is high ,do not set the tPWH(PWM pulse width) is less than 5us .It may cause abnormal working is the backlight .In this case,turn the backlight off and then on again by BLEN signal.
Note7:Regardless of the PWM frequency,both PWM duty radio and PWM pulse width must be always more than the minimum values.

5.3 Power supply voltage Sequence

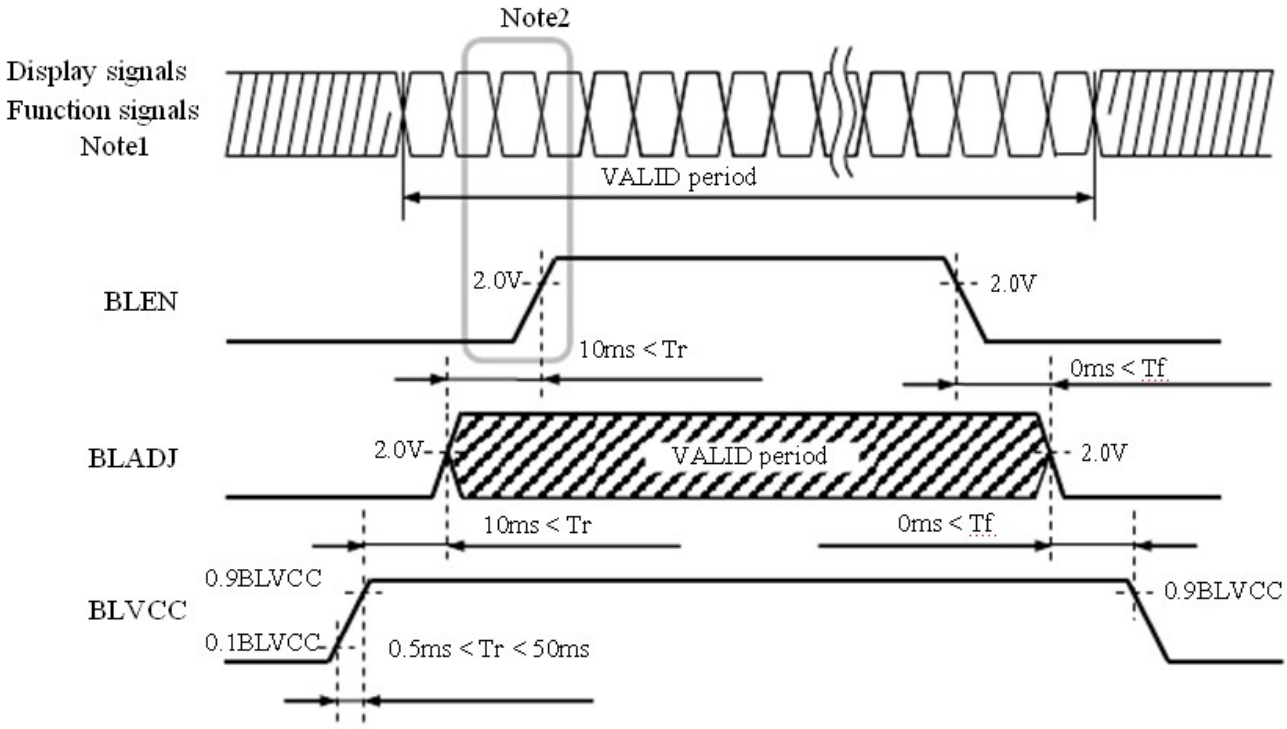
5.3.1 LCD panel signal processing board



* These signals should be measured at the terminal of 100Ω resistance.

Note1: If there is a voltage variation(voltage drop) at the rising edge of VCC below 3.0V,there is a possibility that a product does not work due to a protection circuit.
Note2: Display signals (RIN0±,RIN1±,RIN2±,RIN3± and CLKIN±) and function signals(DPS and FRC) must be set to Low or High-impedance, except the VALID period (See above sequence diagram),in order to avoid the circuitry damage .If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. If a customer stops the display and function signals, VCC also must be shut down.

5.3.2 LED Driver

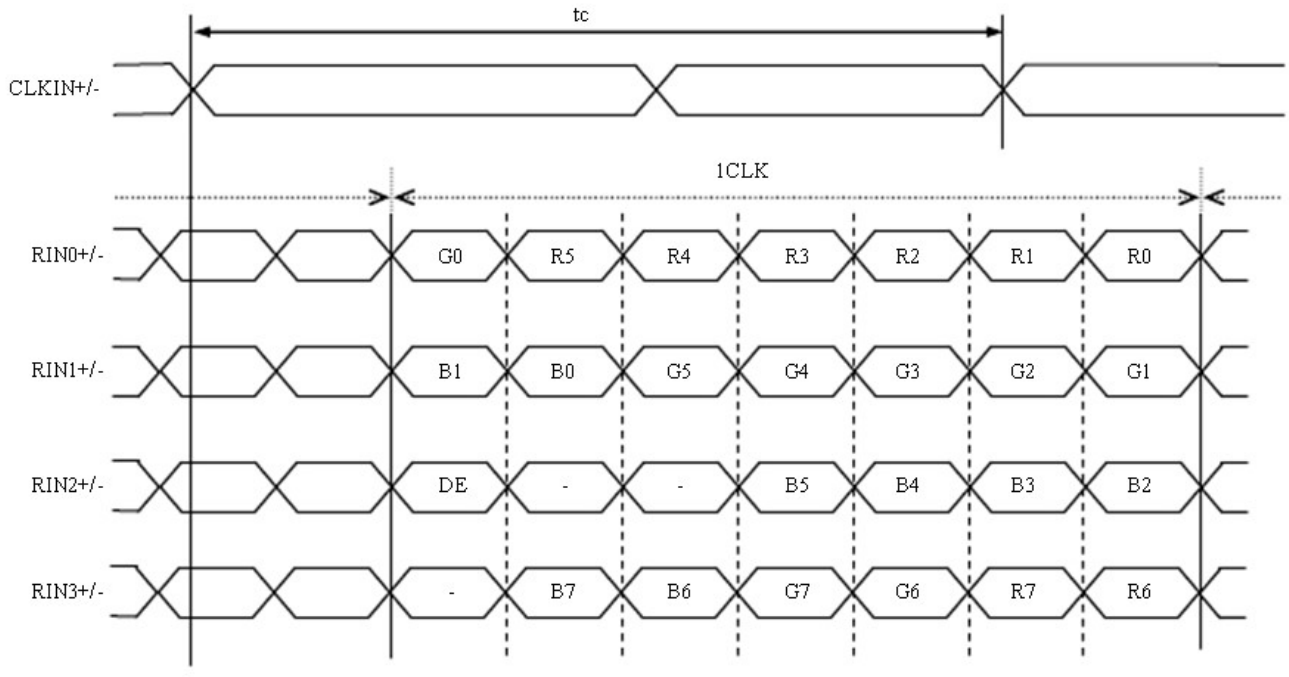


Note1:These are the display and function signals for LCD panel signal processing board.
Note2:The backlight should be turned on within the valid period of display and function signals,in order to avoid unstable data display.

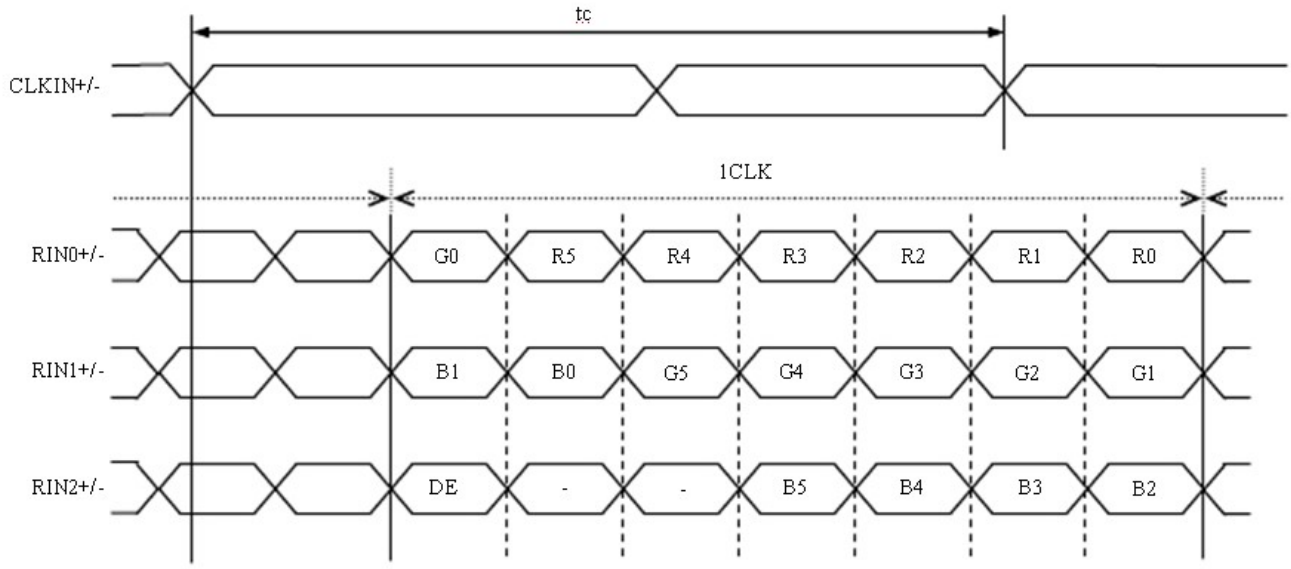
6. AC Characteristics

6.1 Input data mapping

6.1.1 LVDS Input data signal:8-bit



6.1.2 LVDS Input data signal:6-bit



6.2 Timing Characteristics

(Note1,Note2,Note3)

Parameter			Symbol	MIN.	TYP.	MAX.	Unit	Remarks
CLK	Frequency		1/tc	52.0	65.0	71.0	MHz	15.385ns (typ.)
	Duty ratio		-		-		-	-
	Rise time, Fall time		-				ns	
DATA	CLK-DATA	Setup time	-		-		ns	-
		Hold time	-				ns	
	Rise time, Fall time		-				ns	-
DE	Horizontal	Cycle	th	16.542	20.676	26.88	us	48.363kHz (typ.)
				1114	1344	1400	CLK	
		Display period	thd		1024		CLK	-
	Vertical (One frame)	Cycle	tv	13.34	16.666	20.0	ms	60.0Hz (typ.)
				780	806	845	H	
		Display period	tvd		768		H	
	CLK-DE	Setup time	-		-		ns	-
		Hold time	-				ns	
	Rise time, Fall time		-				ns	-

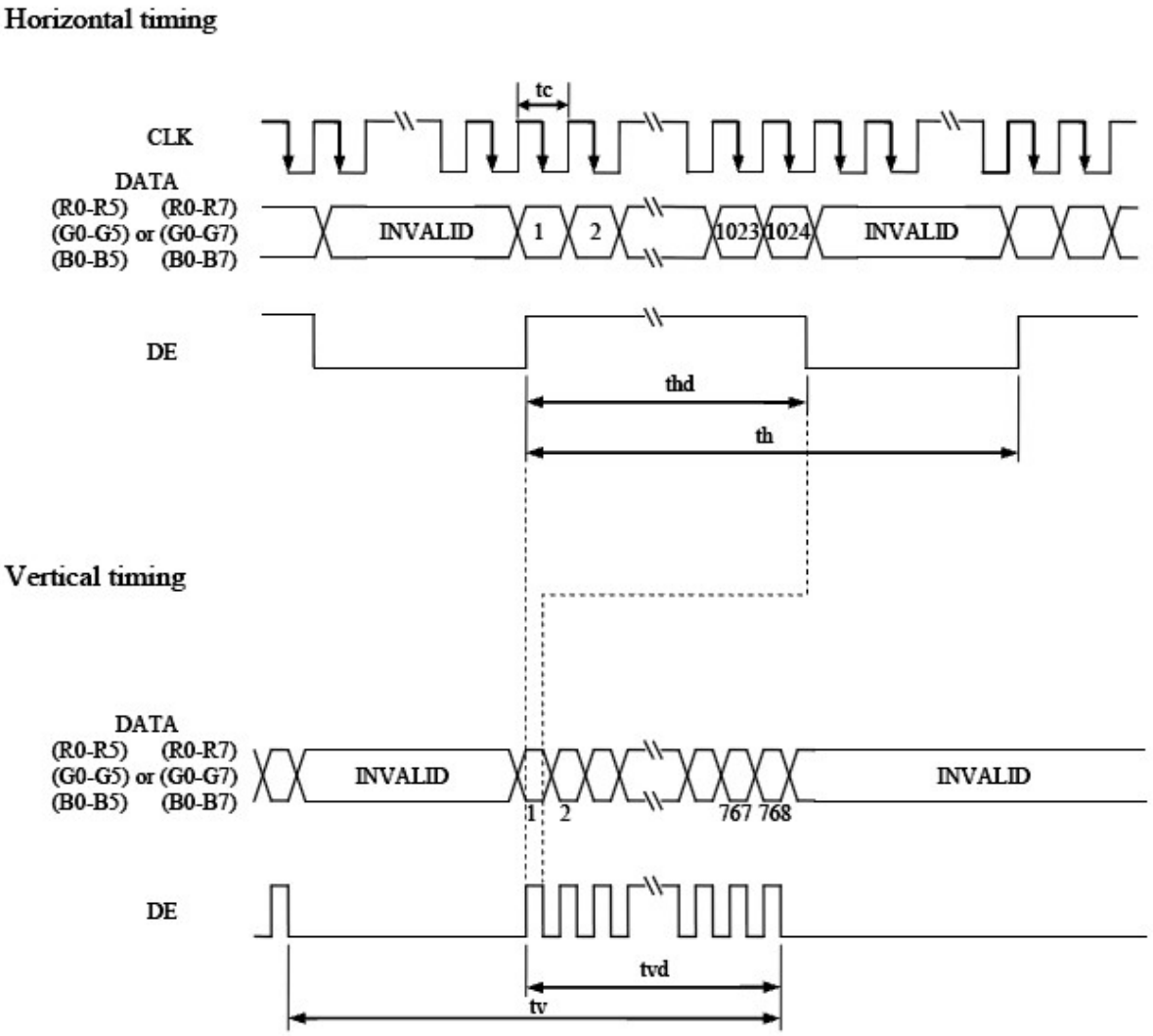
Note1:Definition of parameter is as follows.

tc = 1CLK，th = 1H

Note2:See the data sheet of LVDS transmitter.

Note3:Vertical cycle (tv) should be specified in integral multiple of Horizontal cycle (th).

6.3 Input signal timing chart



7. Optical Characteristics

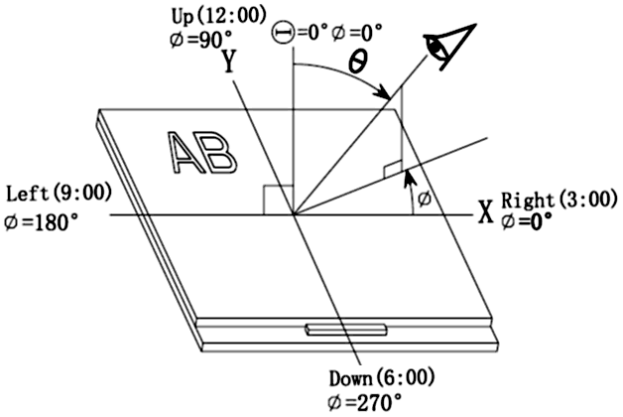
(Note*1,*2)

Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks
Luminance		White at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	L	300	450	-	cd/m2	BM-5A	-
Contrast ratio		White/Black at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	CR	500	700	-	-	BM-5A	Note3
Luminance uniformity		White θR= 0°, θL= 0°, θU= 0°, θD= 0°	LU	-	1.25	(1.33)	-	BM-5A	Note6
Chromaticity	White	**x** coordinate	Wx	0.263	0.313	0.363	-	SR-3	Note5
		y coordinate	Wy	0.279	0.329	0.379	-		
	Red	**x** coordinate	Rx	-	TBD	-	-		
		y coordinate	Ry	-	TBD	-	-		
	Green	**x** coordinate	Gx	-	TBD	-	-		
		y coordinate	Gy	-	TBD	-	-		
	Blue	**x** coordinate	Bx	-	TBD	-	-		
		y coordinate	By	-	TBD	-	-		
Color gamut		θR= 0°, θL= 0°, θU= 0°, θD= 0° at center, against NTSC color space	C	48	55	-	%		
Response time		White to Black	Ton	-	(3)	(5)	ms	BM-5A -10000	Note4
		Black to White	Toff	-	(5)	(8)	ms		
Viewing angle	Right	θU= 0°, θD= 0°, CR≥ 10	θR	70	80	-	°	EZ Contrast	Note2
	Left	θU= 0°, θD= 0°, CR≥ 10	θL	70	80	-	°		
	Up	θR= 0°, θL= 0°, CR≥ 10	θU	70	80	-	°		
	Down	θR= 0°, θL= 0°, CR≥ 10	θD	70	80	-	°		

Note:
*1. The value above are initial Characteristics.
* 2: Measurement conditions are as follows.
Ta= 25℃, VCC= 3.3V, VDD= 12.0V, PWM duty ratio: 100%,
Display mode: XGA, Horizontal cycle= 1/48.363kHz, Vertical cycle= 1/60.0Hz,
DPS= Low or Open: Normal scan, FRC= High

Note 1:
The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment SR-3A (1°)
Measuring condition:
- Measuring surroundings: Dark room
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

Note 2:
The definition of viewing angle:
Refer to the graph below marked by θ and Φ

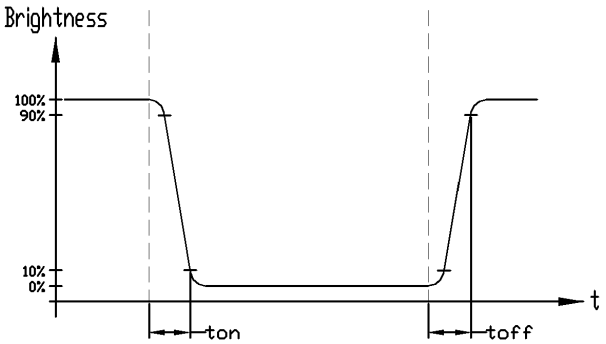


Note 3:
The definition of contrast ratio (Test LCM using SR-3A (1°)):

$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance When LCD is at “White” state}}{\text{Luminance When LCD is at “Black” state}}$$

(Contrast Ratio is measured in optimum common electrode voltage)

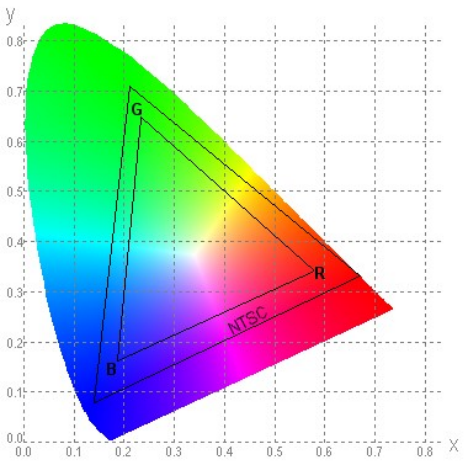
Note 4:
Definition of Response time. (Test LCD using BM-7A(2°)):
The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



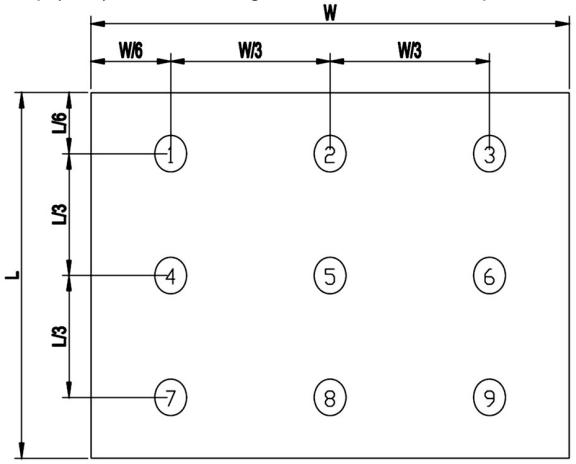
Note 5:
Definition of Color of CIE1931 Coordinate and NTSC Ratio.

Color gamut:

$$S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$



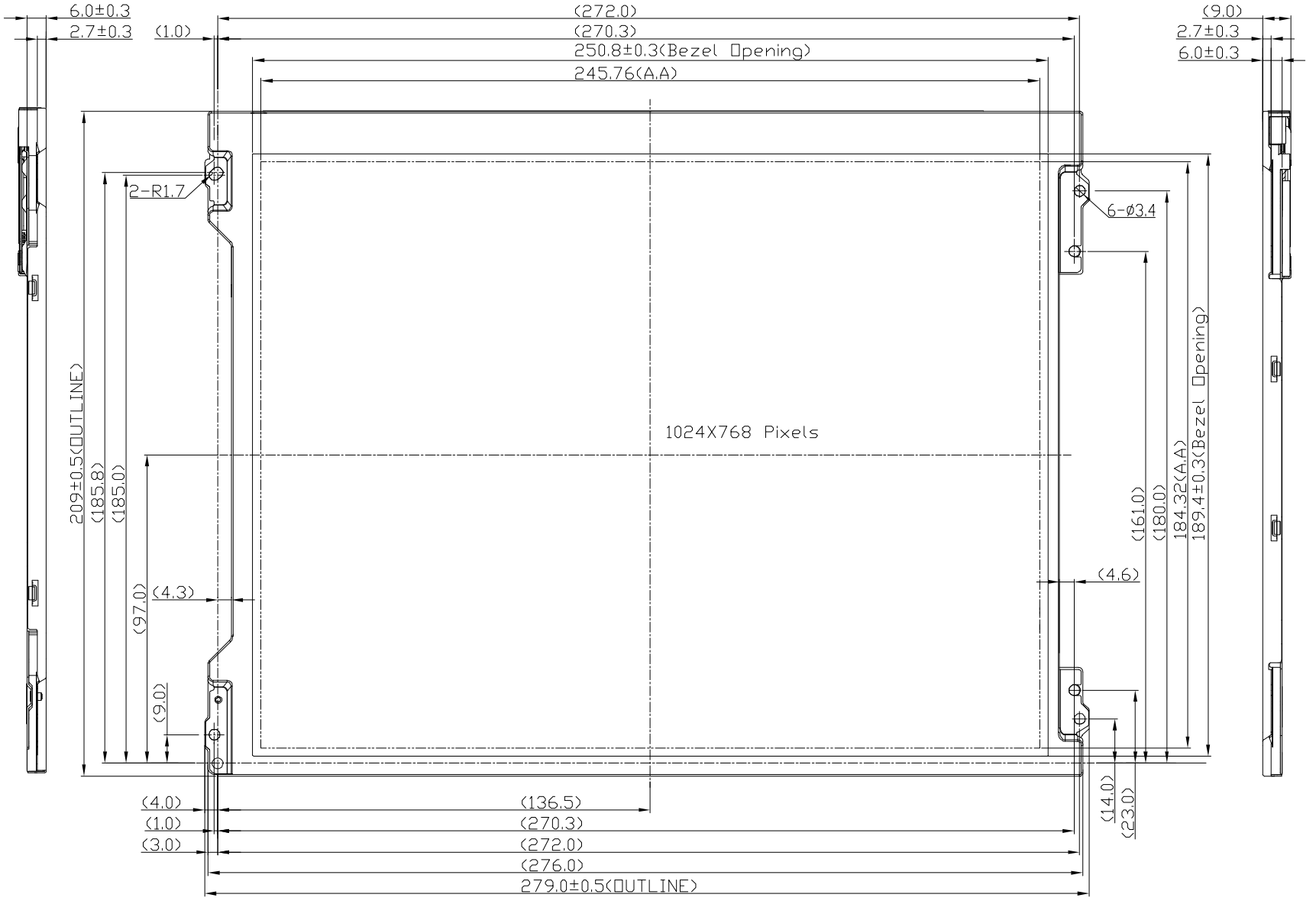
Note 6:
The luminance uniformity is calculated by using following formula.
△Bp = Bp (Min.) / Bp (Max.)×100 (%)
Bp (Max.) = Maximum brightness in 9 measured spots
Bp (Min.) = Minimum brightness in 9 measured spots.



Note 7:
Measured the luminance of white state at center point

8. Precautions of using LCD Modules

Please refer to "LCD-Module-Design-Handling-Precaution.pdf".



K1 Terminal	
No	Pin Name
1	VCC
2	VCC
3	GND
4	FRC
5	RIN0-
6	RIN0+
7	GND
8	RIN1-
9	RIN1+
10	GND
11	RIN2-
12	RIN2+
13	GND
14	CLKIN-
15	CLKIN+
16	GND
17	RIN3-
18	RIN3+
19	DPS
20	NC

K2 Terminal	
No	Pin Name
1	NC
2	BLADJ
3	BLEN
4	BLGND
5	BLVCC

Note:

*1. LCD Display Type: TFT,Transmissive
*2. Pixel Arrangment: RGB-STRIPE
*3. Color Depth : 16.2M(24bit)
*4. Interface : LVDS
*5. Supply Voltage : 3.3V
*6. Backlight Supply : 12.0V Typ.
*7. Backlight : White LED
*8. Operating Temperature : -20°C~70°C
*9. Storage Temperature : -30°C~80°C
*10. Connector type :
K1 connector : STM-MSB240420HE or equivalent
K2 connector : STM-MSB24038P5 or equivalent

Rev	Note	Date
B		
A		

Dwg Title: LMT121DNGFWD Outline Dwg

Dwg No.: MK-005034-2-1

Date: 2014-11-13

Scale: 3/5 | Tol.: ±0.5 | Unit: mm | Paper Size: A3

Approved | Checked | Drawn: Deng Junjie

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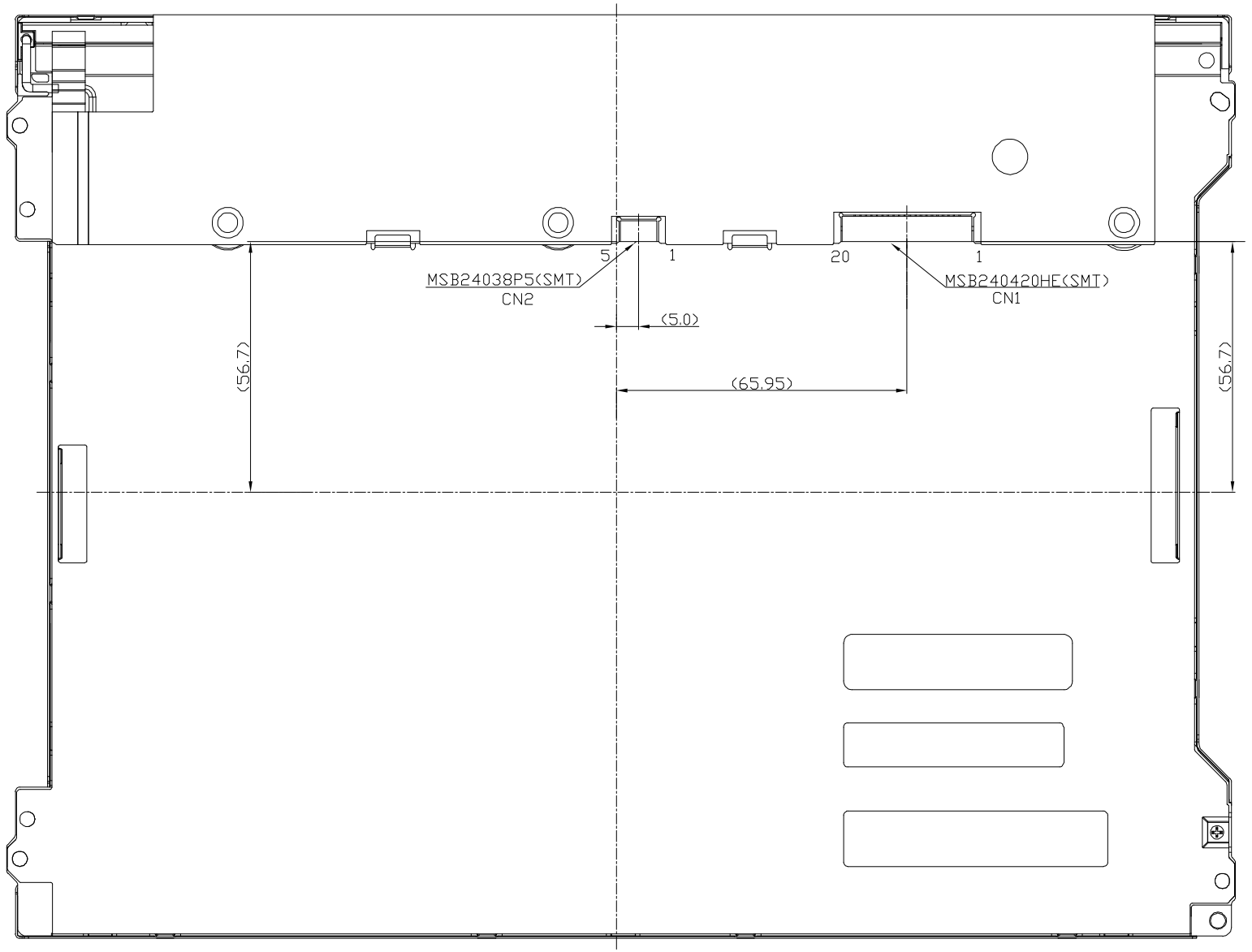

C		
B		
A		
Rev	Note	Date

Dwg Title	LMT121DNGFWD Outline Dwg			
Dwg No.	MK-005034-2-2			Date 2014-11-13
Scale 3/5	Tol. ±0.5	Unit mm	Paper Size A3	
Approved		Checked	Drawn Deng Junjie	

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