SGS-THOMSON MICROELECTRONICS

ST7282A5 - ST7282B5

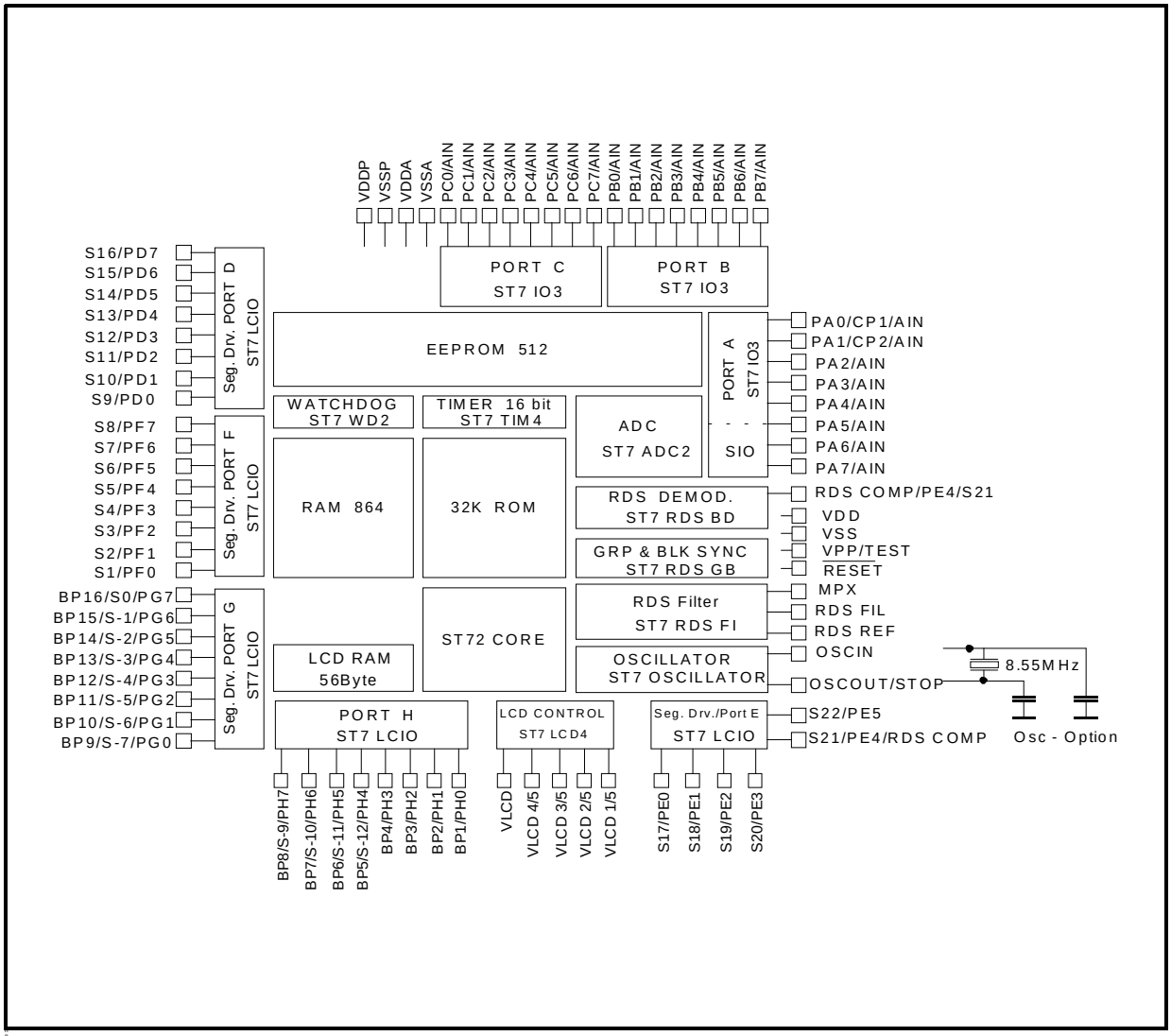
ROM FROM EPROM

PRELIMINARY DATASHEET

- ST72-Core
- Controller/Driver for max. 20 × 16, 28 × 8 or 32 × 4
- LCD segments (ST7LCD4)
- 56 bytes LCD-RAM
- 864 bytes data RAM
- 512 bytes EEPROM (eep2a)
- 32Kbytes program ROM
- 24 digital I/O (ST7 IO3) with pull up, interrupt input, analog input, push-pull/ open drain output
- 36 LCD/IO combi pins (ST7 LCIO1) with pull-up, interrupt input, push-pull, open drain output, LCD output
- 16 bit reload timer (ST7TIM4)
- Watchdog Timer (ST7 WD2)
- 8 bit synchronous serial I/O (ST7SIO)
- 8 bit A/D Converter (ST7ADC2)
- RDS Demodulator (ST7 RDS BD)
- Group & Block Sync Module for RDS (ST7 RDS GB)
- RDS filter (ST7 RDS FI)
- LCD Synchro IN / Out
- System Frequency 8.55 MHz

1 GENERAL DESCRIPTION

Figure 1. Block Diagram



1.1 Quick Reference

The ST7282A5/B5 is a 32K ROM version of the ST72 family, using the ST72CORE and N-Well technology.

It is derived from EPROM M4 version replacing EPROM by ROM.

Two different commercial products are supported by this device : ST7282A5 (no LCD driver) functionnality described in specification SD70KL1618 ed. F) and ST7282B5 (LCD driver) functionnality described in specification 96096 ed. B).

It contains an LCD controller/driver with 20 segment and 16 backplane outputs able to drive up to 20 x 16 = 320 segments.

The LCD control logic reads automatically data from the LCD-RAM independently from the ST7282 B5.

Further it contains up to 62 I/O pins, 24 of them can be used as analog inputs to the 8 bit analog-digital converter. Each digital I/O pin can individually be defined by software to work in one of the following modes: open-drain output, push pull output, input, input with pull-up (23 pins only) or interrupt input with pull up (23 pins only). 3 of the digital I/O pins serve as interface to the SIO. On pin PA4 the pull-up resistor is desactivated.

Port pins PD, PE, PF, PG and PH are multiplexed with LCD Segment and backplane pins.

A 512 byte EEPROM for non volatile storage of data is available. The programming voltage for that device is generated on chip without external components. So no extra supply is necessary. 16 bytes are protected against external readout.

One interrupt vector is connected to the I/O ports. Five more interrupt vectors are available for the timer, the ADC, the serial I/O interface and the Group & Block Sync module (2). The watchdog can be set by the user in 64 increments from 2.8msec to 182msec (f_{OSC} = 8.55 MHz).

A synchronous 8 bit serial interface for serial data IN/OUT is also implemented.

RDS signals can be decoded with the help of RDS filter, RDS demodulator and Group & Block Sync module.

1.2 Parameters

The values below substitute the corresponding values in the specifications of dedicated functions.

1.2.1 Absolute maximum ratings

Supply voltage	**(V_{DD} - V_{SS})**	**-0.3 ... +7V**
Input voltage*	**V_{IN}**	**V_{SS}-0.3V...V_{DD}+0.3V**
Output voltage*	**V_{OUT}**	**V_{SS}-0.3V ... V_{DD}+0.3V**
Input current	**I_{in}**	**-10 ... +10mA**
Output current*	**I_{OUT}**	**-10 ... + 10mA**
Power dissipation	**P_D**	**tbd**
Storage temperature	**T_{stg}**	**-55 ... +125°C**
Operation temperature	**T_{amb}**	**-40 ... +85°C**
Display voltage	**(V_{LCD} - V_{SS})**	**V_{DD} ... 7V**
Output voltage Seg+COM	**V_{OUT}**	**V_{SS}-0.3V ... V_{LCD}+0.3V**
ESD	**ESD**	**2500V**
LU susceptibility	**LU**	**V_{DDA}, Pin 52 - Class C**

1.2.2 Recommended operating conditions

Supply voltage	(V_{DD} - V_{SS})	4.5 ... 5.5V
Supply votage difference	(V_{DD}, V_{DDP}, V_{DDA}) (V_{SS}, V_{SSP}, V_{SSA})	50mV

The maximum accumulated current of all I/O pins should not exceed 40 mA for V_{DDP} and 40 mA for V_{SSP}.

* except LCD pins

** MIL 883B Mode, 100pF through 1.5k

1.2.3 Electrical Characteristics

The values given in the specifications of dedicated functions are generally not applicable for chips. Therefore, only the limits listed below are valid for the product. T = -40 ... +85°C, V_{DD} - V_{SS} = 5V unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply voltage	V_{DD}		4.5	-	5.5	V
Supply current Run Mode	I_{DD}	f_{OSC}=8.55MHz no output load	-	10	20	mA
Supply current Wait Mode	I_{DD}	f_{OSC}=8.55MHz WD, Timer, LCD active	-	3	5	mA
Supply current slow wait mode	I_{DD}	no output load	-	0.7	2	mA
Supply current halt mode	I_{DD}	no output load	-	-	100	µA
Supply current Reset Mode	I_{DD}	V_{RESET}=V_{SS} f=8.55MHz	-	10	15	mA
Display voltage	V_{LCD}		V_{DD}	-	7	V
Supply voltage differences (V_{DD}, V_{DDP}, V_{DDA}) (V_{SS}, V_{SSP}, V_{SSA})	V_D		-	-	50	mV
OSCILLATOR: Input/output cap Cin, Cout Oscillation frequency [1] Built up time [2]	 f_{OSC} t_{BU}	 V_{DD} = 4.5V V_{DD}=5.0V C_1=C_2=22pF	 8.55 -	 8.55 8	 9.00 8.55 20	 pF MHz ms
RESET: Input current [3] Input current [4] Input current [5] Input voltage high Input voltage low	 -I_R I_R I_R V_R V_R	Crystal V_R=V_{SS} V_R=V_{DD} V_R=V_{DD}	 - - - 0.7V_{DD}	 +50 +10 - - -	 +100 +20 1 - 0.2V_{DD}	 µA µA mA V V
POWER-ON RESET Supply rise time Supply recovery time [6] Trigger level on Trigger level off	 t_r t_{rec} V_{tlon} V_{tloff}	 10%-90%	 .01 10 1.4 -	 - - .- -	 10 - - 3	 ms ms V V
RDS FILTER: Center frequency 3dB Bandwith Gain Attenuation Input impedance Load impedance MPX input signal	 fc BW G A R_I R_L V_{IN}	 V_{in} = 3mV_{RMS} 57 KHz, V_{in} = 3mV_{RMS} Δf = ±4 KHz f = 38 KHz f = 67 KHz	 56.5 2.5 18 18 50 35 100 1 170	 57 3 20 22 80 50 160 - 250	 57.5 3.5 22 - - - 200 - 600	 KHz KHz dB dB dB dB KΩ MΩ mV_{RMS}

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
I/O PORTS:						
Input leakage current [7]	I_{IL}	$V=V_{SS}$	-	-	10	µA
Input leakage current	I_{IH}	$V=V_{DD}$	-	-	10	µA
Input voltage high	V_{IH}	leading edge	$0.7V_{DD}$	-	-	V
Input voltage low	V_{IL}	trailing edge	-	-	$0.2V_{DD}$	V
Output voltage high	V_{OH}	I=5mA, V_{DD}=4.5V	3.0	-	-	V
(PA,PB,PC)	V_{OH}	I=1.0mA, V_{DD}=4.5V	4.1	-	-	V
Output voltage high	V_{OH}	I=2.5mA, V_{DD}=4.5V	3.0	-	-	V
(PD, PE, PF, PG, PH)	V_{OH}	I=0.5mA, V_{DD}=4.5V	4.1	-	-	V
Output voltage low	V_{OL}	I=-5mA, V_{DD}=4.5V	-	-	1.0	V
(PA, PB, PC, PD, PE, PF, PG, PH)	V_{OL}	I=-1.6mA, V_{DD}=4.5V	-	-	0.4	V
Output voltage slope	dV_O/dt	C_L=50pF	-	0.25	-	V/ns
Output current slope	dI_O/dt	C_L=50pF	-	2.5	-	mA/ns
Noise amplitude	V_N	20MHz-250MHz	-	100	-	µV
		$V_{IN}=V_{SS}$	-	-	-	-
Pullup Resistor Current	I_{RPU}		-	50	-	µA
ADC:						
Resolution	V_{A1}	f_{OSC}=8.55MHz [8]		-	-	bit
Total Error		f_{OSC}=8.55MHz [8]		-	±2	LSB
Conversion time	t_{con}	f_{OSC}=8.55MHz		34	35	µs
Input capacitance				-	5	pF
Analog source impedance	R_{VA}			-	30	KΩ
Osc. frequency range				8.55	-	MHz
LCD DRIVER:						
Frame frequency	f_F	f_{OSC}=8.55MHz		-	132	Hz
DC offset voltage [9]	V_{OS}	$V_{LCD}=V_{DD}$, no load		-	50	mV
COM output voltage high	V_{OH}	I=50µA		-	-	V
COM output voltage low	V_{OL}	I=50µA		-	0.5	V
SEG output voltage high	V_{OH}	I=25µA		-	-	V
SEG output voltage low	V_{OL}	I=25µA		-	0.5	V
EEPROM:						
Write time	t_W	V_{DD}=4.5V		-	10	ms

1)Operation below 30 KHz Mis possible but requires increased supply current

2)Time to build up the oscillation amplitude to 90% V_{DD}

3)Pull-up resistor

4)WD not active

5)WD generating a reset

6)Period for which V_{DD} has to be disconnected or at OV to allow internal reset function at next power up

7)pull up off

8) noise at V_{DD}, V_{SS} < 10 mV

9)The DC offset voltage refers to all segment and common outputs. It is the difference between the measured voltage value and nominal voltage value for every voltage level. Rin of voltage meter must be > 10 MΩ.

1.3 ST7282A5/B5 ADDRESS MAPPING

ADDR.	USER
$0000	Port A Data Reg.
$0001	Port A Data Direction Reg.
$0002	Port A Option Reg.
$0003	Port A Pin status
$0004	Port B Data Reg.
$0005	Port B Data Direction Reg.
$0006	Port B Option Reg.
$0007	Port B Pin status
$0008	Port C Data Reg.
$0009	Port C Data Direction Reg.
$000A	Port C Option Reg.
$000B	Port C Pin status
$000C	Port D Data Reg.
$000D	Port D Data Direction Reg.
$000E	Port D Option Reg.
$000F	Port D Pin status
$0010	ADC Control Reg.
$0011	ADC Data Reg.
$0012	Watchdog Reg.
$0013	LCD Ctrl. 1
$0014	EECR1
$0015	EECR2
$0016	SIO Data Reg.
$0017	SIO Interrupt Disable
$0018	Timer Reg. 1
$0019	Timer Reg. 2
$001A	Timer Reg. 3
$001B	Timer Reg. 4
$001C	Timer Reg. 5
$001D)	(Not to be used **
--------)	(-----
$0023)	(from $001D to $0023

$0024 $0025 $0026 $0027	CRC Test Reg. (ST use) CRC Test Reg. (ST use) Misc. Reg. LCD Ctrl. 2
$0028 $0029 $002A $002B $002C $002D $002E $002F	reserved reserved Filter Reg. 1 Filter Reg. 2 RDS_R0 RDS_R1 RDS_R2 reserved
$0030 $0031 $0032 $0033 $0034 $0035 $0036 $0037	RDS_BD_H RDS_BD_L RDS_CORRP RDS_QU RDS_INT reserved reserved reserved
$0038 $0039 $003A $003B $003C $003D $003E $003F	reserved reserved reserved reserved reserved reserved reserved reserved
$0040 ----- $0047	LCD RAM 8 Byte MUX8 SEG.-7-0 = Byte 40 ... 47 BP1 ... BP8 = Bit0 ... Bit7
$0048 ----- $005F	LCD RAM 24 Byte MUX8,11,16 SEG. 1 - 24 = Byte 48 ... 5F BP1 ... BP8 = Bit0 ... Bit7

$0060 ----- $0063	LCD RAM 4 Byte Mux 4 Seg -8, -9, -10, -11 BP1 ... BP4 = Bit0 ... Bit3
$0064 $0065 $0066 $0067	LCD RAM not used for display
$0068 ----- $007F	LCD RAM 24 Byte MUX 11, 16 SEG. 1-24 = Byte 68 ... 7F BP9 ... BP16 = Bit0 ... Bit7
$0080 ----- $008F	reserved
$0090 $0091 $0092 $0093	Port E Data Register Port E Data Direction Register Port E Option Register Port E Pin Status
$0094 $0095 $0096 $0097	Port F Data Register Port F Data Direction Register Port F Option Register Port F Pin Status
$0098 $0099 $009A $009B	Port G Data Register Port G Data Direction Register Port G Option Register Port G Pin Status
$009C $009D $009E $009F	Port H Data Register Port H Data Direction Register Port H Option Register Port H Pin Status
$00A0 ----- $03FF	RAM 864 Stack = 300-3FF

$0400 ----- $0DFF	reserved
$0E00 ----- $0E0F	EEPROM read out protected
$0E10 ----- $0FFF	EEPROM 512
$1000 ----- $1FFF	not available (test area)
$2000 ----- $7FFF	reserved
$8000 ----- $FFDF	ROM 32k
$FFE0 ----- $FFEF	reserved (ST Routram area)
$FFF0 ----- $FFFF	user vectors

“Not to be used” is mandatory. Any access would modify the functionality.

2 IMPLEMENTATION REMARKS OF THE DEDICATIONS

In this chapter the options of the dedications, which are implemented are described. The dedications are described in detail in the target specs of the dedications. In case of discrepancies between this specification and the specs. of the dedications, this specification is valid.

2.1 Core

2.1.1 Oscillator

The oscillator can be used with quartz or ceramic resonator. The pins OSCIN and OSCOUT permit connection to the on chip clock oscillator circuit. OSCIN is the input, OSCOUT the clock oscillator output. A quartz or a ceramic resonator can be connected to these pins. Two external ceramic capacitors of 22pF connect the oscillator pins to ground. Also an external system clock can be applied to the oscillator input OSCIN.

2.1.2 External reset input RESET

Low level active external reset input with Schmitt-Trigger characteristic. A pull-up resistor of typically 300kΩ (200kΩ - 500kΩ) is integrated. This pin is resetting the I/O ports immediately without any need of a clock.

2.1.3 Stack

The Stack is located at 3FFH and may go down to 300H.

2.1.4 Interrupts

I1 is connected to IOPorts A ... H (start address FFFAH)

I2 is connected to RDS GRP & BLK SYNC (block interrupt) (start address FFF8H)

I3 is connected to SIO (start address FFF6H)

I4 is connected to Timer (start address FFF4H)

I5 is connected to ADC (start address FFF2H)

I6 is connected to RDS GRP & BLK SYNC (bit interrupt) (start address FFF0H)

If more then 1 input pin of a group, connected to the same interrupt, is selected as interrupt input with pullup, all selected inputs are "AND" connected.

WARNING :

Read modify write instructions may clear interrupt flags of dedications unintentionally if the interrupt flag is set after the read and before the write. Operations on control registers of dedications should be done with sufficient timing distance to interrupt events.

2.1.5 Miscellaneous register(0026h)

Read/Write

Reset Value: 0000 0000 (00h)

This register is a various 8-Bit register where only 3 bits are used for interrupt and slow mode.

– b6 = INTP: Interrupt Positive allows to select the I1 line triggering mode in conjunction with INTN. It can only be modified when the I bit of the CCR is set.

– b5 = INTN: Interrupt Negative allows to select the I1 line triggering mode in conjunction with INTP. It can only be modified when the I bit of the CCR is set.

– b1 = SM: Slow Mode. Setting this bit to "1" enables Slow Mode, thus reducing power consumption. In this mode, an extra divider by 64 is added in the clock circuitry. In Halt Mode SM bit is automatically reset.Registers of all RDS-Modules should not be accessed during slow mode.

Figure 2. External Interrupt Options

INTP	INTN	I1 External Interrupt Options
0	0	Negative edge and Low level sensitive
0	1	Negative edge only
1	0	Positive edge only
1	1	Positive and negative edge sensitive

2.2 LCD controller/driver

The LCD module contains an LCD controller/driver with 20 segment and 16 backplane outputs able to drive up to 20 x 16 = 320 segments. The LCD control logic reads automatically data from the LCD-RAM independently from the ST72 core.

Two signals (LCF32K,LCSYNCHINOUT) can be activated on pins PC0, PC1 to connect a slave display chip for expanding the number of segments. To activate these pins as LCF32K, LCSYNCHINOUT, bit0 of register LCD Ctrl.2 (0027H) has to be set. During reset this bit is cleared.

V_{LCD} must never be below V_{DD}.

2.2.1 Address mapping of the picture elements

The LCD-RAM is located in the address region of the ST72 data space from address 40H - 7FH.

The LCD forms a matrix of 20 segment lines (columns) and 16 backplane lines (rows). Each bit of the LCD-RAM is mapped to one dot of the LCD matrix according to fig. 1. If a bit is set, the corresponding LCD segment is switched on, if it is reset, the segment is switched off.

After reset, the LCD-RAM is not initialized and contains arbitrary information. As the LCD control register is cleared, the LCD is completely switched off.

In halt mode no clock for the LCD module is available from the main oscillator. The LCD module is switched off in halt mode.

The input frequency of the LCD controller is $f_{OSC}/2$ (4.275MHz).

A 32kHz stand by oscillator is not available. Therefore the mode FEXT (C_5, C_4, C_3 = 001) of LCD control register cannot be used.

In any case a missing LCD clock (no oscillator active, broken crystal etc.) is detected by a clock supervisor circuit which switches all segment and common lines to ground to avoid destructive DC levels at the LCD.

If the LCD clock is not missing but far too slow (e.g. due to incorrect setting of C_5, C_4, C_3 in LCD control register) the LCD is switched off periodically. This situation has to be avoided.

A division factor of +256 is recommended for the prescaler (C_5, C_4, C_3 = 110; f_{OUT} = 16.699KHz). With this setting of the predevider, frame frequencies of 132.2Hz, 66.1Hz, 44.1Hz and 33.1Hz can be generated.

The frequency out of the prescaler must not be below 15KHz in order not to switch off the display through the LCD oscillator supervisor.

To activate segments and backplanes, data and option register bits of the corresponding combiport pins have to be set to 1. During reset data and option register bits of combiports are set to 1.

2.2.2 External Divider Chain

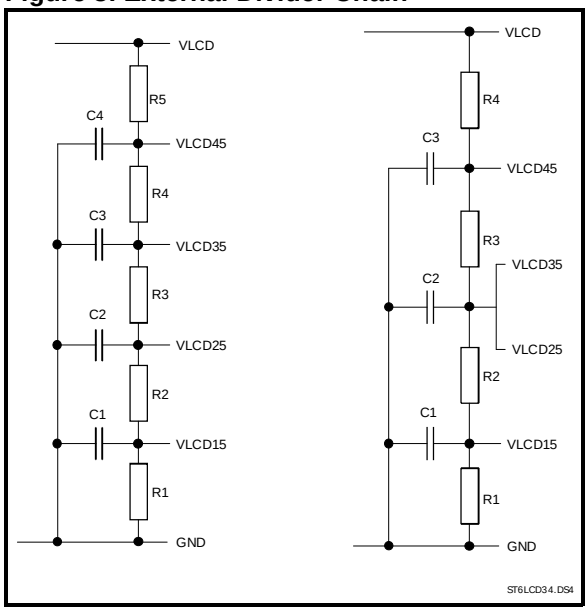
The different display voltage levels are supplied by an external resistor chain as shown in fig. below.

Two different configurations with five or four display voltage levels can be chosen.

The resistors have to have a good matching within < 1% to avoid DC voltage levels on the liquid crystal device.

DC levels trigger electrode reactions on the liquid crystal cell, deteriorating display quality rapidly.

Figure 3. External Divider Chain

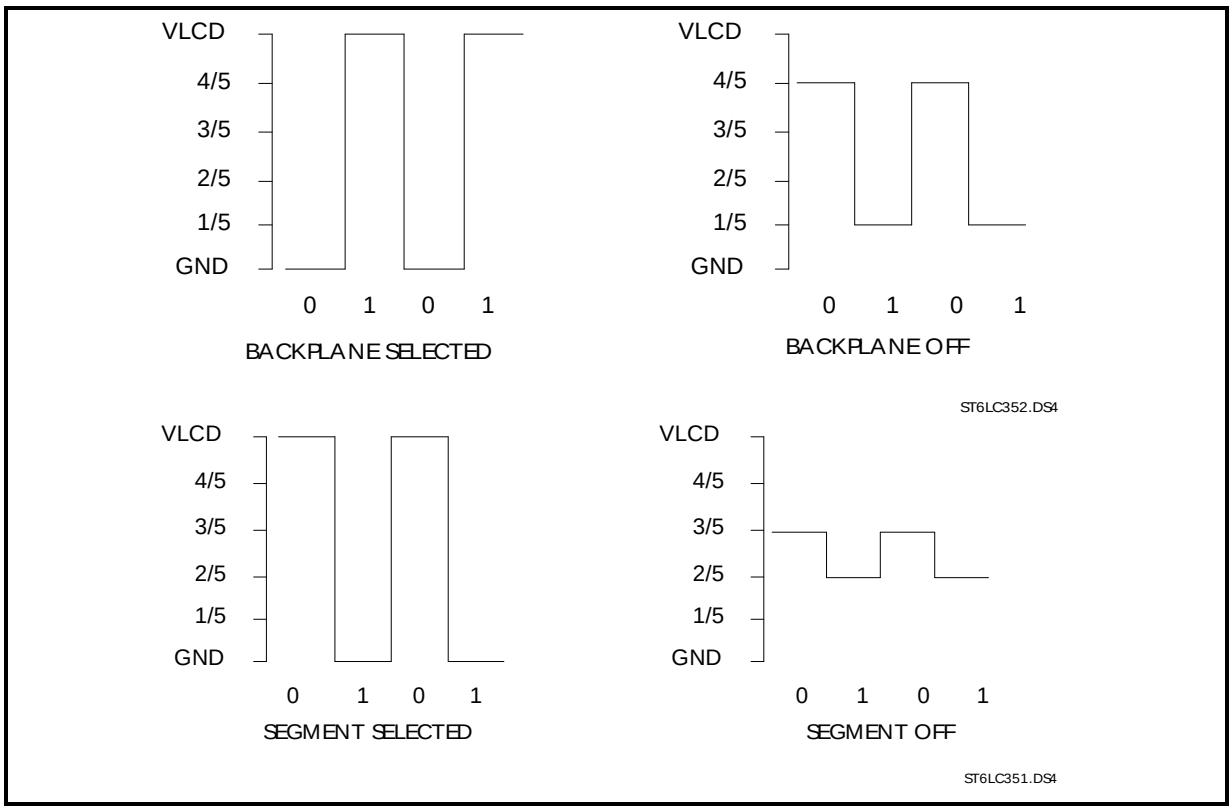


$C_1 = C_2 = C_3 = C_4 = 0.1 \ldots 0.3\mu F$

$R_1 = R_2 = R_3 = R_4 = R_5 = 1 \ldots 200k\Omega$

2.2.2.1 Working with 1/5 Bias

Figure 4. Waveform on common and on segment output working with 1/5 Bias



2.2.2.2 Working with 1/4 Bias

Depending on the selected display material, the operating mode and the display voltage V_{LCD}, it is possible to reduce the LCD resistor chain to 4 resistors, and operate with the 1/4 bias method.

If VLCD35 and VLCD25 are connected to the same voltage, the segment and backplane drivers will work in the same way as with 1/5 bias, but the resulting waveforms will look a bit different :

Figure 5. Waveform on common and on segment output working with Bias 1/4

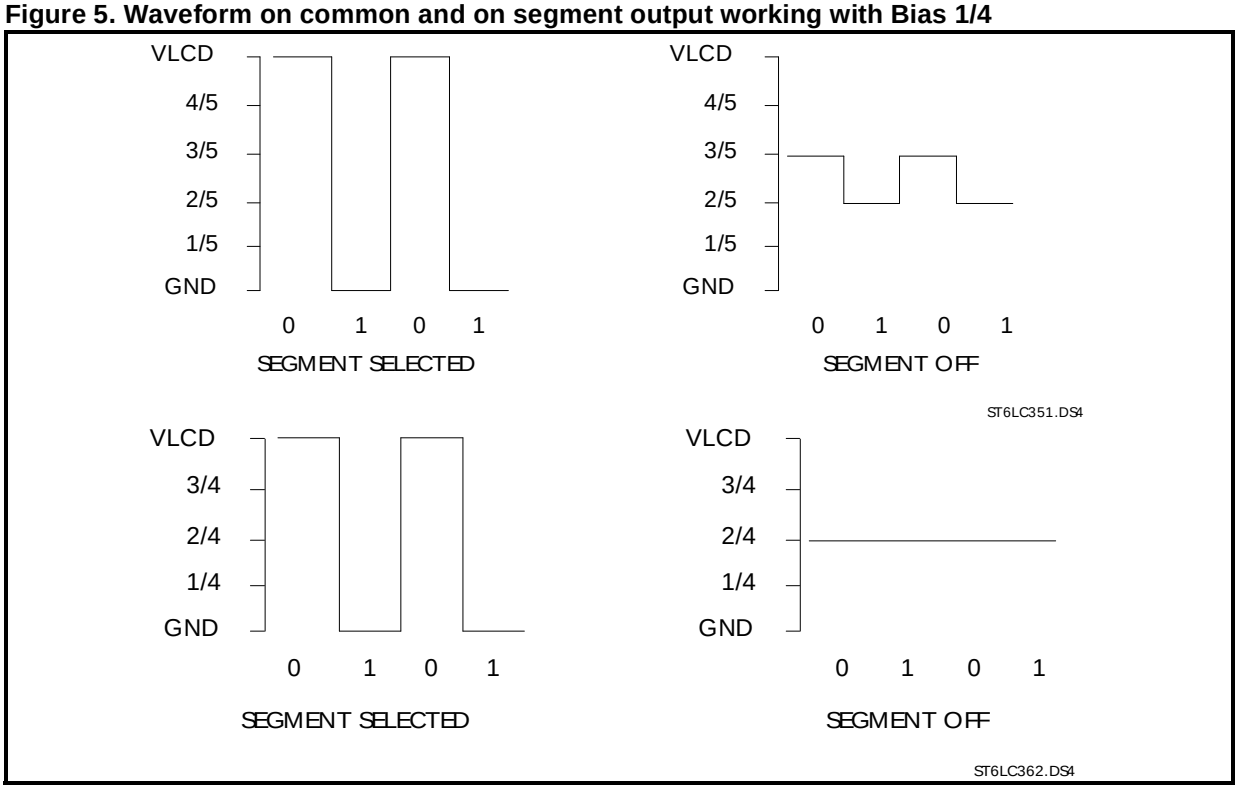


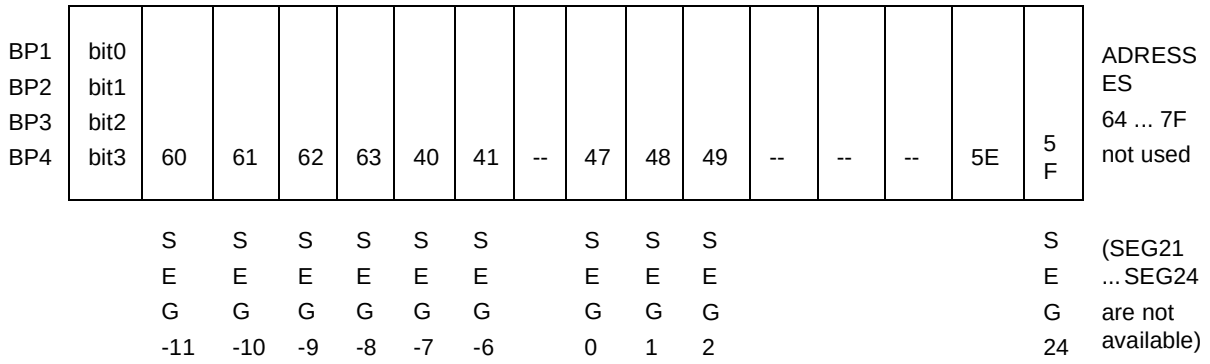
Figure 6. Address Mapping of the LCD-RAM MUX16

BP1	bit0												
BP2	bit1												
BP3	bit2												ADRESSES
BP4	bit3	48	49	--	4F	50	--	--	--	--	5E	5F	40 ... 47
BP5	bit4												and 60 ... 67
BP6	bit5												not used
BP7	bit6												
BP8	bit7												
BP1	bit0												
BP2	bit1												
BP3	bit2												
BP4	bit3	68	69	--	6F	70	--	7B	--	--	7E	7F	
BP5	bit4												
BP6	bit5												
BP7	bit6												
BP8	bit7												
		SEG1	SEG2		SEG8	SEG8		SEG20				SEG24	(SEG21 ... SEG24 are not available)

Figure 7. Address Mapping of the LCD-RAM MUX8

BP1	bit0												
BP2	bit1												
BP3	bit2												ADRESSES
BP4	bit3	40	41	--	47	48	49	--	--	--	--	5E	5F	60 ... 7F
BP5	bit4													not used
BP6	bit5													
BP7	bit6													
BP8	bit7													
		SEG-7	SEG-6		SEG0	SEG1	SEG2						SEG24	(SEG21 ... SEG24 are not available)

Figure 8. Address Mapping of the LCD-RAM MUX4



2.3 TIMER 4

16 bit autoreload timer with 2 capture inputs connected to PA0, PA1 (see spec. ST7TIM4). The input clock of the timer is fosc divided by 2.

2.4 WATCHDOG

The WD2 is used to reset the ST7282 B5 after a certain period of time in the range of 2.8 msec up to 184 msec when f_{OSC} = 8.55 MHz is used.

WD2 will be activated, if bit0 in Watchdog Reg. (Adr. 12h) is set ("1"). Once WD2 is running, any software access to bit0 in Watchdog Reg. will NOT influence WD2. However, a RESET signal (either externally or caused by WD2) will reset bit0 of Watchdog Reg.

After a RESET, WD2 is deactivated and set to it's longest period (184 msec for f_{OSC} = 8.55 MHz).

WD2 is able to produce a SW-Reset (bit0 set to "1", bit1 to "0").

Dedication address of WD2 is 12h .

If WD2 is enabled, any stop instruction will generate a reset. However, the use of a stop instruction (HALT) is not recommended in this case.

2.5 I/O PORTS

Pins PD0 ... PD7, PE0 ... PE3, PF0 ... PF7, PG0 ... PG7 and PH0 ... PH7 are of type LCIO.

Pins PA0 ... PA7, PB0 ... PB7 and PC0 ... PC7 are of type IO3 and can also be used as analog inputs.

The interrupt outputs of PORT A, PORT B, PORT C, PORT D, PORT E, PORT F, PORT G and PORT H are anded and connected to the interrupt input I1 of core (start address FFFAH). So every port pin which is programmed as an input with interrupt enabled can generate an interrupt. If more than one port pin is programmed as an interrupt input, overlapping interrupts cannot be detected due to the AND function.

PA0, PA1 are also used as CP1, CP2 inputs of TIMER 4.

The pins PA5 ... PA7 are also used by the serial I/O (see fig. 2). PA5 is connected with SCL (clock input), PA6 is connected with SDA (data input) and PA7 is connected with DOUT (data output) of the SIO.

For serial input operation PA5 and PA6 have to be programmed as inputs. For serial output PA7 has to be programmed as open drain output (DDR = 1, OPR = 0). In this operation mode the output of the SIO shift register instead of the port data register is connected to the port buffer. When PA7 is programmed as push pull output (DDR = 1, OPR = 1), the port data register is connected to the port buffer.

When the SIO pins are not used PA5 ... PA7 can be used as any other I/O pin (PA7 not in open drain output mode).

After reset ports PA0 ... PA7, PB0 ... PB7 and PC0 ... PC6 are in input mode with pull up resistors switched on and interrupt disabled.

PA4 does not have a pull-up resistor.

Ports PD0 ... PD7, PE0 ... PE3, PF0 ... PF7, PG0 ... PG7 and PH0 ... PH7 are in the "LCD Output mode" (all pins switched to V_{SS}).

PC7 is switched to analog input mode during reset (data register and option register bits are set).

PC0, PC1 may optionally be used to "cascade" the LCD (refer to: 2. LCD CONTROLLER/DRIVER).

2.6 ADC

The reference voltage inputs of the ADC1N are connected to V_{DDA}, V_{SSA}. Therefore special care has to be taken to stabilize V_{DDA}, V_{SSA} and to avoid switching of I/O pins during conversion. Analog inputs may be multiplexed from pins PA0 ... PA7, PB0 ... PB7 and PC0 ... PC7. Up to 24 analog inputs can be multiplexed.

Selection of an analog input is done by programming the corresponding pin of a port as analog input (DDR = 0, DR = 1, OPR = 1). Be sure that only one port pin is programmed as analog input at a time. Otherwise the analog sources are shorted by the analog multiplexer. Conversion time for an 8.55 MHz clock is 34 µsec (i.e. 288 clocks + 0...6 clocks of f_{OSC}) because the ADC is supplied with a clock signal of f_{OSC} : 6 that is also available during WAIT. The ADC interrupt is connected to level sensitive interrupt input I5 of the core (start address FFF2H). So the interrupt has to be cleared before the interrupt service routine is left.

A stop instruction will stop the clock of the ADC and will switch off its comparator to achieve minimum power consumption. This can also be done by clearing bit 5 (SC) of ADC control register (10H).

A rising edge on EOC-bit sets the interrupt flipflop. To remove the interrupt, a write operation to ADC-Control register has to be executed, to clear the interrupt flipflop. After the reset, the interrupt flipflop is also cleared.

2.7 SERIAL I/O

The 8 bit SIO generates an interrupt after the falling edge of the eight external clock pulse. The interrupt signals to the ST72 to read or write the SIO via an 8 bit register (adr. 26H).

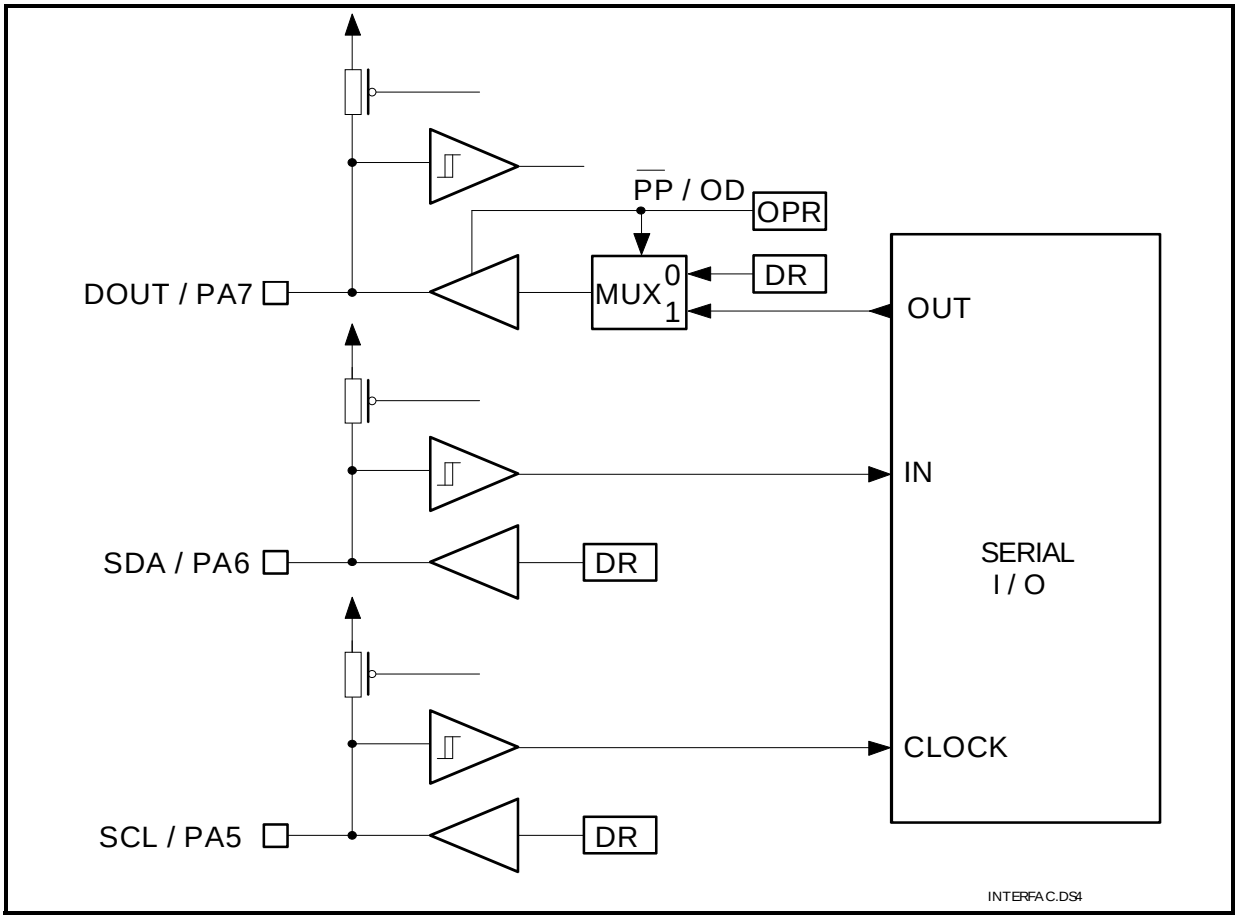
The SIO uses the input/output structure of Port A (PA5 : SCL, PA6 : SDA, PA7 : DOUT) (see fig. 2).

The 3 pins can be operated in the following ways: directly by software, as an S-BUS, as an I^2C-BUS and as a standard SIO (clock, data, enable).

To operate the SIO PA5 and PA6 have to be programmed as inputs, PA7 as open drain output. The SIO interrupt (active low) is connected to the interrupt input I3 of the core (address FFF6H).

After reset all ports are in input mode with pull up resistors switched on and the SIO interrupt is disabled.

Figure 9. Peripheral Interface Configuration of Serial I/O



2.8 RAM

The RAM is located in the address range A0H-3FFH.

300H-3FFH may be used as Stack area.

2.9 EEPROM

The 512 bytes EEPROM is located at addresses 0E00 - 0FFF. 2 cells of 256 bytes each or one cell of 512 bytes may be used. EEPROM control register EECR (adr. 014H) is used to control the different operation modes of the range 0E00H - 0EFFH, EEPROM control register EECR2 (adr. 015H) that of range 0F00H - 0FFFH. Some of its bits are read only, some are write only. So no single bit instructions are allowed.

To avoid destruction of data during power up or down, the reset pin directly desactivates the chargepump of EEPROM cells.

The EEPROM can be used for data storage only, no program execution and no read modify write instructions (single bit, increment, decrement) are possible.

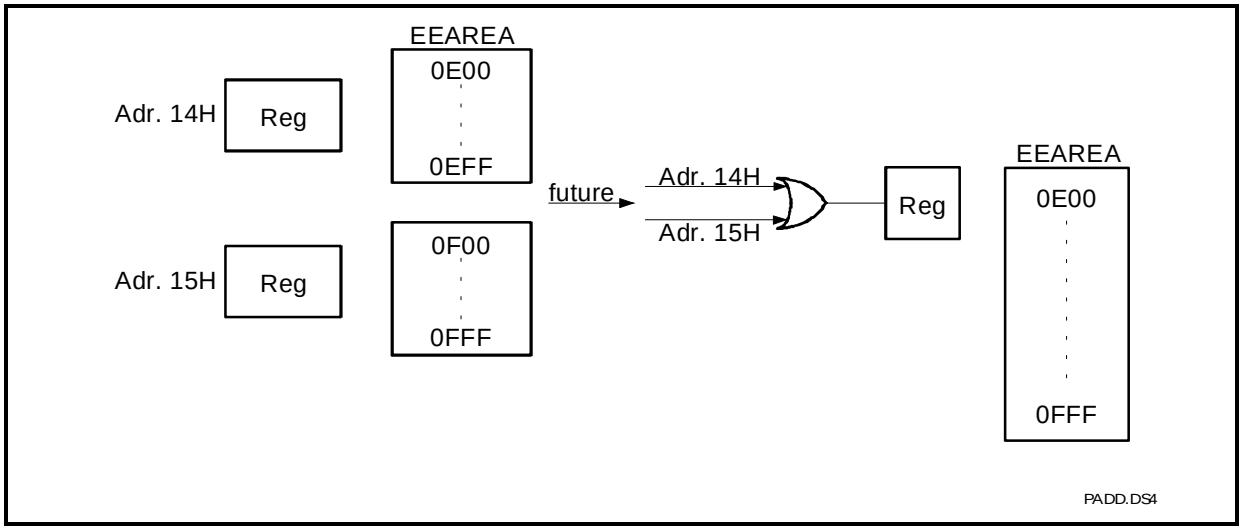
After bit E2LAT of EECR goes to low, there should not be a read operation during the next 20 µsec.

A parallel programming mode for 8 bytes is available. No clear is needed before a write.

Two cells of 256 bytes are used, parallel programming of bytes in each cell is possible. This should be avoided however, to keep software compatitility between all future versions and ROM versions, that have only one physical register, that will be addressed through two different addresses 14H and 15H.

Before access to one area, also the control register of the other area should be checked and access done only, if both areas allow the required access.

SGS-THOMSON may implement a single or double register version in future ROM or EPROM versions.



2.10 32K ROM

The 32K ROM is located at addresses 8000H-FFFFH.

16 bytes (FFE0H - FFEFH) are reserved for SGS-Thomson test vectors.

2.11 RDS

Modules (see separate specs)

Registers of all RDS-Modules should not be accessed (read or write) during slow mode of CPU.

2.12 OSCILLATOR

The ST7 Oscillator allows operation with a crystal or external input. The corresponding mode is defined by a metal option. In case of external input the clock amplitude into OSCI may not be lower then 50mV. The pin OSCO/STOP then is serving as output for the stop signal to synchronize with external clock sources.

In the present version, the device works with a dedicated crystal.

3 TESTING

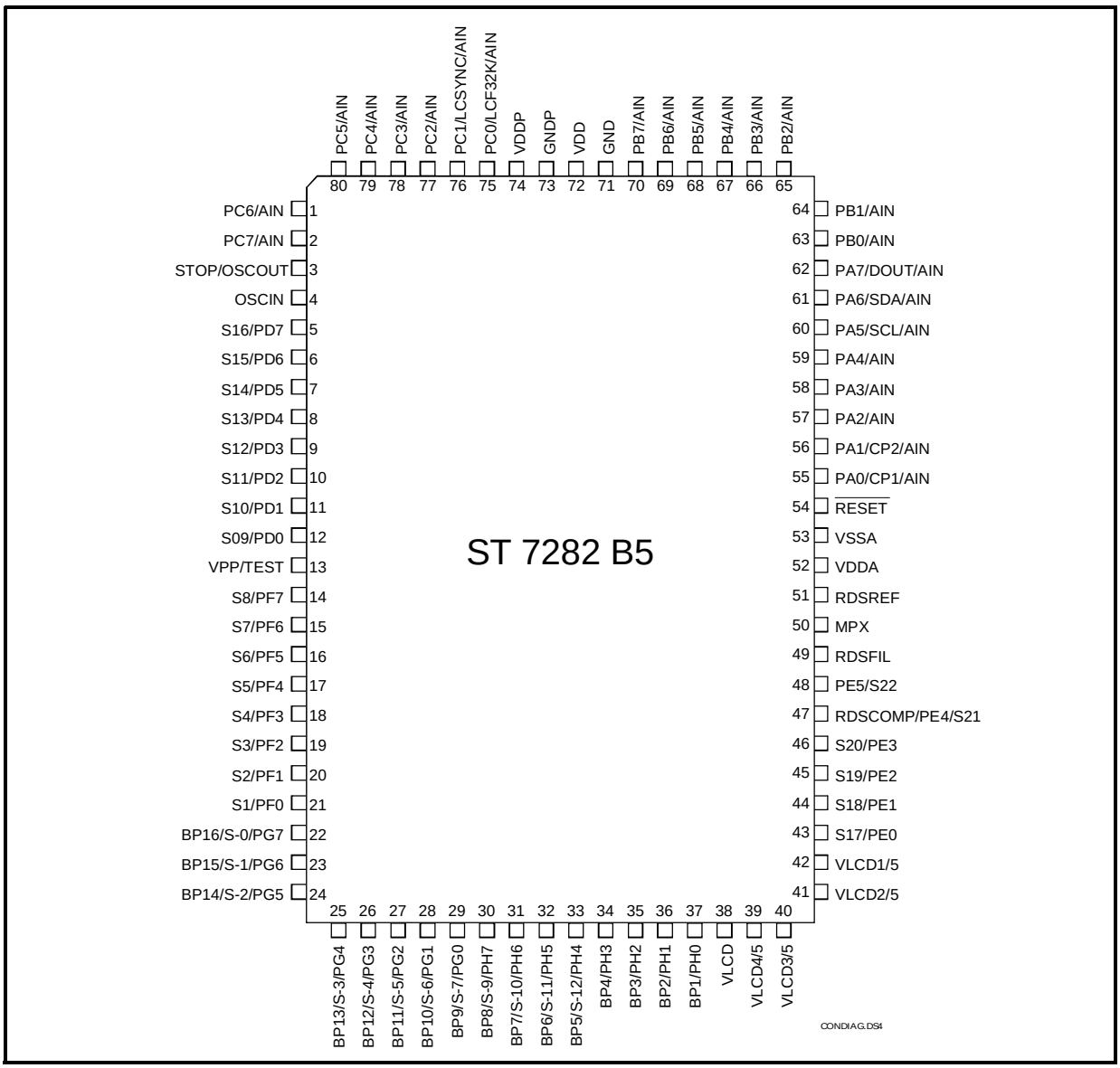
Pin VPP/TEST is used for testing the device. For normal operation pin VPP/TEST has to be connected to V_{SS} or has to be left open. An internal pull down resistor of about 100k is integrated to select normal operation mode if pin VPP/TEST is not connected.

The testmodes are for SGS THOMSON internal use only!

4 PIN DESCRIPTION

4.1 Connection diagram

Figure 10. Connection Diagram (top view) for the 80 pin quad flat pack



4.2 PIN DESCRIPTION

Ports A, B, C, D, E, F, G are described on page 18	
STOP/OSCOUT STOP/OSCIN	Oscillator pins
VPP/TEST	Test pin
VLCD VLCD 4/5 VLCD 3/5 VLCD 2/5 VLCD 1/5	Voltage levels for the LCD module
NC	(not connected) - must be left open
RDSCOMP RDSFIL MPX RDSREF	I/O Pins for the RDS module (see seperate spec)
VSSA VDDA	Analog voltages for the ADC and filter module
VDD GND	Supply voltage
VDDP GNDP	Peripheral supply voltage
$\overline{\textbf{Reset}}$	Reset pin - active low

5 RELATED DOCUMENTS

ST7 ADC2- SD 70K L138 ed. A
ST7 RDS BD - SD 70K L145 ed. B
ST7 RDS GB - SD 70K L144 ed. B
ST7 RDS FI - SD 70K L129 ed. C
ST7 SIO - # 96098 ed. B
ST7 OSCILLATOR - SD 70K L163 ed. A
ST7 LCIO1 - SD 70K L135 ed. C
ST7 IO3 - SD 70K L136 ed. B
ST7 LCD4 - SD 70K L140 ed. B
ST7 TIM4 - SD 70K L130 ed. A
ST7 WD2 - SD 70K L137 ed. A
ST7 EEPROMeep2a

6 HISTORIC

Below, the differences between the original specification # 96096 ed. B (ST7282B5) and the present specification # 97115 ed. B:

Page # modified in original spec 96096	Modifications	New page
1	Block diagram : S21, S22	2
2	Quick reference : 2 commercial products	3
3	VLCD changed from target of 10V to < 7V LU on all pins changed from target of class A to class A on all pins except pin V_{DDA} (52) class C	3
4	Islow changed from target of 1mA to 2mA; Ihalt changed from target of 10µA to 100µA ; VLCD changed from target of 10V to 7V.	4 - 5
7	Address mapping : TIMER	7 - 8 - 9 - 10
21	EEPROM : 2 bank 256 bytes	19
	Oscillator	20
23	Connection diagram : S21, S22	21
	Related documents, sales types	23

7 ORDERING INFORMATION

SALES TYPE	OPTIONS	TEMP RANGE	PACKAGE
ST7282A5Q6B/XXX	NO LCD	-40°C to 85°C	PQFP80
ST7282B5Q6B/XXX	WITH LCD		

The user code to be delivered to SGS-THOMSON must be in Motorola S.format (.S19) and must NOT include EEPROM content.