深圳市拓普微科技开发有限公司

SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LMT035DNJFWD-1

LCD Module User Manual

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Rev.	Descriptions	Release Date
0.1	Preliminary New release	2020-09-16
0.2	Update LED Backlight Circuit Characteristics	2021-09-01
0.3	Add Inspection Condition Packing Drawing	2021-10-13
0.4	Update DC Characteristics	2022-02-23
0.5	Update section 6.2	2022-03-05

Table of Content

1. Basic Specifications 3

1.1 Block Diagram 3
1.2 Terminal Functions 4

2. Absolute Maximum Ratings 5

3. Electrical Characteristics 5

3.1 DC Characteristics 5
3.2 LED Backlight Circuit Characteristics 6

4. AC Characteristics 6

4.1 DBI Type B 6
4.2 3-Line SPI Interface Timing Characteristic 11
4.3 4-Line SPI Interface Timing Characteristic 12
4.4 DPI Interface 13
4.5 Power ON/OFF Sequence 16
4.6 Reset timing 17

5 . Optical Characteristics 18

6 .INSPECTION CONDITION 检验条件 21

6.2. Display Pattern显示缺陷 21
6.3 .Quality Level and Sampling抽样方法 23
6.4 Handling Precaution使用注意事项 23

7 .Packing Drawing 24

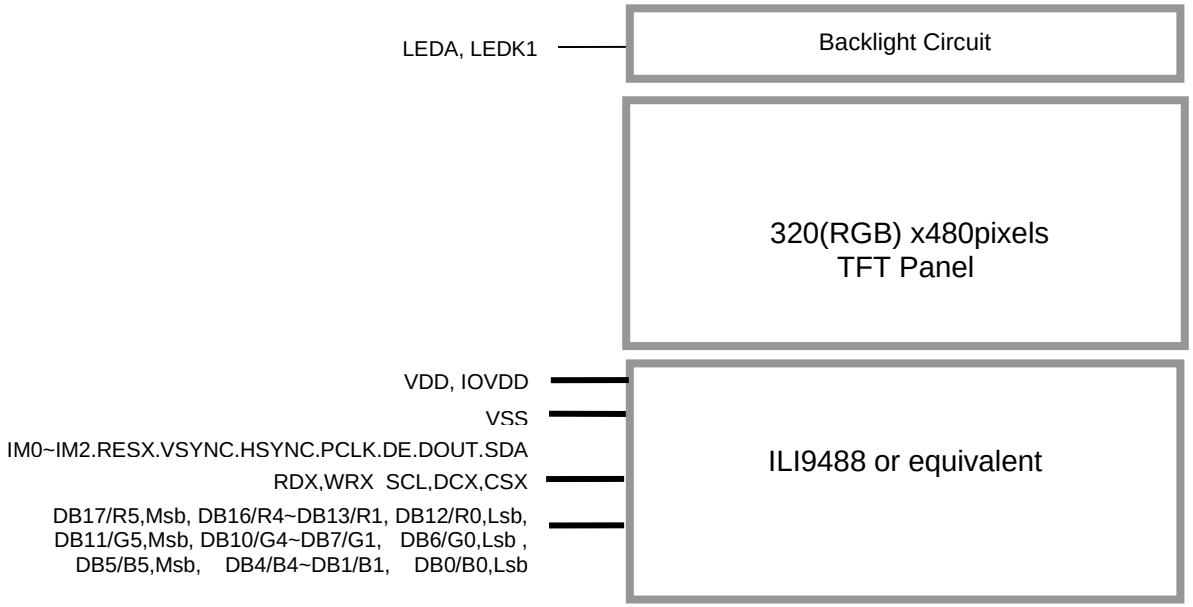
1. Basic Specifications

Screen Size(Diagonal) :	3.5”
Color Depth:	65K/262K Color
Number of dots :	320(RGB)x480
Active Area :	48.96x73.44mm
Dot Pitch :	0.153x0.153mm
Display Technology :	a-Si TFT active matrix
Display Mode :	Transmissive With Normally white
Pixel Configuration :	RGB Vertical Stripe
Viewing Direction :	12H (*1) (gray scale inverse) 6H (*2)
Polarizer Surface Treatment:	HC
Backlight Type:	LEDs
Outline Dimension :	55.26x 84.69 x 2.2 mm (exclude FPC , see dwg for details)
Operating Temperature :	-20 ~ +70°C (No Condensation)
Storage Temperature :	-30 ~ +80°C (No Condensation)

Note:

*1. For saturated color display content (eg. pure-red, pure-green, pure-blue or pure-colors-combinations).
*2. For “color scales” display content.
*3. Color tone may slightly change by temperature and driving condition.

1.1 Block Diagram



1.2 Terminal Functions

Pin No.	PIN Name	I/O	Descriptions
1	VSS	Power	Negative power supply,0V
2,3	IOVDD	Power	IO Positive Power
4,5	VDD	Power	Positive power supply
6	IM0	Input	MPU system interface mode select
7	IM1	Input	MPU system interface mode select
8	IM2	Input	MPU system interface mode select
9	RESX	Input	Reset signal RESX = L, Initialization is executed RESX = H, Normal running.
10	VSYNC	Input	Vertical sync. signal in RGB mode If no used, please connect this pin to VSS
11	HSYNC	Input	Horizontal sync, signal in RGB mode If no used, please connect this pin to VSS
12	PCLK	Input	Pixel clock signal in RGB mode If no used, please connect this pin to VSS
13	DE	Output	Data enable signal in RGB mode If no used, please fix this pin at VSS level
14	DB17/R5,Msb	I/O	Data Bus
15	DB16/R4	I/O	
:	:	:	
18	DB13/R1	I/O	
19	DB12/R0,Lsb	I/O	
20	DB11/G5,Msb	I/O	
21	DB10/G4	I/O	
:	:	:	
24	DB7/G1	I/O	
25	DB6/G0,Lsb	I/O	
26	DB5/B5,Msb	I/O	
27	DB4/B4	I/O	
:	:	:	
30	DB1/B1	I/O	
31	DB0/B0,Lsb	I/O	
32	VSS	Power	Negative power supply,0V
33	DOUT	Output	Serial data output pin If no used, leave this pin open
34	SDA	I/O	serial data input /output bi-direction pin
35	RDX	Input	serve as a read signal
36	WRX_SCL	Input	(WR) Write data enable pin in DBI Type B (SCL) Write data enable pin in DBI Type C If no used, please connect this pin to IOVDD
37	DCX	Input	Data/Command Selection pin Low: Command High: Parameter
38	CSX	Input	Chip select signal If no used, please connect this pin to IOVDD
39	NC(XR)	-	No connect
40	NC(YD)		
41	NC(XL)		
42	NC(YU)		
43	LEDA	Power	LED ANODE
44~49	LEDK	Power	LEDK CATHODE
50	VSS	Power	Negative power supply,0V

IM2	IM1	IM0	Interface	WR/SCL	DATA Bus use	
					Command/Parament	GRAM
0	0	0	DBITYPE-B18-bit (DB_EN='0')	WR	DB7~DB0	DB17 ~DB0:18bits Data
0	0	1	DBI TYPE-B 9-bit	WR	DB7~DB0	DB8 ~DB0: 9bits Data
0	1	0	DBI TYPE-B 16-bit	WR	DB7~DB0	DBI5~DB0:16bits Data
0	1	1	DBI TYPE-B 8-bit	WR	DB7~DB0	DB7 -DB0:8bits Data
1	0	1	DBI TYPE-C Option 1(3 wire)	SCL	SDA/DOUT	
1	1	1	DBI TYPE-C Option 3(4 wire)	SCL	SDA/DOUT	

System interface select

2. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Power Voltage	VDD	-0.3	+3.6	V	V_{SS} = 0V
Input Voltage	V_{IN}	-0.3	+3.6	V	V_{SS} = 0V
Operating Temperature	T_{OP}	-20	+70	°C	No Condensation
Storage Temperature	T_{ST}	-30	+80	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

3. Electrical Characteristics

3.1 DC Characteristics

V_{SS}=0V, T_{OP}=25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition / Application Pin
Operating Voltage	VDD	2.65	3.0	3.6	V	VDD,IOVDD
Input High Voltage	V_{IH}	0.7xV_{DD}	-	V_{DD}	V	IM0~IM2,RESX,VSYNC,HSYNC,PCLK,DB17/R5,Msb, DB16/R4~DB13/R1 ,DB12/R0,Lsb,DB11/G5,Msb, DB10/G4~DB7/G1 ,DB6/G0,Lsb,DB5/B5,Msb, DB4/B4~DB1/B1,DB0/B0,Lsb, SDA,RDX,WRX_SCL,DCX, CSX,
Input Low Voltage	V_{IL}	-0.3	-	0.3xV_{DD}	V	
Output Low Voltage	V_{OL}	0	-	0.99	V	DB17/R5,Msb, DB16/R4~DB13/R1 ,DB12/R0,Lsb,DB11/G5,Msb, DB10/G4~DB7/G1 ,DB6/G0,Lsb,DB5/B5,Msb, DB4/B4~DB1/B1,DB0/B0,Lsb, DE,SDA,DOUT
Operating Current	I_{DD}	-	8	-	mA	VDD (*1)

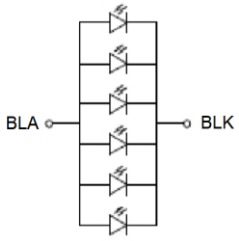
Note: *1. VDD=3.0V

3.2 LED Backlight Circuit Characteristics

T_{OP} =25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Forward Voltage	Vf	-	3.2	-	V	For each LED
Forward Current	If	-	20	-	mA	For each LED
LED lifetime	-	-	30000	-	Hours	

Note1:LED CIRCUIT DIAGRAM



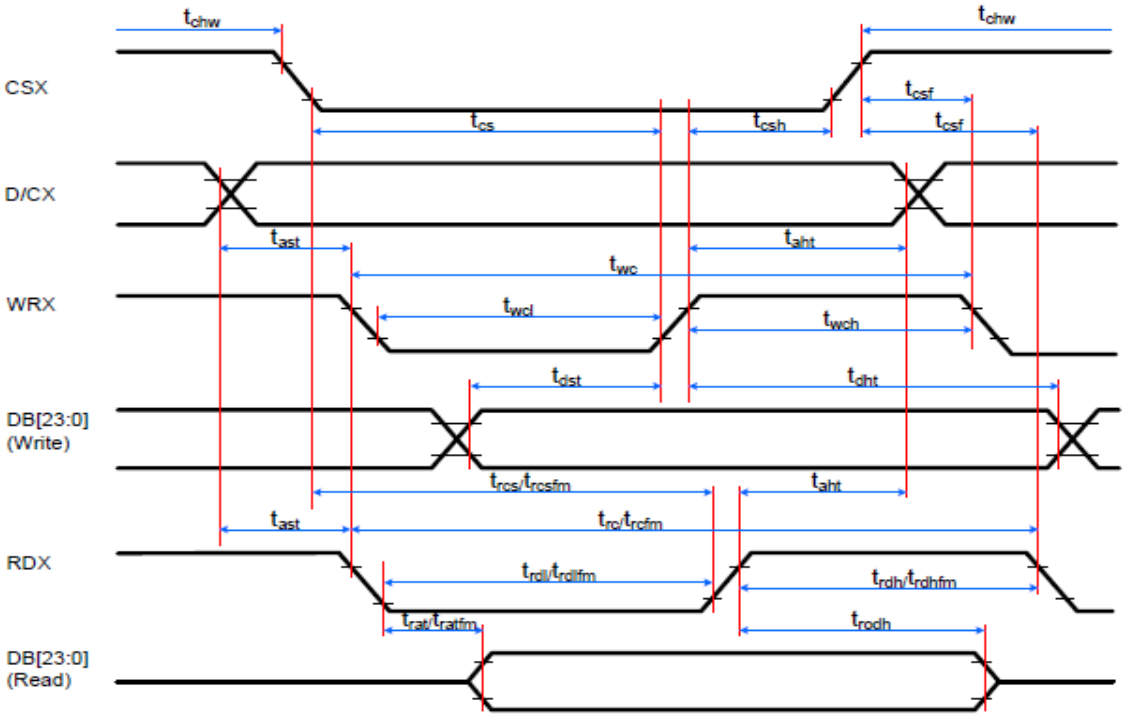
No. of LEDs = 6pcs

Note 2:LED: VF =3.2V, IF =20mA(TYP)
Note 3:IF is defined for one LED.
Optical performance should be evaluated at Ta=25℃ only.
If LED is driven by high current, high ambient temperature & humidity condition.
The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness.
Typical operating life time is estimated data.
Note 4:Under LCM operating, the stable forward current should be inputted. And forward voltage is for reference only.

4. AC Characteristics

4.1 DBI Type B

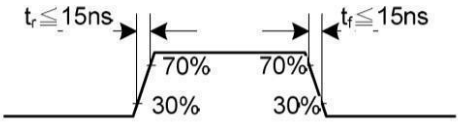
4.1.1 DBI Type B Timing Characteristic



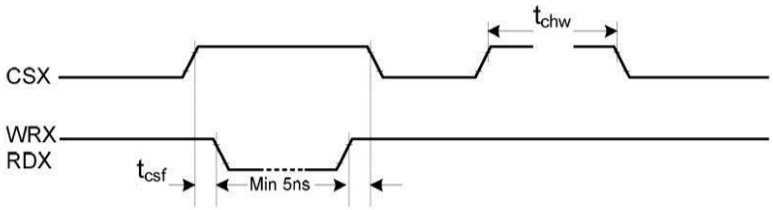
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	taht	Address hold time (Write/Read)	0	-	ns	-
CSX	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
WRX	twc	Write cycle	40	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB [23:0], DB [17:0], DB [15:0], DB [8:0], DB [7:0]	tdst	Write data setup time	10	-	ns	For maximum, CL=30pF For minimum, CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Notes:

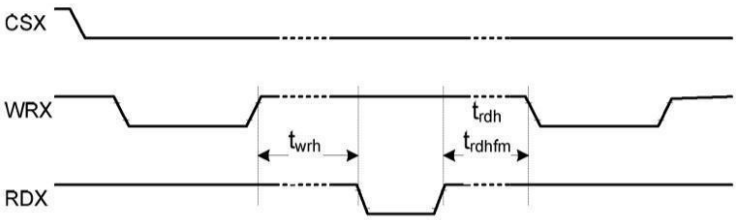
1. Ta = -30 to 70 ℃, IOVDD、VDD = 2.5V to 3.3V, VSS = 0V
2. Logic high and low levels are specified as 30% and 70% of IOVDD for input signals.
3. Input signal rising time and falling time:



4. The CSX timing:



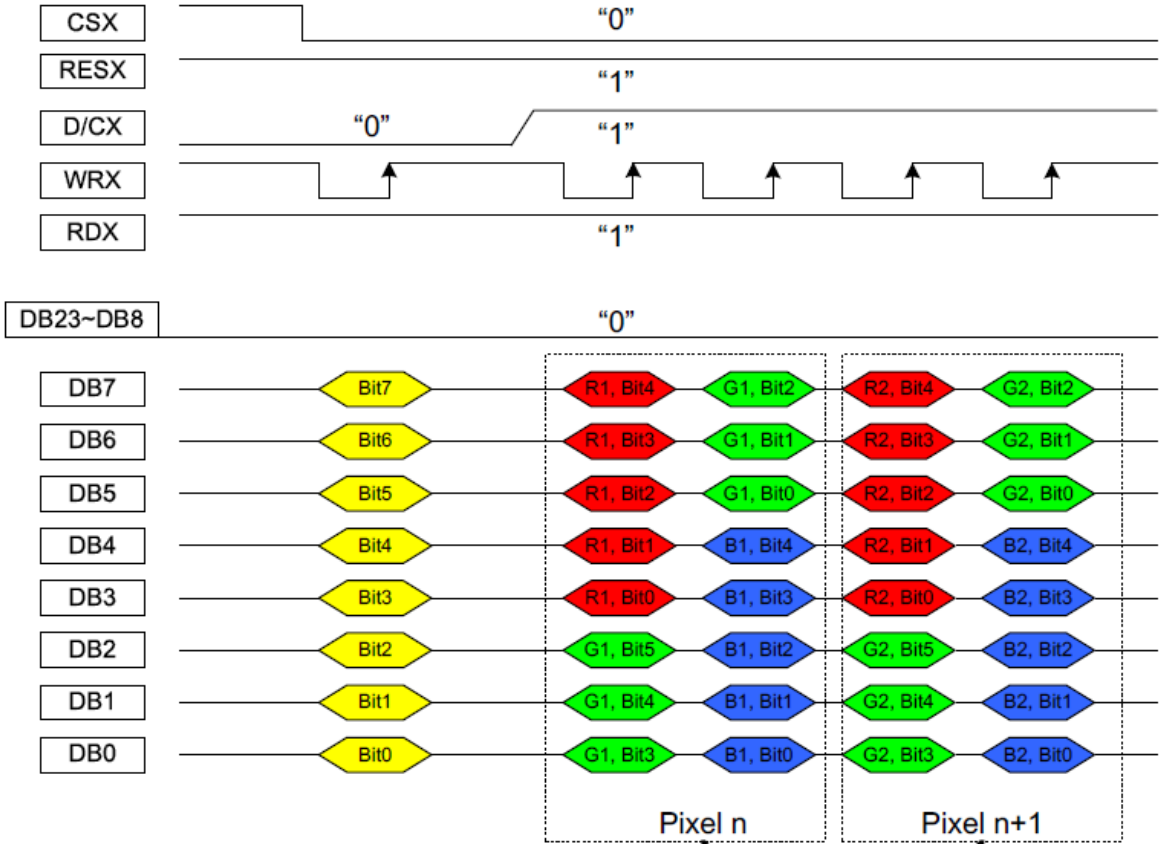
5. The Write to Read or the Read to Write timing:



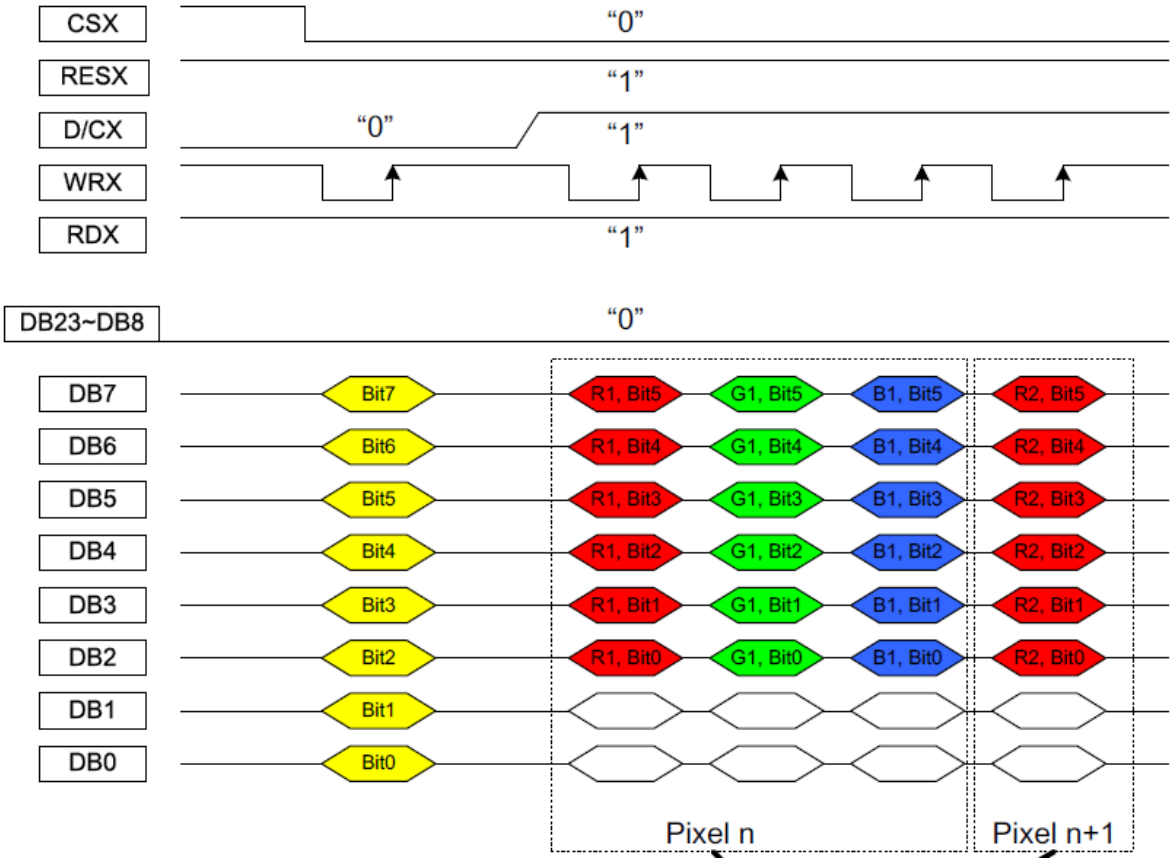
Please refer to IC: ILI9488 data sheet for more details.

4.1.2 DBI Type B Data Bus

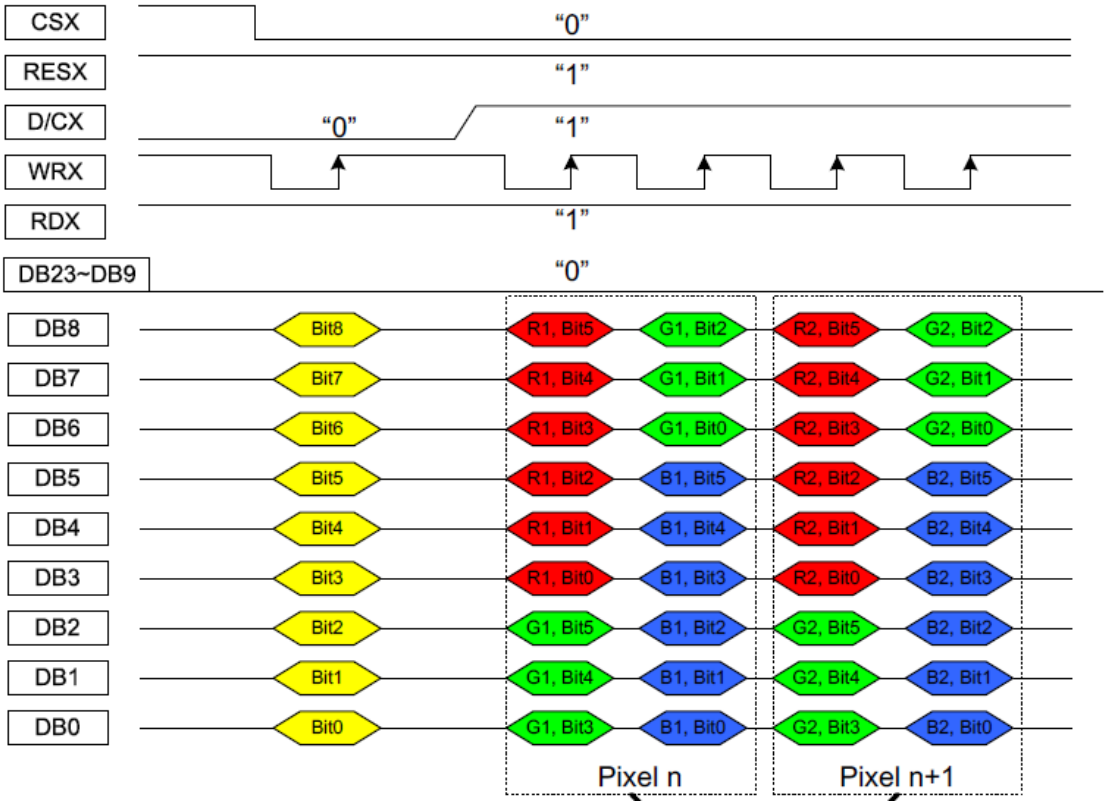
8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color



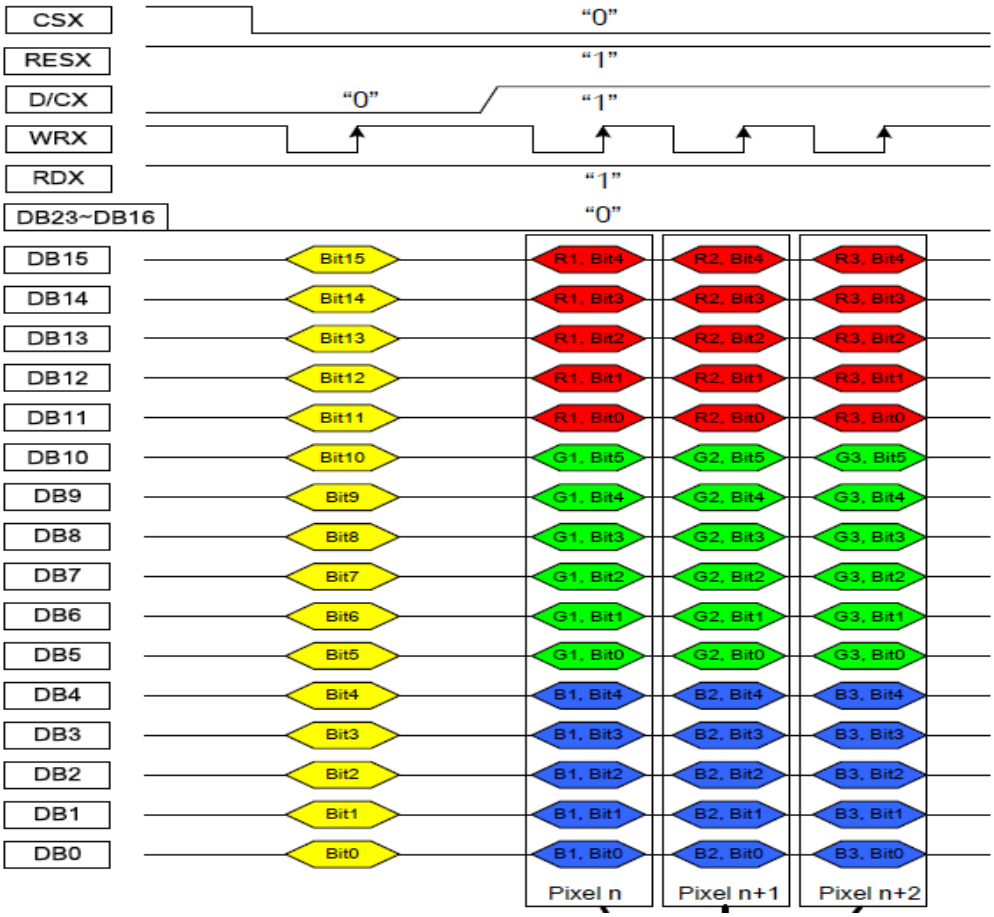
8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



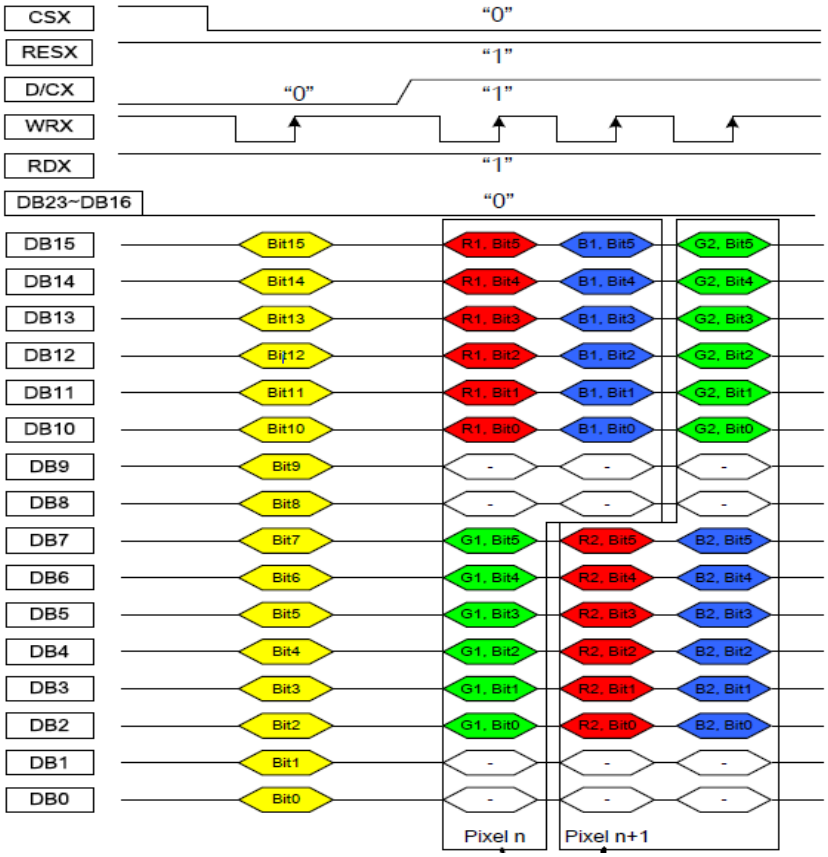
9-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



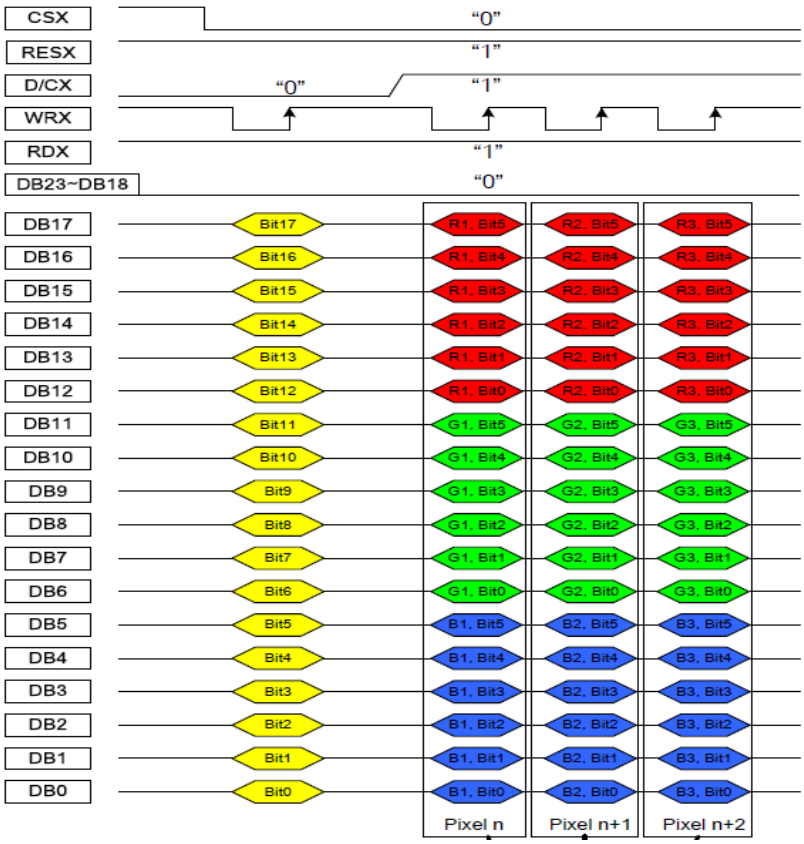
16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color



16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

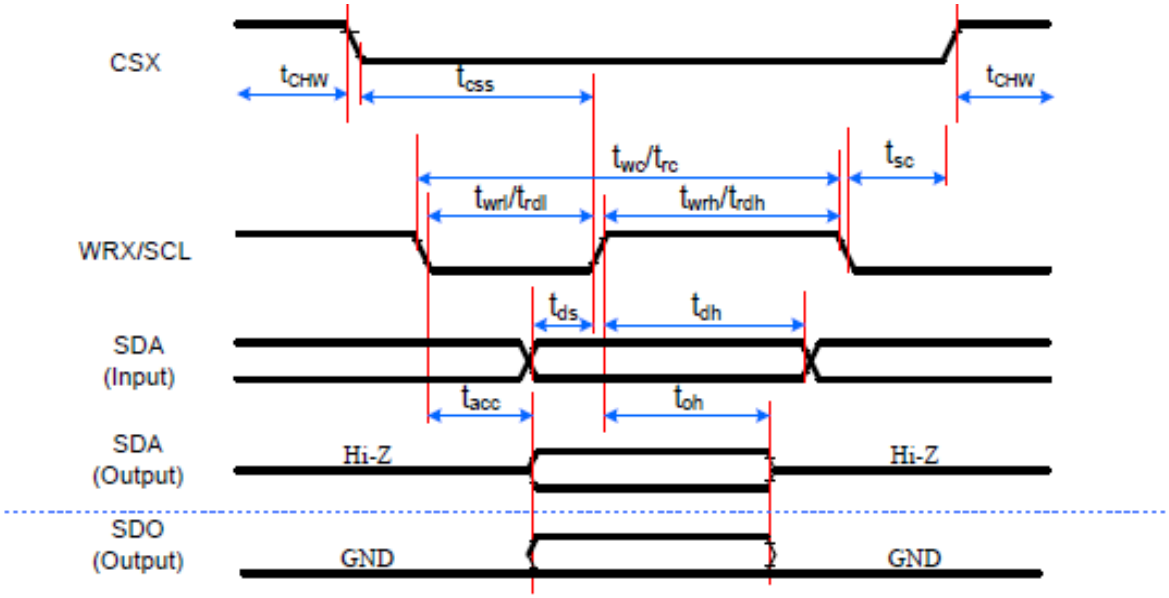


18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



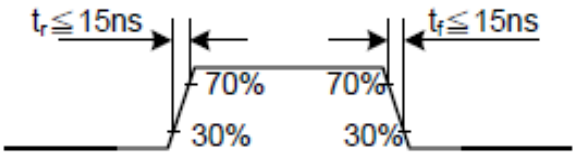
Please refer to IC: ILI9488 data sheet for more details.

4.2 3-Line SPI Interface Timing Characteristic



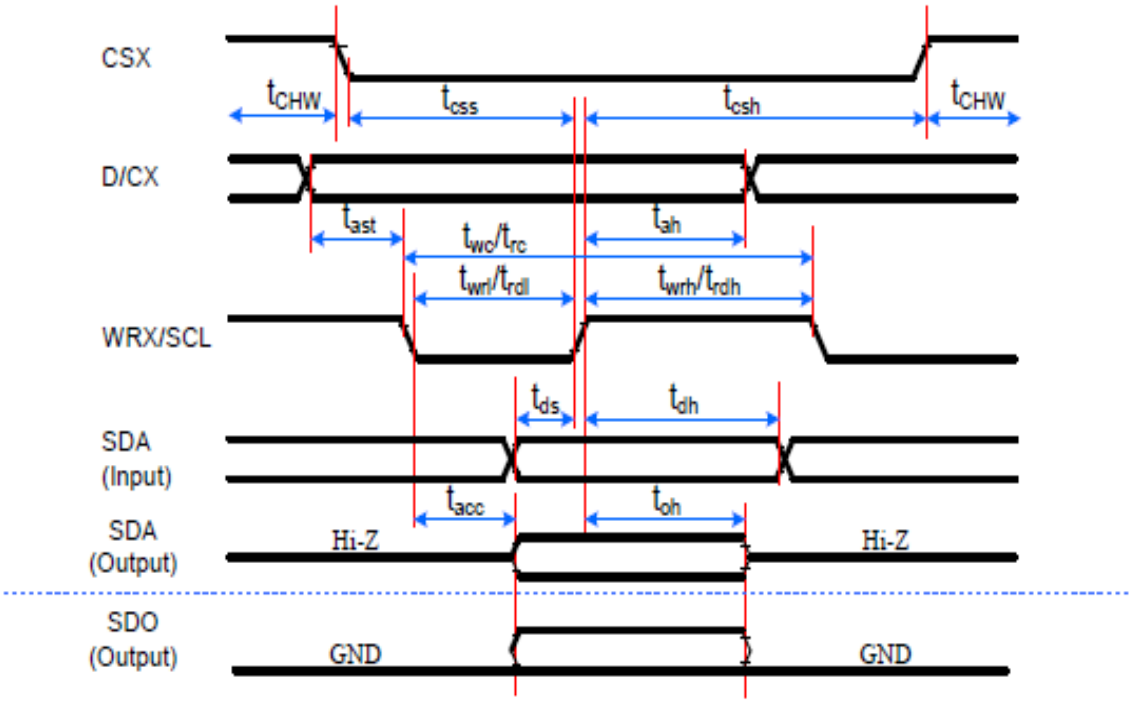
Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchw	CSX H Pulse Width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
	twrl	SCL L Pulse Width (Write)	15	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = -30 to 70 °C, IOVDD,VDD=2.5V to 3.3V,VSS=0V, T = 10+/-0.5ns



Please refer to IC: ILI9488 data sheet for more details.

4.3 4-Line SPI Interface Timing Characteristic

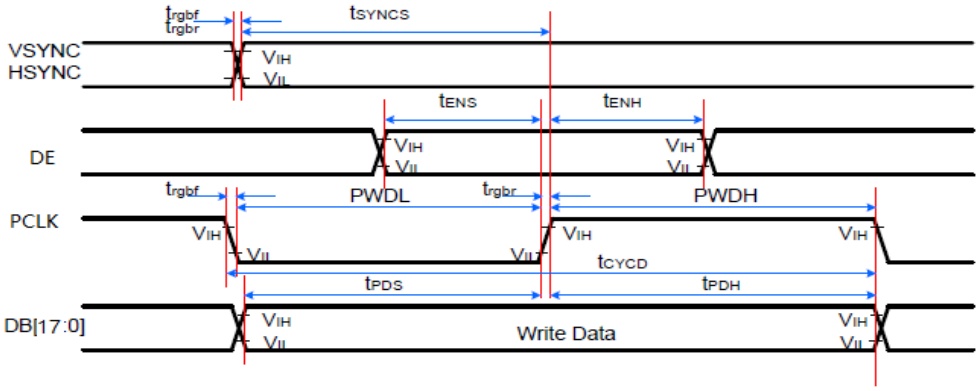


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS H pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	50	-	ns	
	twrh	SCL H pulse width (Write)	10	-	ns	
	twrl	SCL L pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	-	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note:Ta=-30 to 70℃, IOVDD, VDD=2.5V to 3.3V, VSS=0V, T=10+/-0.5ns.
Please refer to IC: ILI9488 data sheet for more details.

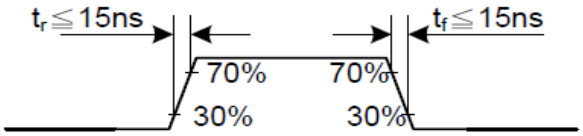
4.4 DPI Interface

4.4.1 DPI Interface Characteristic



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	16-/18-/24-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
DB[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
PCLK	PWDH	DOTCLK high-level period	20	-	ns	
	PWDL	DOTCLK low-level period	20	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, IOVCC , VDD=2.5V to 3.3V, VSS=0V, T=10+/-0.5ns.



Please refer to IC: ILI9488 data sheet for more details.

4.4.2 DPI Interface pixel format

18-bit DPI interface connection (DB [17:0] is used): set pixel format DPI [2:0] = 3'h6

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
						R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

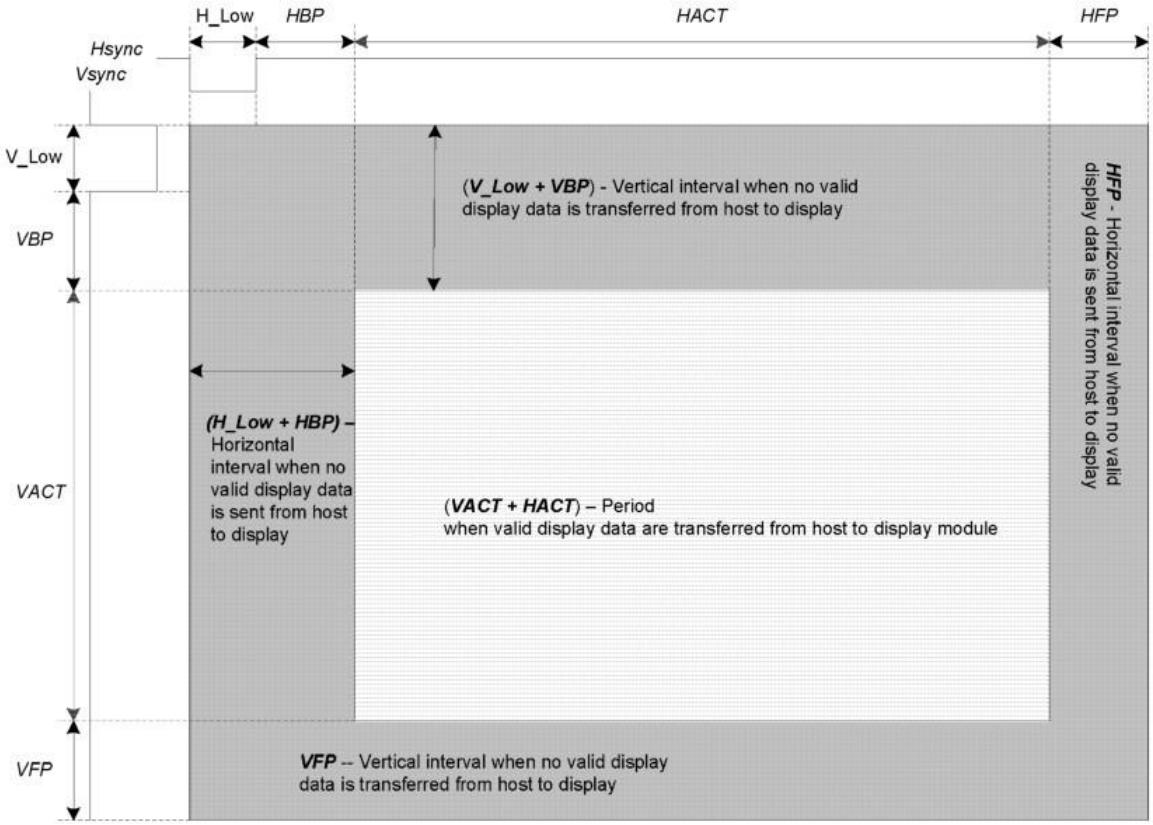
16-bit DPI interface connection (DB [15:0] is used): set pixel format DPI [2:0] = 3'h5

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
								R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

The Pixel clock (DCLK) runs all the time without stop. It is used to enter VS, HS, DE and D[17: 0] states when there is a rising edge of the DCLK. The DCLK cannot be used as the internal clock for other functions of the display module.
Vertical synchronization (VS) is used to indicate when a new frame of the display is received. This is low enable and its state is read to the display module by a rising edge of the DCLK signal.
Horizontal synchronization (HS) IS used to indicate when a new line of the frame is received. This is low enable and its state is read to the display module by a rising edge of the DCLK signal.
Data Enable (DE) is used to indicate when the RGB information that should be transferred in the display is received. This is a high enable, and its state is read to the display module by a rising edge of the DCLK signal.
D[17:0] is used to indicate what is the information of the image that is transferred on the display (when DE = 0 (low) and there is a rising edge of DCLK). D[17:0] can be 0(low) or 1(high). These lines are read by a rising edge of the DCLK signal. In RGB interface modes, the input display data is written to GRAM first then outputs the corresponding source voltage according to the gray data from GRAM.

Note: Please refer to IC: ILI9488 data sheet for more details.

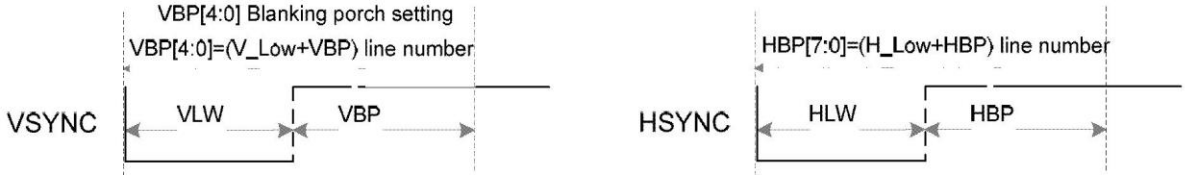
4.4.3 DPI(RGB) Interface timing

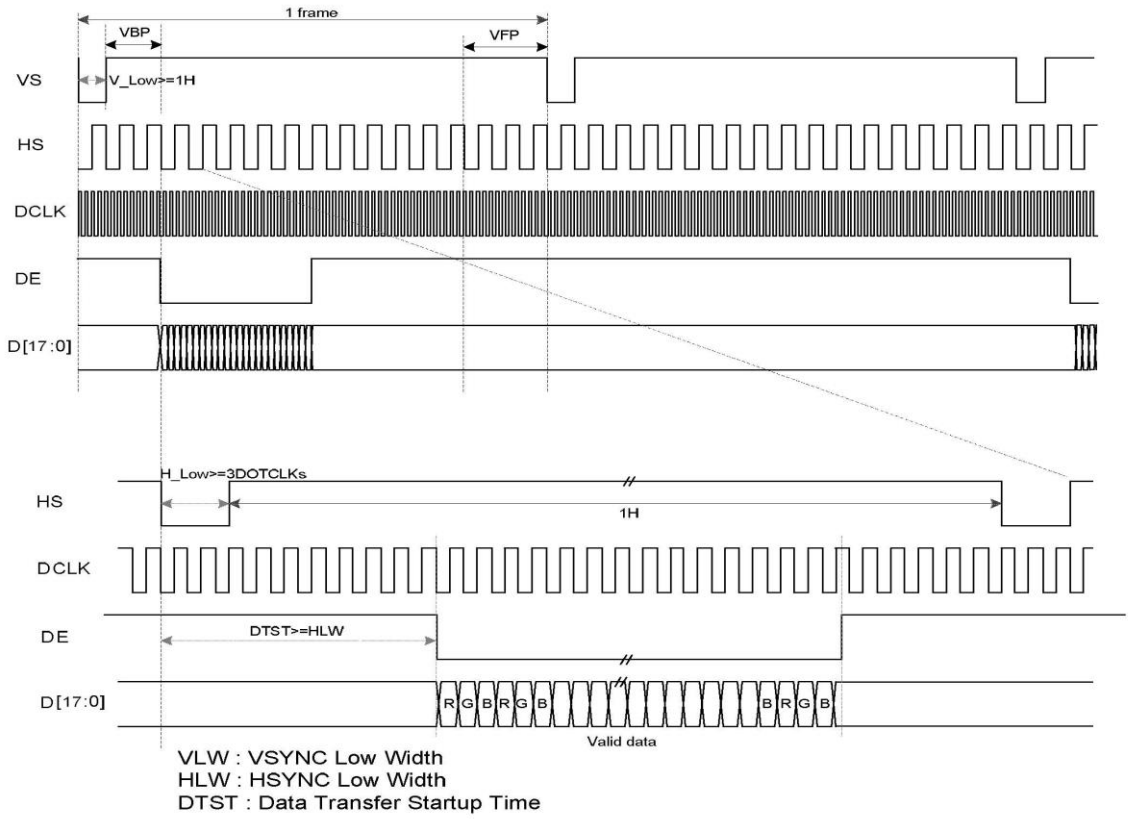


Parameters	Symbols	Min.	Typ.	Max.	Units
Horizontal Synchronization	H_Low	3	-	H_Low+HBP <192	DCLK
Horizontal Back Porch	HBP	3	-		DCLK
Horizontal Front Porch	HFP	3	-	255	DCLK
Horizontal Address	HACT	-	320	-	DCLK
Horizontal Frequency		-	-	33	KHz
Vertical Synchronization	V_Low	1	-	V_Low+VBP+VFP < 32	Line
Vertical Back Porch	VBP	2	-		Line
Vertical Front Porch	VFP	2	-		Line
Vertical Address	VACT	-	480	-	Line
Vertical Frequency		60	-	70	Hz
DCLK cycle		100	-	50	ns
DCLK Frequency		10	-	20	MHz

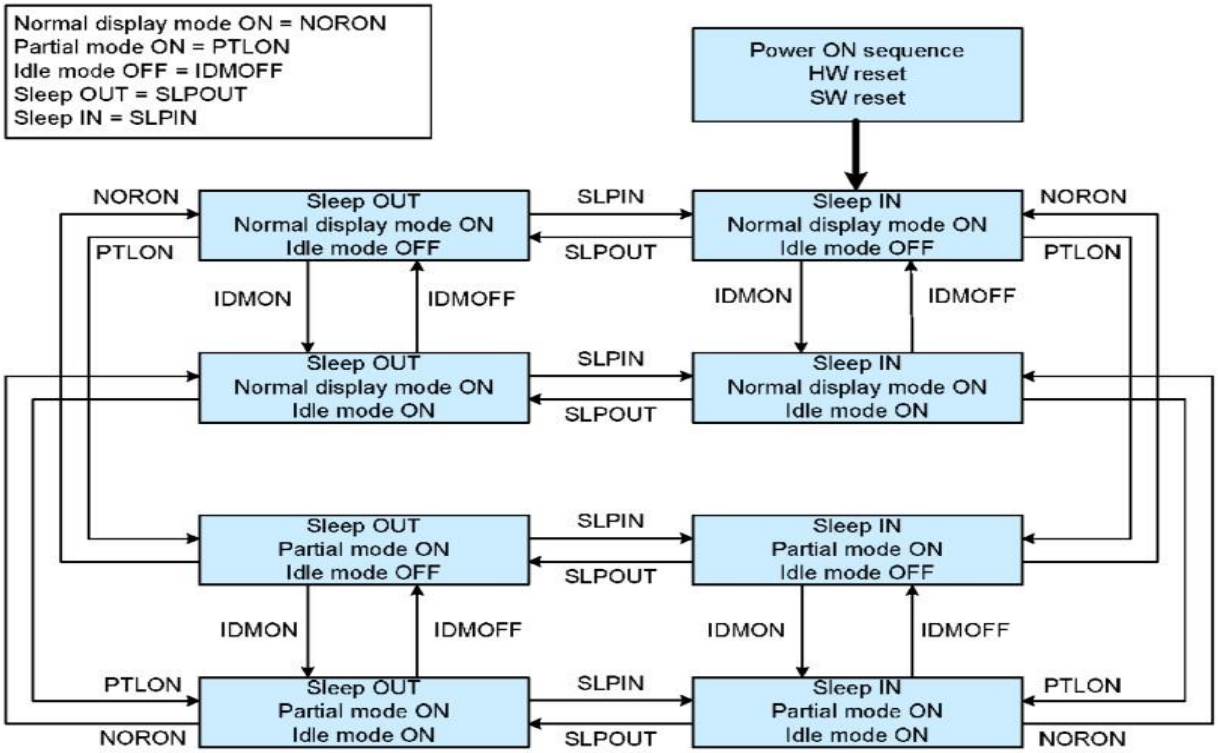
Example： DCLK = 20Mhz, TE=70Hz, V_Low+VBP=2, VFP=2, H_Low+HBP=100, HFP=170.

Note: VBP[4:0]/HBP[7:0] (Blanking Porch Control, RB5h) define as follows:





4.5 Power ON/OFF Sequence



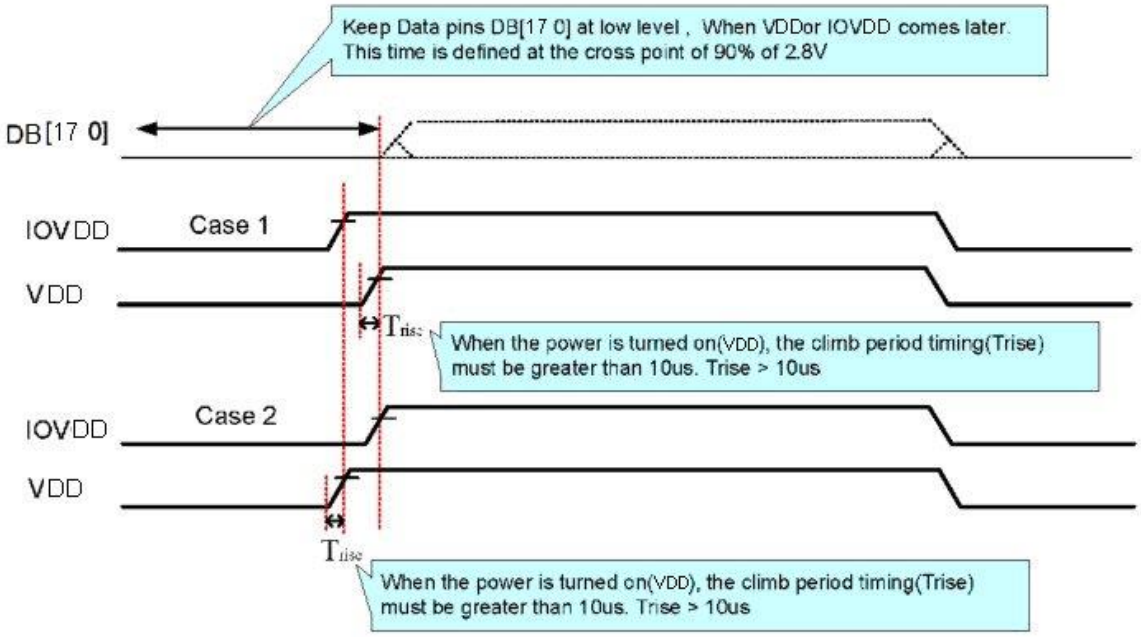
Notes:

1. There are not any abnormal visual effects when one power mode changes to another power mode.
2. There is not any limitation, which is not specified by users, when one power mode changes to another power mode.

IOVDD and VDD can be applied or powered down in any order. During the Power Off sequence ,if the LCD is in the Sleep In mode, VDD and IOVDD must be powered down with a minimum of 120 msec.If the LCD is in the Sleep In mode, VDD and IOVDD can be powered down with a minimum of 0msec after the /RST has been released. /CS can be applied at any time or can be permanently grounded. /RST has priority over /CS.

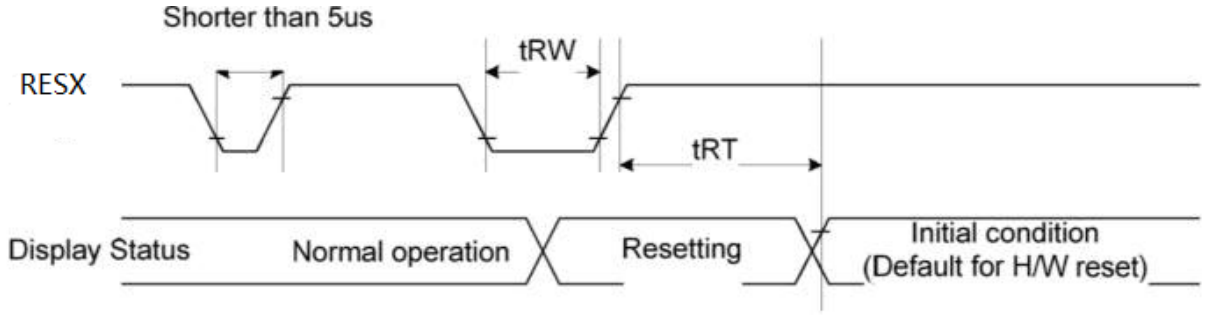
Notes:

1. There will be no damage to the ILI9488 if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequence.
3. There will be no abnormal visible effects on the display between the end of the Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the /RST line is not steadily held by the host during the Power On Sequence as defined in Sections 11.1 and 11.2 (ILI9488 datasheet), then it will be necessary to apply the Hardware /RST after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.
5. When the power is turned on, the climb period timing (Trise) must be greater than 10us.
6. Keep data pins D[17:0] at low level, or IOVDD comes later



Note: Please refer to IC: ILI9488 data sheet for more details.

4.6 Reset timing



Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset LOW pulse width	t_{RW}	1.0	-	-	us
Reset time	T_{RT}	-	-	120	ms

Please refer to IC: ILI9488 data sheet for more details.

5 . Optical Characteristics

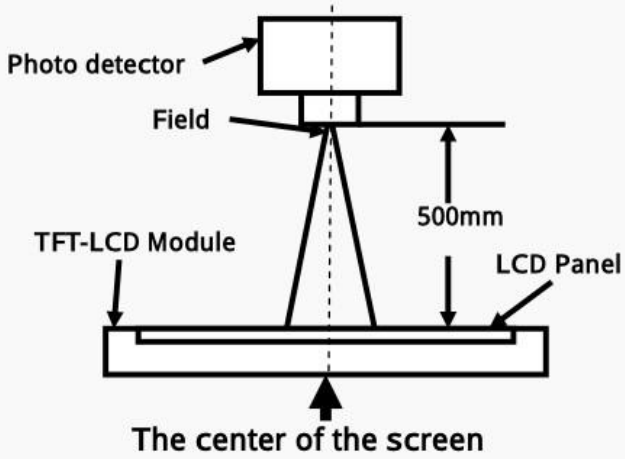
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	60	70		Degree	Note2,3
		θB		50	60			
		θL		60	70			
		θR		60	70			
Contrast Ratio		CR	θ=0°	400	500			Note 3
Response Time		T_{ON}	25℃		25	35	ms	Note 4
		T_{OFF}						
Chromaticity	White	x	Backlight is on		0.286			Note 1,5
		y			0.304			
	Red	x			0.608			Note 1,5
		y			0.336			
	Green	x			0.341			Note 1,5
		y			0.604			
	Blue	x			0.146			Note 1,5
		y			0.073			
Uniformity		U			80		%	Note 6
NTSC					60		%	Note 5
Luminance		L		200			cd/m^2	Note 7

Test Conditions:

1. I_{BLA} = 120 mA, and the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

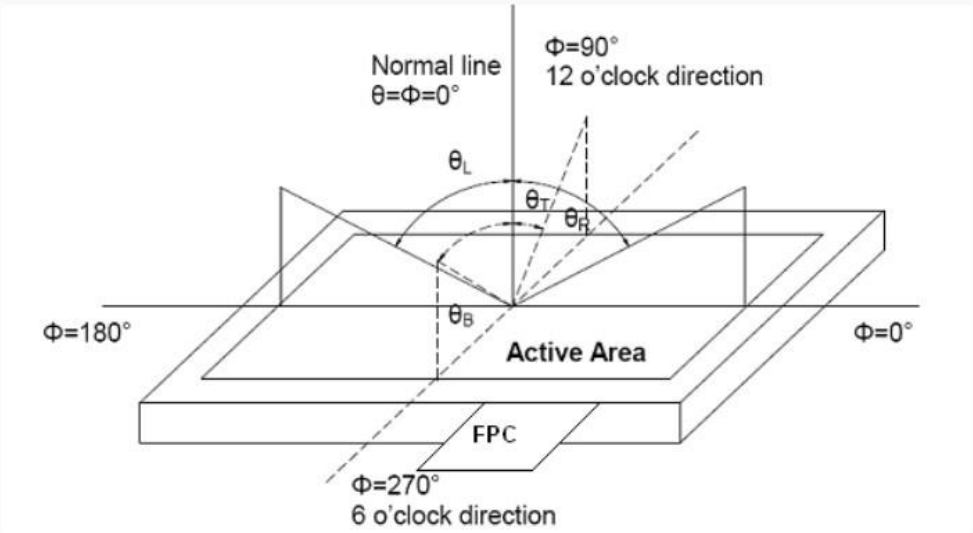
The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

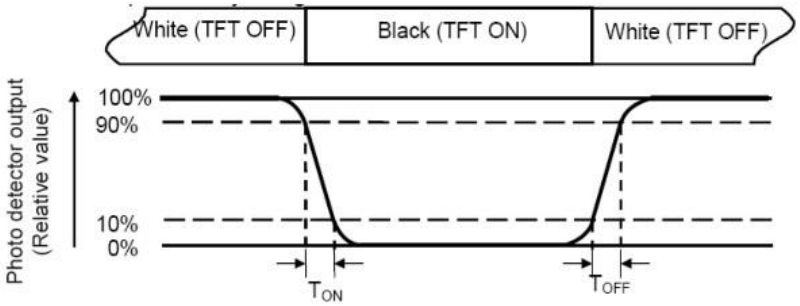
"White state ": The state is that the LCD should drive by Vwhite.

"Black state": The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

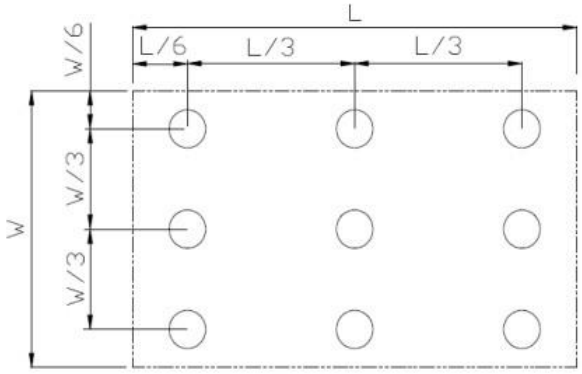
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

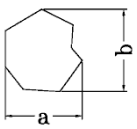
6 .INSPECTION CONDITION 检验条件

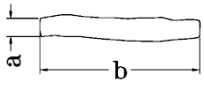
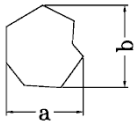
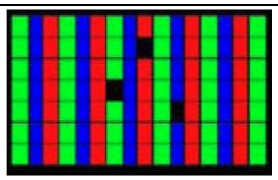
Unless otherwise stated，all the inspections are carryout under the following condition
除非有特别的规定，检验条件按以下执行。

No.	Items 项目	Conditions 条件
1	Lighting 照明	Illumination: Appearance 300-700Lux 环境亮度在 300~700LUX
2	Inspection Distance 检验距离	30-40cm form the test sample，within normal viewing angle 眼睛距显示器表面 30~40cm
3	Temperature 环境温度	Room Temperature (25 ºC), no condensation 室温（25 度），无凝水
4	Viewing Angle 视角	U/D: 45º/45º, L/R: 45º/45º 前后左右 45 度角范围内
5	Inspection Time 检验时间	15 seconds 15 秒内
6	Defect Allowance 缺陷总数	Under 5.0” (include 5.0”): 3 5.0” to 7.0”: 4 Above 7.0”: 6 5 寸(含)及以下：3 个 5 寸 ~ 7 寸：4 个 7 寸及以上：6 个

6.2. Display Pattern显示缺陷

Units(单位)=mm

No.	Items /Contents 检查项目	Type 类别			Standard 标准	Judgment 判定
		CR	MA	MI		
1	No Display/Unstable Display 无显示/显示不稳定		√		--	Not Allowed 不允许
2	Line defect 缺少行或列		√		--	Not Allowed 不允许
3	Display abnormally 错误的显示		√		--	Not Allowed 不允许
4	Function Defective 缺少功能		√		--	Not Allowed 不允许
5	Glass Crack 玻璃破碎		√		--	Not Allowed 不允许
6	Spot Defect Including: Black spot, White spot， Foreign particle, Polarizer dirt, Cell particle 黑点/白点 			√	Under 5.0” (include 5.0”) 5 寸及以下	
					(a+b)/2≤0.15	Allowed 允许
					0.15<(a+b)/2≤0.25	3 max. 允许 3 个
					(a+b)/2＞0.25	Not Allowed 不允许
					Above 5.0” 5 寸及以上	
					(a+b)/2≤0.25	Allowed 允许
					0.25<(a+b)/2≤0.5	3 max. 允许 3 个
					(a+b)/2＞0.5	Not Allowed 不允许

7	Line Defect Including: Black line, White line, Scratch 线 			√	Under 5.0” (include 5.0”) ·5 寸及以下	
					a≤0.03	Allowed 允许
					0.03<a≤0.05 and b≤5.0	2 max. 允许 2 个
					a＞0.05 or b＞5.0	Not Allowed 不允许
					Above 5.0” 5 寸及以上	
					a≤0.03	Allowed 允许
					0.03<a≤0.05 and b≤5.0	4 max. 允许 4 个
					a＞0.05 or b＞5.0	Not Allowed 不允许
8	Polarizer Dent/Bubble 偏光片气泡 			√	Under 5.0” (include 5.0”) ·5 寸及以下	
					(a+b)/2≤0.25	Allowed 允许
					0.25< (a+b)/2≤0.5	3 max. 允许 3 个
					(a+b)/2＞0.5	Not Allowed 不允许
					Above 5.0” 5 寸及以上	
					(a+b)/2≤0.25	Allowed 允许
					0.25< (a+b)/2≤0.5	3 max. 允许 3 个
					(a+b)/2＞0.5	Not Allowed 不允许
9	Bright dot defect 亮点 (在全黑屏下多像素点）				√	Under 5.0” (include 5.0”) 5 寸及以下
						0 max. 允许 0 个
					5.0” to 7.0” 5 寸 ~ 7 寸	2 max. 允许 2 个
					Above 7.0” 7 寸以上	3 max. 允许 3 个
					3 consecutive dots 3 个或以上连续的点	Not Allowed 不允许
10	Dark dot defect 暗点 （在全红或全绿或全蓝屏下缺像素点）				√	Under 5.0” (include 5.0”) 5 寸及以下
						2 max. 允许 2 个
					5.0” to 7.0” 5 寸~7 寸	4 max. 允许 4 个
					Above 7.0” 7 寸以上	5 max. 允许 5 个
					3 consecutive dots 3 个或以上连续的点	Not Allowed 不允许
11	Bright dot defect + Dark dot defect 亮点 + 暗点				√	Under 5.0” (include 5.0”) 5 寸及以下
						2 max. 允许 2 个
					5.0” to 7.0” 5 寸~7 寸	4 max. 允许 4 个
					Above 7.0” 7 寸以上	5 max. 允许 5 个
12	FPC or FFC broken FPC/FFC 损坏			√	--	Not Allowed 不允许
13	PCBA defect PCBA 缺陷			√	Refer to IPC-A-610 按照 IPC-A-610	--

6.3 .Quality Level and Sampling抽样方法

Items项目	Standard标准
Sampling Standard引用标准	MIL-STD-105E
Sampling Level 抽样等级	Ⅱ
AQL level 合格判定水平	MA: AQL=0.65 MI: AQL=1.0

6.4 Handling Precaution使用注意事项

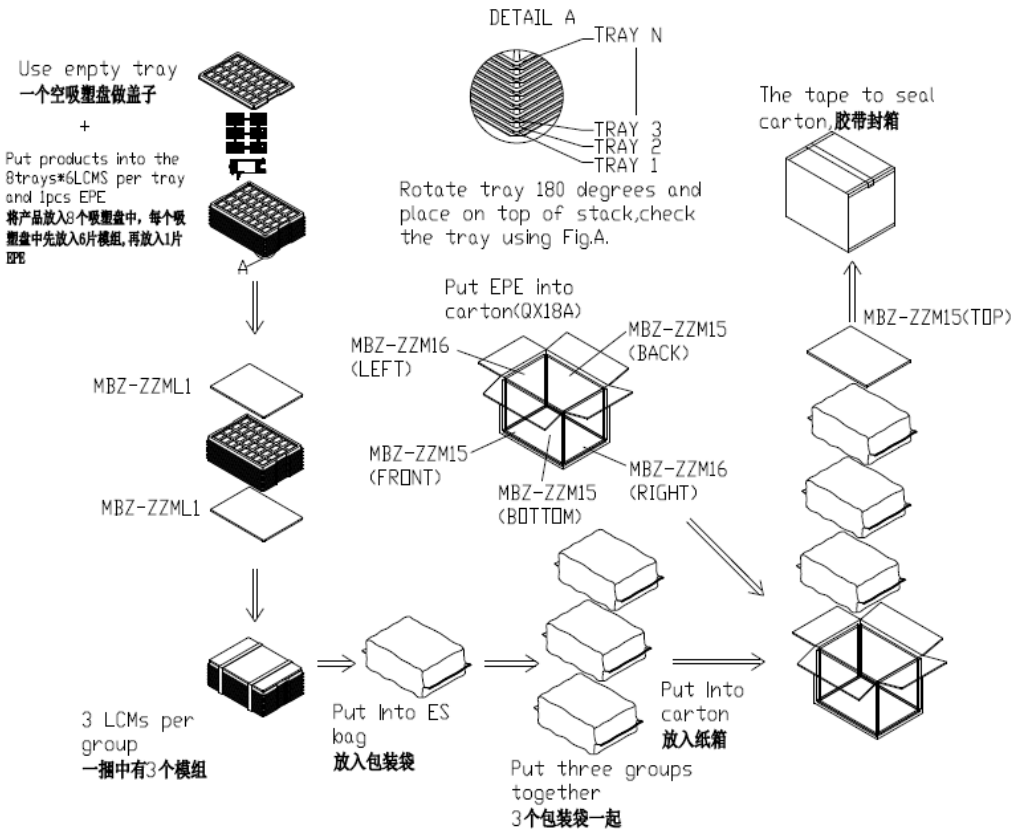
1. Never attempt to disassemble or rework LCD module
   禁止拆卸或改造显示模块
2. Never let LCD module contact with liquids
   禁止液体接触
3. LCD module can be easily damaged by electrostatic charge.
   Please maintain an optimum anti-static working environment.
   请在静电防护环境下打开包装使用
4. LCD panel is made with glass.
   Any mechanical shock (eg. Vibration, distortion, extrusion, impact，drop) will damage the LCD module.
   振动、扭曲、挤压、碰撞、跌落等会造成损失或破裂
5. Avoid showing a display pattern on screen for a long time (continuous ON segment)
   长时间画面停留会造成影像残留
6. The color and evenness of the display may slightly vary with the temperature
   显示颜色和显示均匀度会因外界温度而有所变化
7. Signal and Power supply excess the operation range may damage the LCD module
   错误的输入电压（电流）或电信号会造成电路或元器件烧坏
8. Avoid touching the LCD surface to prevent any scratch on its surface
   避免手指和其他物品接触液晶屏表面

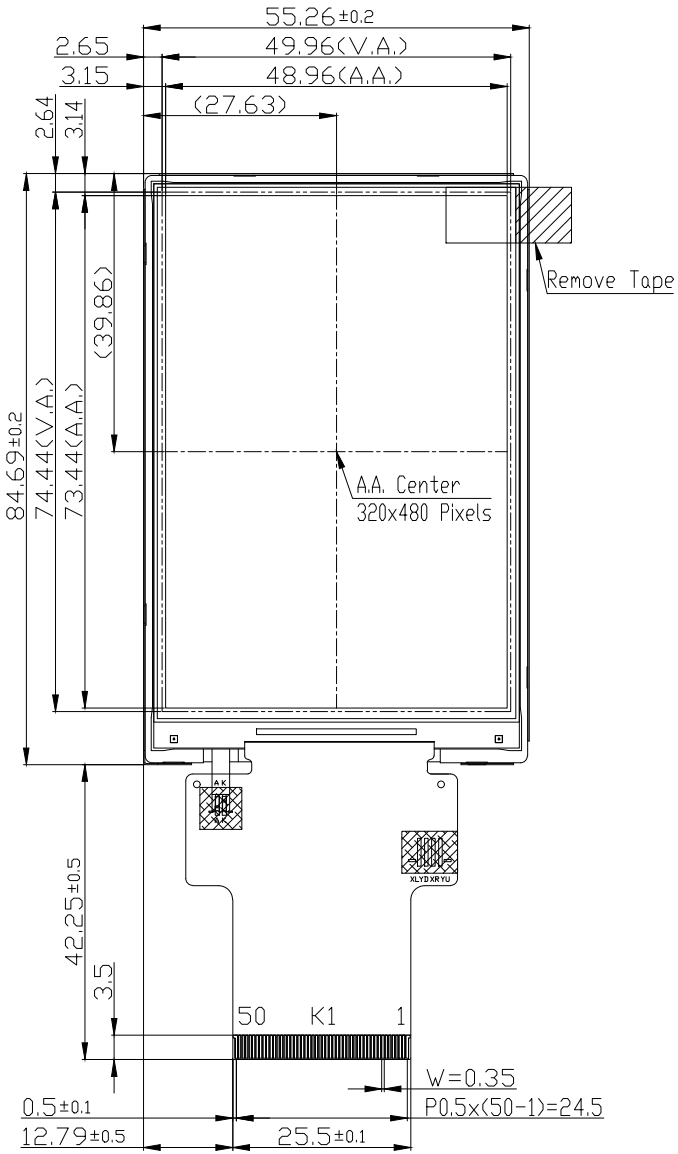
7 .Packing Drawing

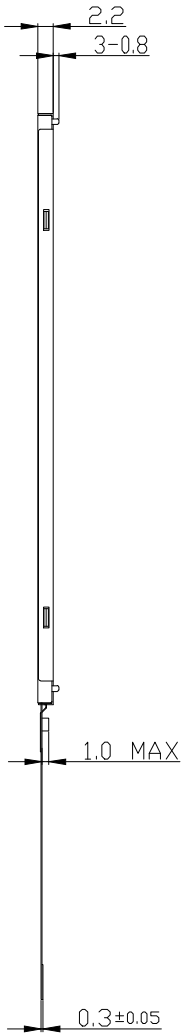
Per Carton

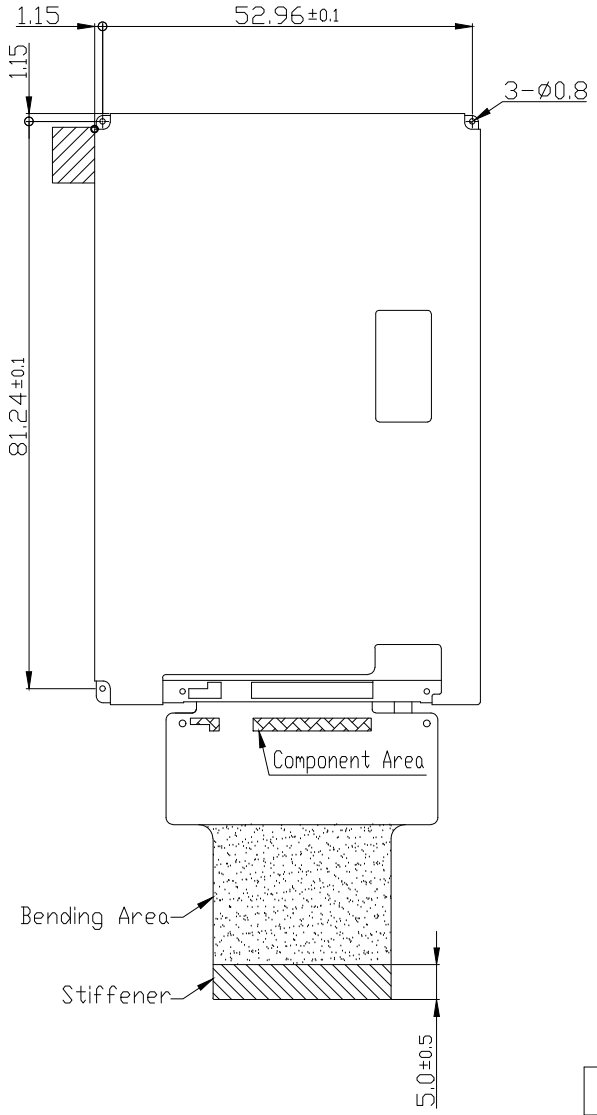
No	Item	Model (Materiel)	Dimensions(mm)	Unit Weight(Kg)	Quantity	Remark
1	LCM	LMT035DNJFWD-1	84.19*54.76*2.00	TBD	144	LMT035DNJFWD-1
2	Tray	PET	356*256*14.5	TBD	27	1150357260
3	EPE	EPE	196.78*191.54*2	0.002	24	1680370570
4	EPE（珍珠棉1）	MBZ-ZZML1	336*246*6	0.01	6	1680104800
5	EPE（珍珠棉2）	MBZ-ZZM15	375*275*10	0.014	4	1680267110
6	EPE（珍珠棉3）	MBZ-ZZM16	250*280*12	0.015	2	1680267120
7	Carton	QX18A	395*290*315	0.58	1	1680104790
8	ESD bag（防静电包装袋）	JD13	400*520	0.042	3	1680213550
9	Total Weight			TBD		

(1) LCM quantity per tray:6
(2) Total LCM quantity per group:48 (8trays×per tray 6 and 1 empty tray)
(3) Total LCM quantity in Carton: Number of PET trays 24× quantity per tray 6 = 144
Note: Please refer to the data from "estimated report about the dimension and stack of Carton" about stacking carton

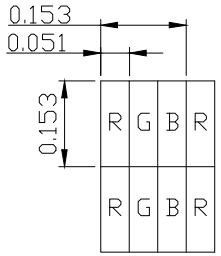








K1 Terminal		K1 Terminal	
No.	Pin Name	No.	Pin Name
1	VSS	26	DB5/B5,Msb
2	IOVDD	27	DB4/B4
3	IOVDD	28	DB3/B3
4	VDD	29	DB2/B2
5	VDD	30	DB1/B1
6	IM0	31	DB0/B0,Lsb
7	IM1	32	VSS
8	IM2	33	DOUT
9	RESX	34	SDA
10	VSYNC	35	RDX
11	HSYNC	36	WRX_SCL
12	PCLK	37	DCX
13	DE	38	CSX
14	DB17/R5,Msb	39	NC(XR)
15	DB16/R4	40	NC(YD)
16	DB15/R3	41	NC(XL)
17	DB14/R2	42	NC(YU)
18	DB13/R1	43	LEDA
19	DB12/R0,Lsb	44	LEDK
20	DB11/G5,Msb	45	LEDK
21	DB10/G4	46	LEDK
22	DB9/G3	47	LEDK
23	DB8/G2	48	LEDK
24	DB7/G1	49	LEDK
25	DB6/G0,Lsb	50	VSS



Pixel Details
Scale=100/1

Note:
*1. LCD Display Type : TFT,Transmissive
*2. Pixel Arrangment : RGB-STRIPE
*3. Color Depth : 262k Color
*4. Operating Voltage(VDD , IOVDD) : 3.0V
*5. Backlight : White LEDs
*6. Backlight Supply : 6x20mA (VF=3.2V, TYP)
*7. Recommended Connector K1: FH19SC-50S-0.5SH(HIROS) Or Equivalent
*8. Operating Temperature : -20°C~70°C
*9. Storage Temperature : -30°C~80°C

Rev	Note	Date
C		
B		
A		

Dwg Title	LMT035DNJFWD-1 Outline Dwg		
Dwg No.	MK-007050-1-1		Date 2020-09-16
Scale 5/4	Tol. ±0.3	Unit mm	Paper Size A3
Approved	Checked		Drawn Qiu Shaoping

TOPWAY