



深圳市拓普微科技开发有限公司

SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

# LMT035DNJFWD-NAN

## LCD Module User Manual

|                  |             |              |
|------------------|-------------|--------------|
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| Date: 2023-08-31 | Date:       | Date:        |

| Rev. | Descriptions                                                                                            | Release Date |
|------|---------------------------------------------------------------------------------------------------------|--------------|
| 0.1  | Preliminary New release                                                                                 | 2020-06-22   |
| 0.2  | Update Electrical Characteristics                                                                       | 2020-07-16   |
| 0.3  | Add interface mode selection                                                                            | 2022-07-06   |
| 0.4  | Update Basic Specifications and the hardware system interface selection of the 1.2 terminal function    | 2023-03-29   |
| 0.5  | Modify 1.2 Terminal Function Description, Unified I/O voltage name                                      | 2023-04-12   |
| 0.6  | Modify 1.2 Hardware system interface select of 4-SPI, Remove CTP /RTP Mounting Instructions for 7 and 8 | 2023-08-31   |

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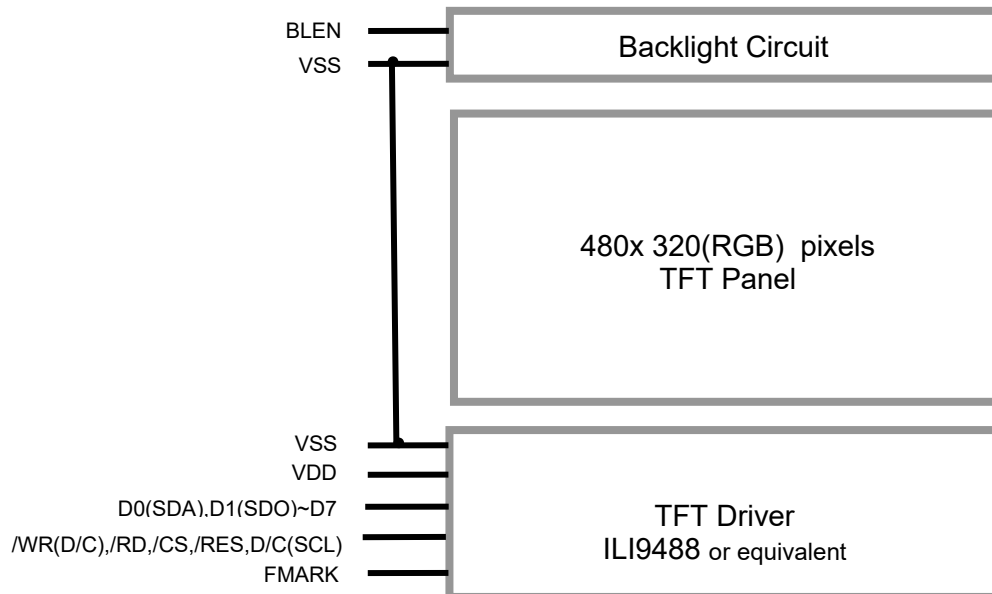
## 1. Basic Specifications

|                              |                                                        |
|------------------------------|--------------------------------------------------------|
| Screen Size(Diagonal) :      | 3.5"                                                   |
| Active Area :                | 48.96x73.44(mm)                                        |
| Number of dots :             | 480x320(RGB)                                           |
| Pixel Pitch:                 | 0.153x0.153(mm)                                        |
| Color Depth:                 | 65K/262K Color                                         |
| Display Technology :         | a-Si TFT active matrix                                 |
| Display Mode :               | Transmissive With Normally white                       |
| Display Interface :          | RGB                                                    |
| Viewing Direction :          | 3 o' clock (gray scale inverse)(*1)<br>9 o' clock (*2) |
| Polarizer Surface Treatment: | HC                                                     |
| Operating Temperature :      | -20 ~ +70°C (No Condensation)                          |
| Storage Temperature :        | -30 ~ +80°C (No Condensation)                          |

Note:

- \*1. For saturated color display content (eg. pure-red, pure-green, pure-blue or pure-colors-combinations).
- \*2. For "color scales" display content.
- \*3. Color tone may slightly change by temperature and driving condition.

### 1.1 Block Diagram



## 1.2 Terminal Functions

| Pin No.<br>(K1) | Pin Name | I/O | Descriptions                                                                                      |                                                                                    |                                                                |
|-----------------|----------|-----|---------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|----------------------------------------------------------------|
|                 |          |     | 80-8bit(default)                                                                                  | 3-SPI                                                                              | 4-SPI                                                          |
| 1               | VSS      | P   | Negative power supply,0V                                                                          |                                                                                    |                                                                |
| 2               | VSS      |     |                                                                                                   |                                                                                    |                                                                |
| 3               | BLEN     | I   | Backlight enable<br>BLEN = H: turn off Backlight<br>BLEN = L: turn on Backlight (*1)              |                                                                                    |                                                                |
| 4               | VDD      | P   | Positive power supply                                                                             |                                                                                    |                                                                |
| 5               | VDD      |     |                                                                                                   |                                                                                    |                                                                |
| 6               | /RD      | I   | Read enable input, active low                                                                     | Please fix this pin at IOVCC                                                       |                                                                |
| 7               | /WR(D/C) | I   | Write enable input, active low                                                                    | Please fix this pin at IOVCC.                                                      | Display data/command selection pin in 4-line serial interface. |
| 8               | D/C(SCL) | I   | Register Select<br>D/C=H, Transferring the Display Data<br>D/C = L, Transferring the Control Data | This pin is used to be serial interface clock.                                     |                                                                |
| 9               | /CS      | I   | Chip Select<br>/CS=L, enable access to the LCD module<br>/CS=H, disable access to the LCD module  |                                                                                    |                                                                |
| 10              | D0(SDA)  | I/O | Data Input                                                                                        | The data is latched on the rising edge of the SCL signal.                          |                                                                |
| 11              | D1(SDO)  | I/O |                                                                                                   | SPI interface output pin. The data is output on the rising edge of the SCL signal. |                                                                |
| :               | :        | :   |                                                                                                   |                                                                                    |                                                                |
| 17              | D7       | I/O |                                                                                                   | Please fix this pin at IOVCC or GND level.                                         |                                                                |
| 18              | /RES     | I   | Reset signal<br>/RES = L, Initialization is executed<br>/RES = H, Normal running.                 |                                                                                    |                                                                |
| 19              | FMARK    | O   | Displaying Timing Frame Signal                                                                    |                                                                                    |                                                                |
| 20~28           | NC       | -   | -                                                                                                 |                                                                                    |                                                                |

### Hardware system interface select

| Mode              | Install                                | No install    |
|-------------------|----------------------------------------|---------------|
| 80-8bit (default) | R23,R24(0R,0603,5%)                    | R22,R25       |
| 3-SPI             | R22,R25,R7,R8,R9,R10(100R,0603,5%)     | R23,R24,R2,R3 |
| 4-SPI             | R22,R24,R7,R8,R9,R10,R11(100R,0603,5%) | R23,R25,R2,R3 |

Note:

\*1 :The PWM frequency is between 2k Hz and 10kHz.

## 2. Absolute Maximum Ratings

VDD =5V, VSS=0V, T<sub>OP</sub>=25 °C

| Items                 | Symbol          | Min. | Max. | Unit | Condition            |
|-----------------------|-----------------|------|------|------|----------------------|
| Power Voltage         | VDD             | -0.3 | +5.5 | V    | V <sub>SS</sub> = 0V |
| Input Voltage         | V <sub>IN</sub> | -0.3 | +5.5 | V    | V <sub>SS</sub> = 0V |
| Operating Temperature | T <sub>OP</sub> | -20  | +70  | °C   | No Condensation      |
| Storage Temperature   | T <sub>ST</sub> | -30  | +80  | °C   | No Condensation      |

Cautions:

Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

## 3. Electrical Characteristics

### 3.1 DC Characteristics

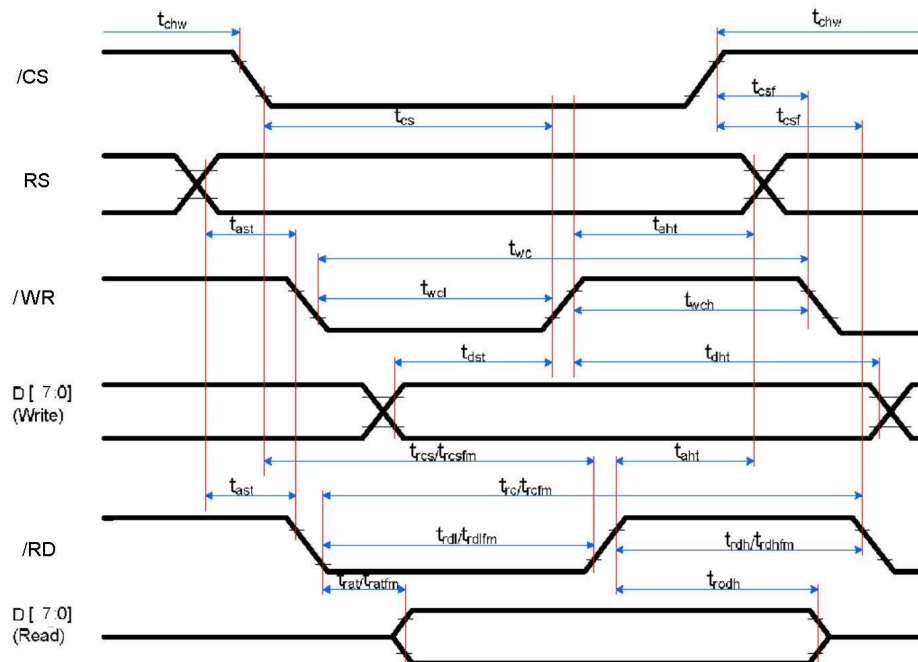
VDD =5V, IOVCC=3.3V, VSS=0V, T<sub>OP</sub>=25°C

| Items               | Symbol          | MIN.      | TYP. | MAX.      | Unit | Condition / Application Pin                                  |
|---------------------|-----------------|-----------|------|-----------|------|--------------------------------------------------------------|
| Operating Voltage   | VDD             | 4.8       | 5.0  | 5.2       | V    | VDD                                                          |
| Input High Voltage  | V <sub>IH</sub> | 0.7*IOVCC | -    | IOVCC     | V    | /RES,D0(SDA),<br>D1(SDO)~D7<br>/CS,/RD,/WR,BLEN,<br>D/C(SCL) |
| Input Low Voltage   | V <sub>IL</sub> | -0.3      | -    | 0.3*IOVCC | V    |                                                              |
| Output High Voltage | V <sub>OH</sub> | 0.8*IOVCC | -    | IOVCC     | V    | D0~D7, SDO, FMARK                                            |
| Output Low Voltage  | V <sub>OL</sub> | 0         | -    | 0.2*IOVCC | V    |                                                              |
| Operating Current   | I <sub>DD</sub> | -         | 105  | -         | mA   | Backlight are ON                                             |
|                     |                 | -         | 4.8  | -         | mA   | Backlight are OFF                                            |

## 4. AC Characteristics

### 4.1 DBI Type B

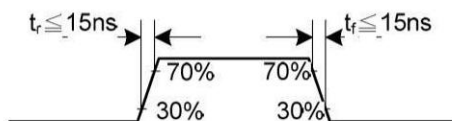
#### 4.1.1 DBI Type B Timing Characteristic



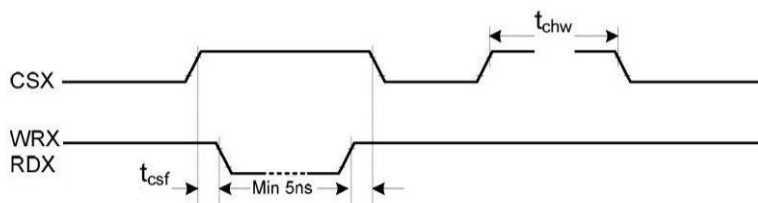
| Signal  | Symbol | Parameter                          | min | max | Unit | Description                                 |
|---------|--------|------------------------------------|-----|-----|------|---------------------------------------------|
| RS      | tast   | Address setup time                 | 0   | -   | ns   | -                                           |
|         | that   | Address hold time (Write/Read)     | 0   | -   | ns   | -                                           |
| /CS     | tchwh  | CSX "H" pulse width                | 0   | -   | ns   | -                                           |
|         | tcs    | Chip Select setup time (Write)     | 19  | -   | ns   | -                                           |
|         | trcs   | Chip Select setup time (Read ID)   | 58  | -   | ns   | -                                           |
|         | trcsfm | Chip Select setup time (Read FM)   | 461 | -   | ns   | -                                           |
|         | tcsf   | Chip Select Wait time (Write/Read) | -   | -   | ns   | -                                           |
| /WR     | twc    | Write cycle                        | 52  | -   | ns   | -                                           |
|         | twrh   | Write Control pulse H duration     | 19  | -   | ns   | -                                           |
|         | twrl   | Write Control pulse L duration     | 19  | -   | ns   | -                                           |
| /RD(FM) | trcfm  | Read Cycle (FM)                    | 585 | -   | ns   | When read from Frame Memory                 |
|         | trdhfm | Read Control H duration (FM)       | 117 | -   | ns   |                                             |
|         | trdlfm | Read Control L duration (FM)       | 461 | -   | ns   |                                             |
| /RD(ID) | trc    | Read cycle (ID)                    | 208 | -   | ns   | When read ID data                           |
|         | trdh   | Read Control pulse H duration      | 117 | -   | ns   |                                             |
|         | trdl   | Read Control pulse L duration      | 58  | -   | ns   |                                             |
| D[7:1]  | tdst   | Write data setup time              | 13  | -   | ns   | For maximum, CL=30pF<br>For minimum, CL=8pF |
|         | tdht   | Write data hold time               | 13  | -   | ns   |                                             |
|         | trat   | Read access time                   | -   | 40  | ns   |                                             |
|         | trafm  | Read access time                   | -   | 340 | ns   |                                             |
|         | trod   | Read output disable time           | 20  | 80  | ns   |                                             |

**Notes:**

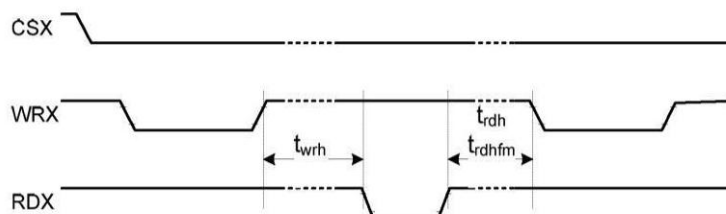
1.  $T_a = -30$  to  $70\text{ }^{\circ}\text{C}$ ,  $\text{IOVCC}$ ,  $\text{VDD} = 2.5\text{V}$  to  $3.3\text{V}$ ,  $\text{VSS} = 0\text{V}$
2. Logic high and low levels are specified as 30% and 70% of  $\text{IOVCC}$  for input signals.
3. Input signal rising time and falling time:



4. The CSX timing:

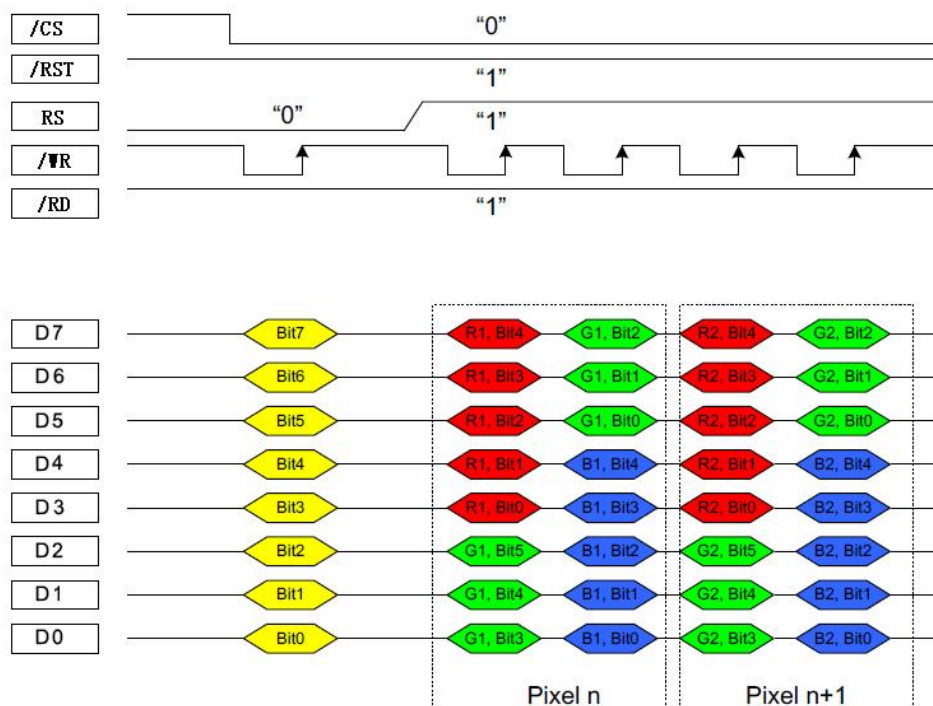


5. The Write to Read or the Read to Write timing:

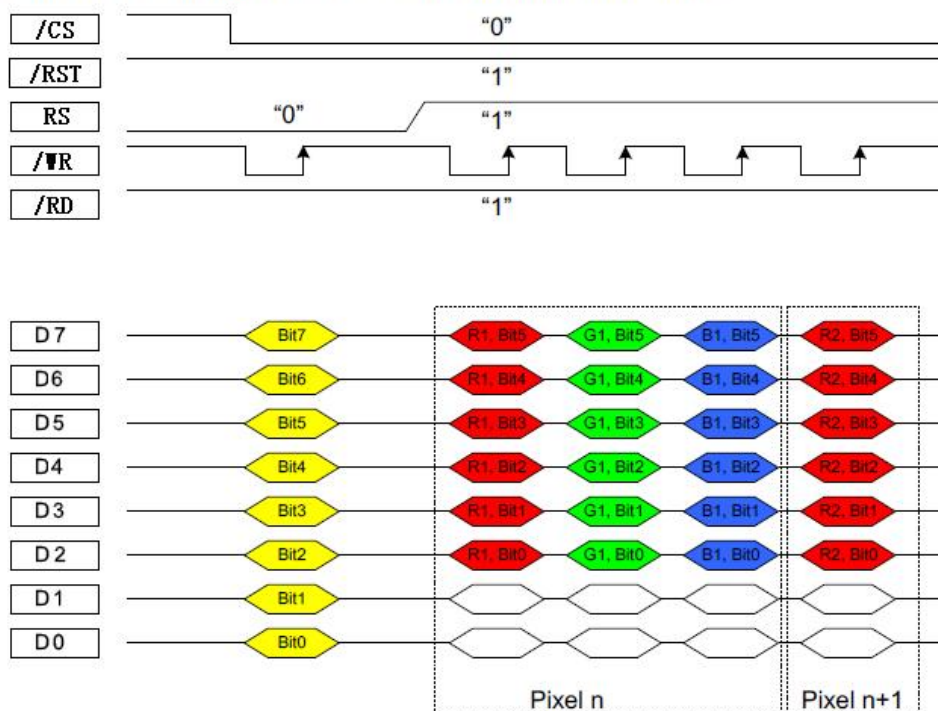


### 4.1.2 DBI Type B Data Bus

#### 8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color

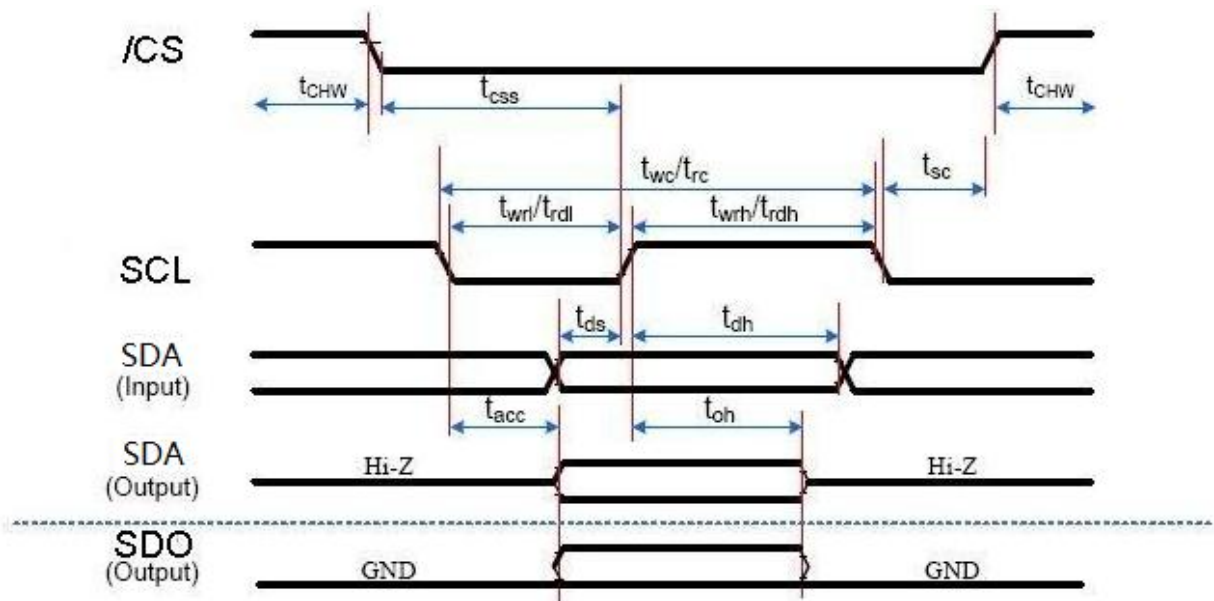


#### 8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



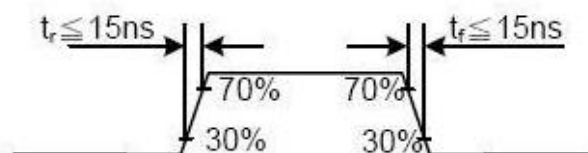


## 4.2 3-Line SPI Interface Timing Characteristic

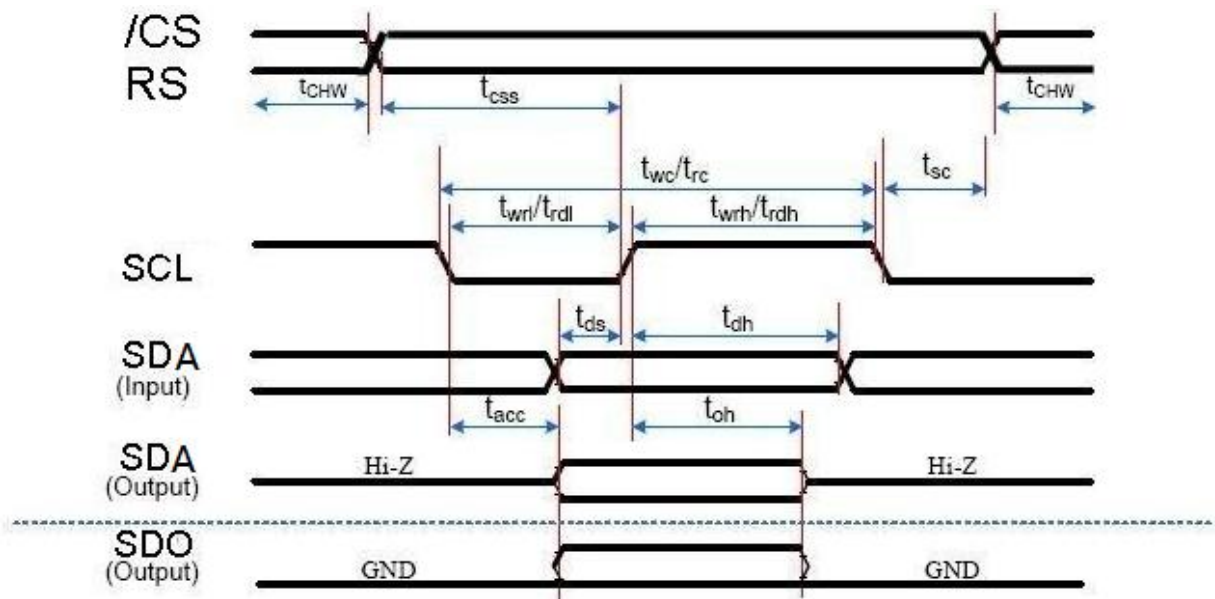


| Signal           | Symbol    | Parameter                     | min | max | Unit | Description         |
|------------------|-----------|-------------------------------|-----|-----|------|---------------------|
| $\overline{CS}$  | $t_{sc}$  | SCL- $\overline{CS}$          | 19  | -   | ns   |                     |
|                  | $t_{chw}$ | $\overline{CS}$ H Pulse Width | 52  | -   | ns   |                     |
|                  | $t_{css}$ | Chip select time (Write)      | 88  | -   | ns   |                     |
|                  | $t_{csh}$ | Chip select hold time (Read)  | 84  | -   | ns   |                     |
| SCL              | $t_{wc}$  | Serial Clock Cycle (Write)    | 85  | -   | ns   |                     |
|                  | $t_{wrh}$ | SCL H Pulse Width (Write)     | 19  | -   | ns   |                     |
|                  | $t_{wrl}$ | SCL L Pulse Width (Write)     | 19  | -   | ns   |                     |
|                  | $t_{rc}$  | Serial Clock Cycle (Read)     | 195 | -   | ns   |                     |
|                  | $t_{rdh}$ | SCL H Pulse Width (Read)      | 78  | -   | ns   |                     |
|                  | $t_{rdl}$ | SCL L Pulse Width (Read)      | 78  | -   | ns   |                     |
| SDA (Input)      | $t_{ds}$  | Data setup time (Write)       | 13  | -   | ns   |                     |
|                  | $t_{dh}$  | Data hold time (Write)        | 13  | -   | ns   |                     |
| SDA/SDO (Output) | $t_{acc}$ | Access time (Read)            | 13  | 65  | ns   | For maximum CL=30pF |
|                  | $t_{oh}$  | Output disable time (Read)    | 19  | 35  | ns   | For minimum CL=8pF  |

Note:  $T_a = -30$  to  $70^\circ\text{C}$ ,  $IOVCC$ ,  $VDD = 2.5\text{V}$  to  $3.3\text{V}$ ,  $VSS = 0\text{V}$ ,  $T = 10 \pm 0.5\text{ns}$

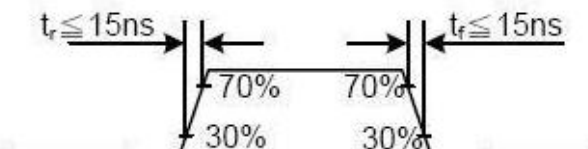


### 4.3 4-Line SPI Interface Timing Characteristic



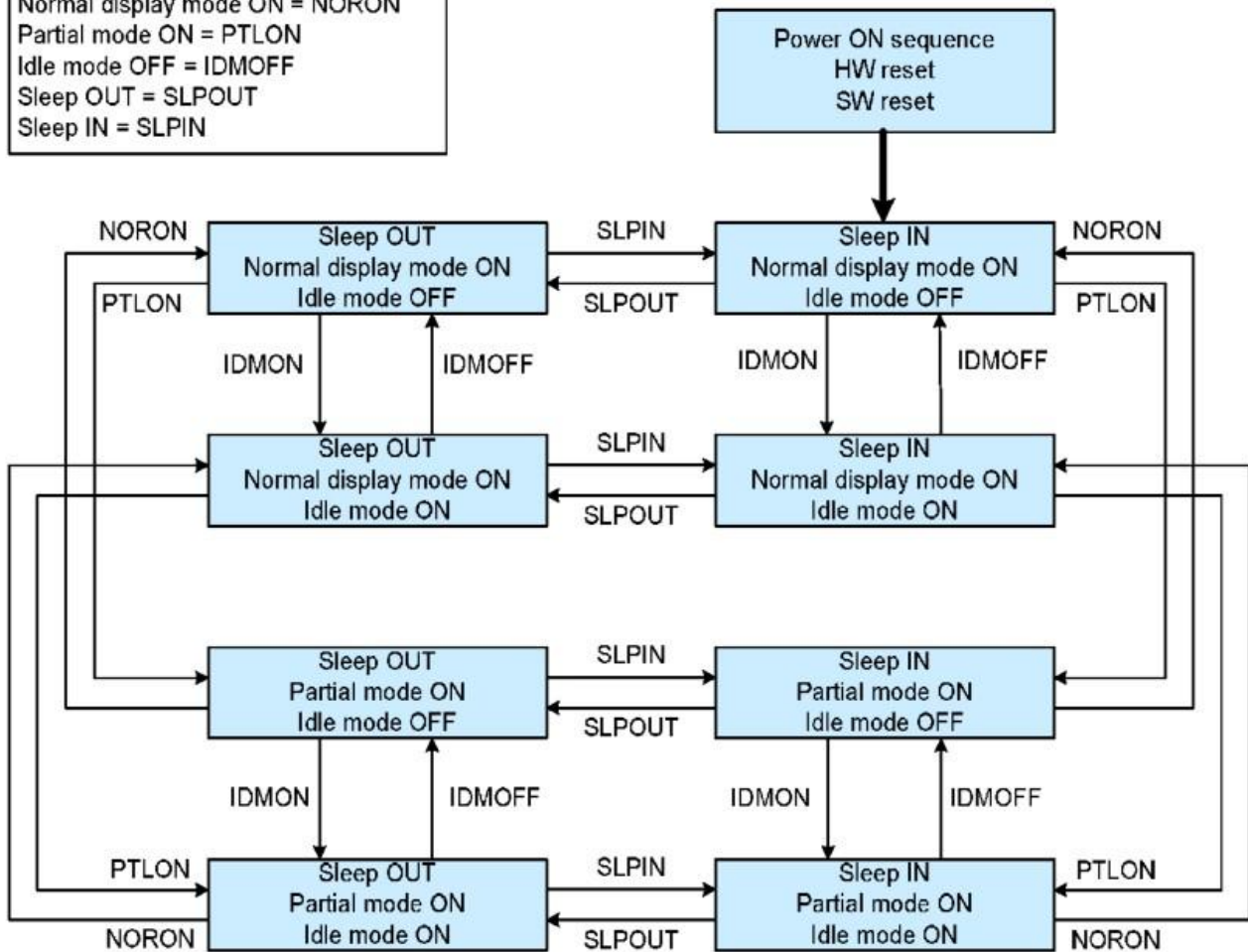
| Signal                              | Symbol           | Parameter                            | min | max | Unit | Description                         |
|-------------------------------------|------------------|--------------------------------------|-----|-----|------|-------------------------------------|
| $\overline{\text{CS}}$              | $t_{\text{sc}}$  | SCL- $\overline{\text{CS}}$          | 19  | -   | ns   |                                     |
|                                     | $t_{\text{chw}}$ | $\overline{\text{CS}}$ H Pulse Width | 52  | -   | ns   |                                     |
|                                     | $t_{\text{css}}$ | Chip select time (Write)             | 88  | -   | ns   |                                     |
|                                     | $t_{\text{csh}}$ | Chip select hold time (Read)         | 84  | -   | ns   |                                     |
| $\text{SCL}$                        | $t_{\text{wc}}$  | Serial Clock Cycle (Write)           | 85  | -   | ns   |                                     |
|                                     | $t_{\text{wrh}}$ | SCL H Pulse Width (Write)            | 19  | -   | ns   |                                     |
|                                     | $t_{\text{wrl}}$ | SCL L Pulse Width (Write)            | 19  | -   | ns   |                                     |
|                                     | $t_{\text{rc}}$  | Serial Clock Cycle (Read)            | 195 | -   | ns   |                                     |
|                                     | $t_{\text{rdh}}$ | SCL H Pulse Width (Read)             | 78  | -   | ns   |                                     |
|                                     | $t_{\text{rdl}}$ | SCL L Pulse Width (Read)             | 78  | -   | ns   |                                     |
| $\text{SDA}$<br>(Input)             | $t_{\text{ds}}$  | Data setup time (Write)              | 13  | -   | ns   |                                     |
|                                     | $t_{\text{dh}}$  | Data hold time (Write)               | 13  | -   | ns   |                                     |
| $\text{SDA}/\text{SDO}$<br>(Output) | $t_{\text{acc}}$ | Access time (Read)                   | 13  | 65  | ns   | For maximum $\text{CL}=30\text{pF}$ |
|                                     | $t_{\text{oh}}$  | Output disable time (Read)           | 34  | 35  | ns   | For minimum $\text{CL}=8\text{pF}$  |

Note:  $T_a = -30$  to  $70^\circ\text{C}$ ,  $\text{IOVCC}$ ,  $\text{VDD} = 2.5\text{V}$  to  $3.3\text{V}$ ,  $\text{VSS} = 0\text{V}$ ,  $T = 10 \pm 0.5\text{ns}$



#### 4.5 Power ON/OFF Sequence

Normal display mode ON = NORON  
 Partial mode ON = PTLON  
 Idle mode OFF = IDMOFF  
 Sleep OUT = SLPOUT  
 Sleep IN = SLPIN



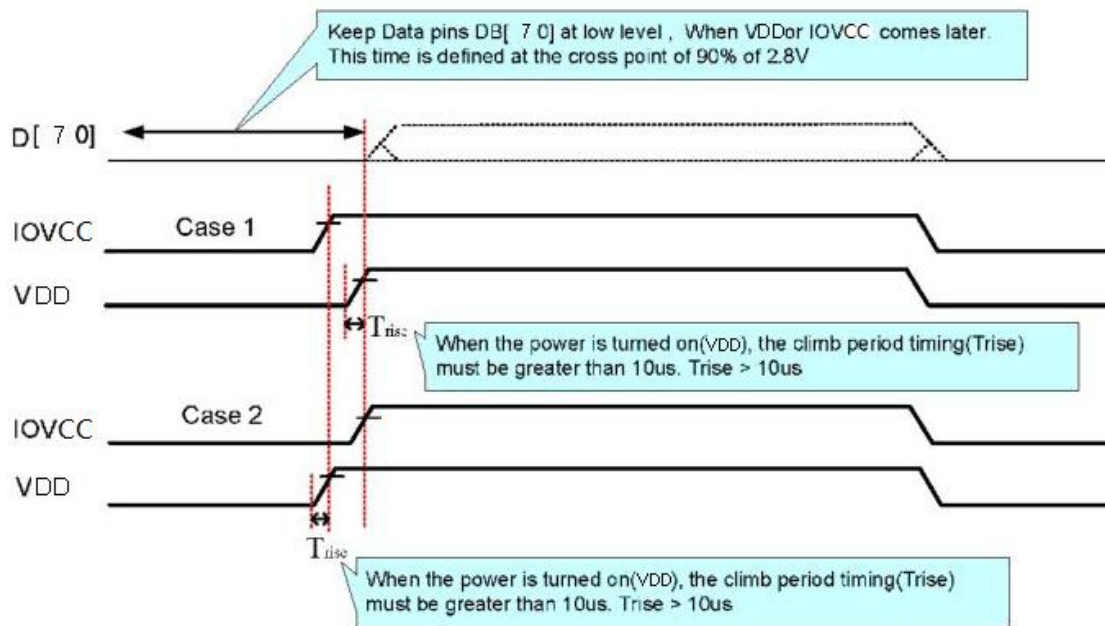
#### Notes:

1. There are not any abnormal visual effects when one power mode changes to another power mode.
2. There is not any limitation, which is not specified by users, when one power mode changes to another power mode.

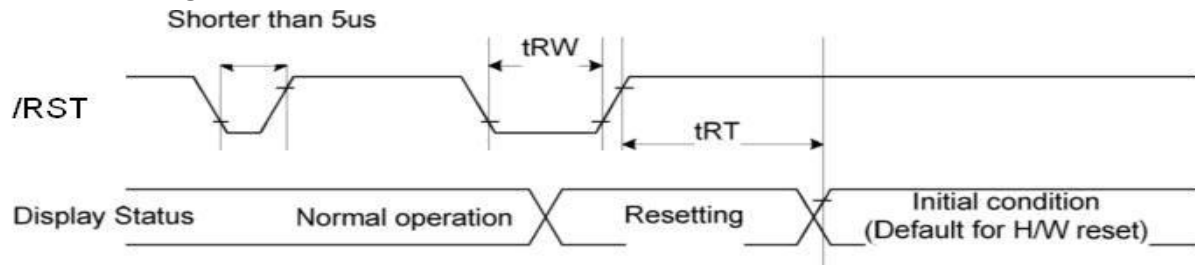
IOVCC and VDD can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep In mode, VDD and IOVCC must be powered down with a minimum of 120 msec. If the LCD is in the Sleep In mode, VDD and IOVCC can be powered down with a minimum of 0msec after the /RST has been released. /CS can be applied at any time or can be permanently grounded. /RST has priority over /CS.

**Notes:**

1. There will be no damage to the ILI9488 if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequence.
3. There will be no abnormal visible effects on the display between the end of the Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the /RST line is not steadily held by the host during the Power On Sequence as defined in Sections 11.1 and 11.2 ( ILI9488 datasheet ), then it will be necessary to apply the Hardware /RST after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.
5. When the power is turned on, the climb period timing ( $T_{rise}$ ) must be greater than 10us.
6. Keep data pins D[17:0] at low level, or IOVCC comes later



#### 4.6 Reset timing



| Item                  | Symbol   | MIN. | TYP. | MAX. | Unit |
|-----------------------|----------|------|------|------|------|
| Reset LOW pulse width | $t_{RW}$ | 1.0  | -    | -    | us   |
| Reset time            | $T_{RT}$ | -    | -    | 120  | ms   |

### 5 . Optical Characteristics

| Item           |       | Symbol           | Condition       | Min | Typ   | Max | Unit              | Remark   |
|----------------|-------|------------------|-----------------|-----|-------|-----|-------------------|----------|
| View Angles    |       | θT               | CR≧10           | 60  | 70    |     | Degree            | Note2,3  |
|                |       | θB               |                 | 50  | 60    |     |                   |          |
|                |       | θL               |                 | 60  | 70    |     |                   |          |
|                |       | θR               |                 | 60  | 70    |     |                   |          |
| Contrast Ratio |       | CR               | θ=0°            | 400 | 500   |     |                   | Note 3   |
| Response Time  |       | T <sub>ON</sub>  | 25℃             |     | 25    | 35  | ms                | Note 4   |
|                |       | T <sub>OFF</sub> |                 |     |       |     |                   |          |
| Chromaticity   | White | x                | Backlight is on |     | 0.286 |     |                   | Note 1,5 |
|                |       | y                |                 |     | 0.304 |     |                   |          |
|                | Red   | x                |                 |     | 0.608 |     |                   | Note 1,5 |
|                |       | y                |                 |     | 0.336 |     |                   |          |
|                | Green | x                |                 |     | 0.341 |     |                   | Note 1,5 |
|                |       | y                |                 |     | 0.604 |     |                   |          |
|                | Blue  | x                |                 |     | 0.146 |     |                   | Note 1,5 |
|                |       | y                |                 |     | 0.073 |     |                   |          |
| Uniformity     |       | U                |                 |     | 80    |     | %                 | Note 6   |
| NTSC           |       |                  |                 |     | 60    |     | %                 | Note 5   |
| Luminance      |       | L                |                 | 250 |       |     | cd/m <sup>2</sup> | Note 7   |

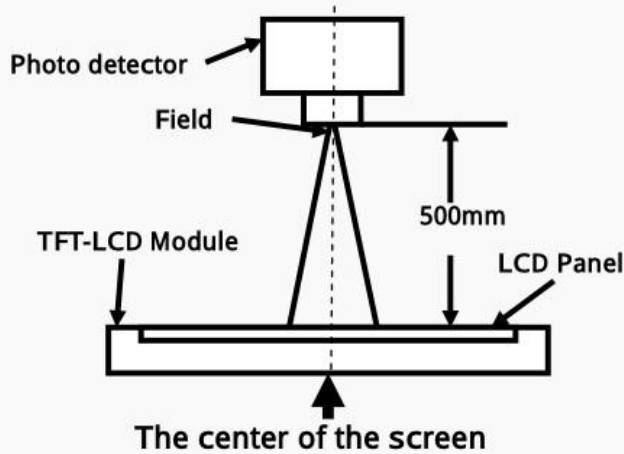
Test Conditions:

1.  $I_{BLA} = 120 \text{ mA}$ , and the ambient temperature is  $25^\circ C$ .
2. The test systems refer to Note 1 and Note 2.



Note 1: Definition of optical measurement system.

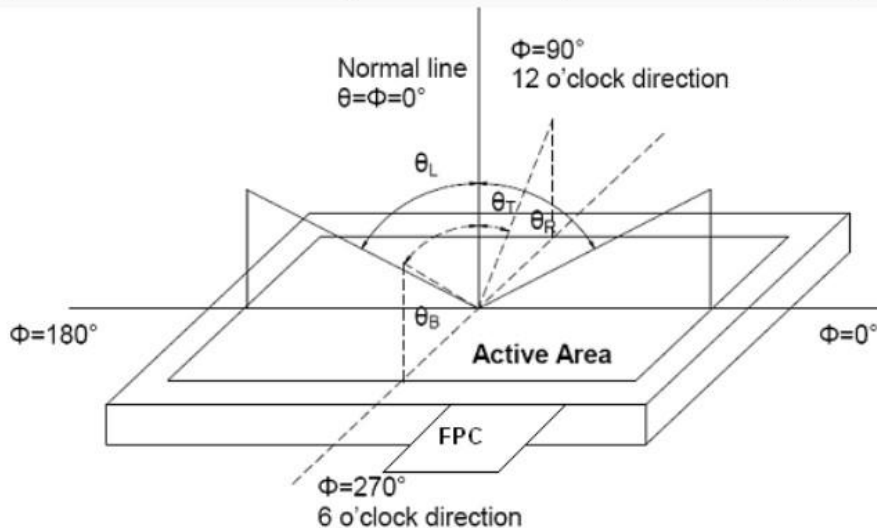
The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



| Item           | Photo detector | Field |
|----------------|----------------|-------|
| Contrast Ratio | SR-3A          | 1°    |
| Luminance      |                |       |
| Chromaticity   |                |       |
| Lum Uniformity |                |       |
| Response Time  | BM-7A          | 2°    |

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

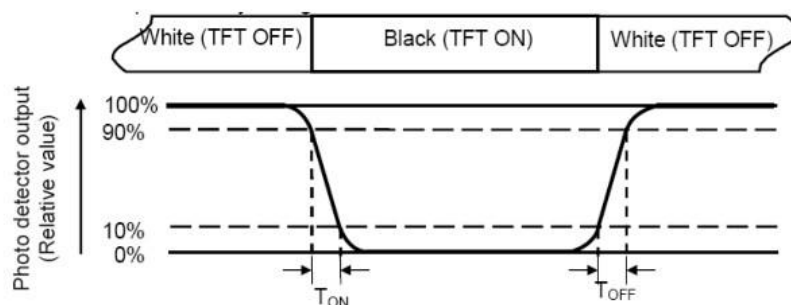
"White state ": The state is that the LCD should drive by V<sub>white</sub>.

"Black state": The state is that the LCD should drive by V<sub>black</sub>.

V<sub>white</sub>: To be determined    V<sub>black</sub>: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time ( $T_{ON}$ ) is the time between photo detector output intensity changed from 90% to 10%. And fall time ( $T_{OFF}$ ) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

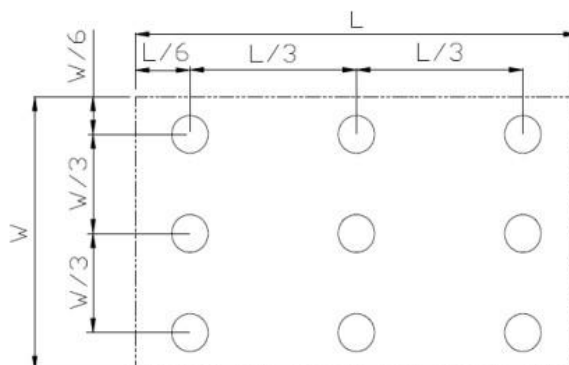
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity ( $U$ ) =  $L_{min} / L_{max}$

L-----Active area length W----- Active area width



$L_{max}$ : The measured Maximum luminance of all measurement position.

$L_{min}$ : The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

## 6. LCD Module Design and Handling Precautions

- Please ensure V0, VCOM is adjustable, to enable LCD module get the best contrast ratio under different temperatures, view angles and positions.
- Normally display quality should be judged under the best contrast ratio within viewable area. Unexpected display pattern may come out under abnormal contrast ratio.
- Never operate the LCD module exceed the absolute maximum ratings.
- Never apply signal to the LCD module without power supply.
- Keep signal line as short as possible to reduce external noise interference.
- IC chip (e.g. TAB or COG) is sensitive to light. Strong light might cause malfunction. Light sealing structure casing is recommended.
- Make sure there is enough space (with cushion) between case and LCD panel, to prevent external force passed on to the panel; otherwise that may cause damage to the LCD and degrade its display result.
- Avoid showing a display pattern on screen for a long time (continuous ON segment).
- LCD module reliability may be reduced by temperature shock.
- When storing and operating LCD module, avoids exposure to direct sunlight, high humidity, high or low temperature. They may damage or degrade the LCD module.
- Never leave LCD module in extreme condition (max./min-storage/operate temperature) for more than 48hr.
- Recommend LCD module storage conditions is 0°C~40°C <80%RH.
- LCD module should be stored in the room without acid, alkali and harmful gas.
- Avoid dropping & violent shocking during transportation, and no excessive pressure press, moisture and sunlight.
- LCD module can be easily damaged by static electricity. Please maintain an optimum anti-static working environment to protect the LCD module. (eg. ground the soldering irons properly)
- Be sure to ground the body when handling LCD module.
- Only hold LCD module by its sides. Never hold LCD module by applying force on the heat seal or TAB.
- When soldering, control the temperature and duration avoid damaging the backlight guide or diffuser which might degrade the display result such as uneven display.
- Never let LCD module contact with corrosive liquids, which might cause damage to the backlight guide or the electric circuit of LCD module.
- Only clean LCD with a soft dry cloth, Isopropyl Alcohol or Ethyl Alcohol. Other solvents (e.g. water) may damage the LCD.
- Never add force to components of LCD module. It may cause invisible damage or degrade the module's reliability.
- When mounting LCD module, please make sure it is free from twisting, warping and bending.

## 6. 液晶显示模块设计和使用须知

请注意 V0, VCOM 的设定, 以确保液晶显示模块在不同的使用温度下以及在不同的视角和位置观察模块显示, 均能达到最佳对比度, 请务必将应用电路上设置为对比度可调。

请注意液晶显示模块的显示品质判定是指在正常对比度下以及视窗 (V.A) 范围内进行的, 非正常对比度下液晶可能会出现非预期的显示不良, 应注意区分。

请勿在最大额定值以外使用液晶显示模块。

请勿在没有接通电源的条件下, 给液晶显示模块输送信号。

请尽可能缩短信号线的连接, 以避免对液晶显示模块的信号干扰。

集成电路因 IC 芯片 (如 TAB 或 COG) 对紫外线极为敏感, 强光环境下可能会引起液晶显示模块功能失效, 故应采用不透光的外壳。

请在液晶显示模块与外壳之间保留足够的空间 (可使用衬垫), 以缓冲外力对液晶显示模块的损坏或因受力不均而产生的显示不匀等异常现象。

避免液晶显示屏在某一画面下长时间点亮, 否则有出现残影的风险; 请通过软件每隔一段时间改变一次画面。

液晶显示模块的可靠性可能因温度冲击而降低。

请勿在阳光直射、高湿、高温或低温下储存和使用液晶显示模块, 这将造成液晶显示模块的损坏或失效。

请勿在极限环境 (最大/最小存储/工作温度) 下使用或放置液晶显示模块超过 48 小时以上。

液晶显示模块建议存储条件为: 0°C~40°C <80%RH。

请勿让液晶显示模块存储于带有酸性、碱性、有害气体环境之中。

在运输过程中, 请勿让液晶显示模块跌落与猛烈震动, 同时避免异常挤压, 高湿度, 与阳光照射。

液晶显示模块极易受静电损坏, 请务必保证液晶显示模块在防静电的工作环境中使用或保存。(如: 烙铁正确接地, 等)

拿取液晶显示模块时需注意操作人员的接地情况。

请手持液晶显示模块的边沿取放模块, 防止热压纸或 TAB 部位受力。

焊接液晶模块时, 请注意控制烙铁的温度、焊接时间, 以免烫坏导光板或偏光片, 导致显示不匀等不良现象发生。

请勿使用洗板水等腐蚀性液体接触液晶模块, 以免腐蚀导光板或模块电路。

仅可使用柔软的干布, 异丙醇或乙醇清洁液晶屏表面, 其他任何溶剂 (如: 水) 都有可能损坏液晶模块。

请勿挤压液晶显示模块上的元器件, 以避免产生潜在的损坏或失效而影响产品可靠性。

装配液晶显示模块时, 请务必注意避免液晶显示模块的扭曲或变形。



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| <ul style="list-style-type: none"><li>- Do not add excessive force on surface of LCD, which may cause the display color change abnormally.</li><li>- LCD panel is made with glass. Any mechanical shock (e.g. dropping from high place) will damage the LCD module.</li><li>- Protective film is attached on LCD screen. Be careful when peeling off this protective film, since static electricity may be generated.</li><li>- Polarizer on LCD gets scratched easily. If possible, do not remove LCD protective film until the last step of installation.</li><li>- When peeling off protective film from LCD, static charge may cause abnormal display pattern. The symptom is normal, and it will turn back to normal in a short while.</li><li>- LCD panel has sharp edges, please handle with care.</li><li>- Never attempt to disassemble or rework LCD module.</li><li>- If display panel is damaged and liquid crystal substance leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes promptly wash it off using soap and water.</li></ul> | <p>请勿挤压液晶显示屏表面，这将导致显示颜色的异常。</p> <p>液晶屏由玻璃制作而成，任何机械碰撞（如从高处跌落）均有可能损坏液晶显示模块。</p> <p>液晶屏表面带有保护膜，揭除保护膜时需要注意可能产生的静电。</p> <p>因液晶显示屏表面的偏光片极易划伤，安装完成之前请尽量不要揭下保护膜。</p> <p>请缓慢揭除保护膜，在此过程中液晶显示屏上可能会产生静电，此为正常情况，可在短时间内消失。</p> <p>请注意避免被液晶显示屏的边缘割伤。</p> <p>请不要试图拆卸或改造液晶显示模块。</p> <p>当液晶显示屏出现破裂，内部液晶液体可能流出；相关液体不可吞吃，绝对不可接触嘴巴，如接触到皮肤或衣服，请使用肥皂与清水彻底清洗。</p> |
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## Warranty

This product has been manufactured to our company's specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

- We cannot accept responsibility for any defect, which may arise from additional manufacturing of the product (including disassembly and reassembly), after product delivery.
- We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
- We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed our company's acceptance inspection procedures.
- When the product is in CCFL models, CCFL service life and brightness will vary according to the performance of the inverter used, leaks, etc. We cannot accept responsibility for product performance, reliability, or defect, which may arise.
- We cannot accept responsibility for intellectual property of a third part, which may arise through the application of our product to our assembly with exception to those issues relating directly to the structure or method of manufacturing of our product.

