深圳市拓普微科技开发有限公司
SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LMT035DNJFWD-NNA-1

LCD Module User Manual

Prepared by:	Checked by:	Approved by:
Li Yongzheng		
Date: 2023-08-23	Date:	Date:

Rev.	Descriptions	Release Date
0.1	Preliminary New release	2020-08-18
0.2	Update DC Characteristics	2022-02-23
0.3	Update Outline Dwg	2022-09-15
0.4	Update Outline Dwg And Mounting Instructions	2023-08-23

Table of Content

1. Basic Specifications 3

1.1 Block Diagram 3
1.2 Terminal Functions 4

2. Absolute Maximum Ratings 5

3. Electrical Characteristics 5

3.1 DC Characteristics 5
3.2 LED Backlight Circuit Characteristics 6

4. AC Characteristics 6

4.1 DBI Type B 6
4.2 3-Line SPI Interface Timing Characteristic 11
4.3 4-Line SPI Interface Timing Characteristic 12
4.4 DPI Interface 13
4.5 Power ON/OFF Sequence 16
4.6 Reset timing 17

5 . Optical Characteristics 18

6. LCD Module Design and Handling Precautions 21
7. RTP Mounting Instructions 22

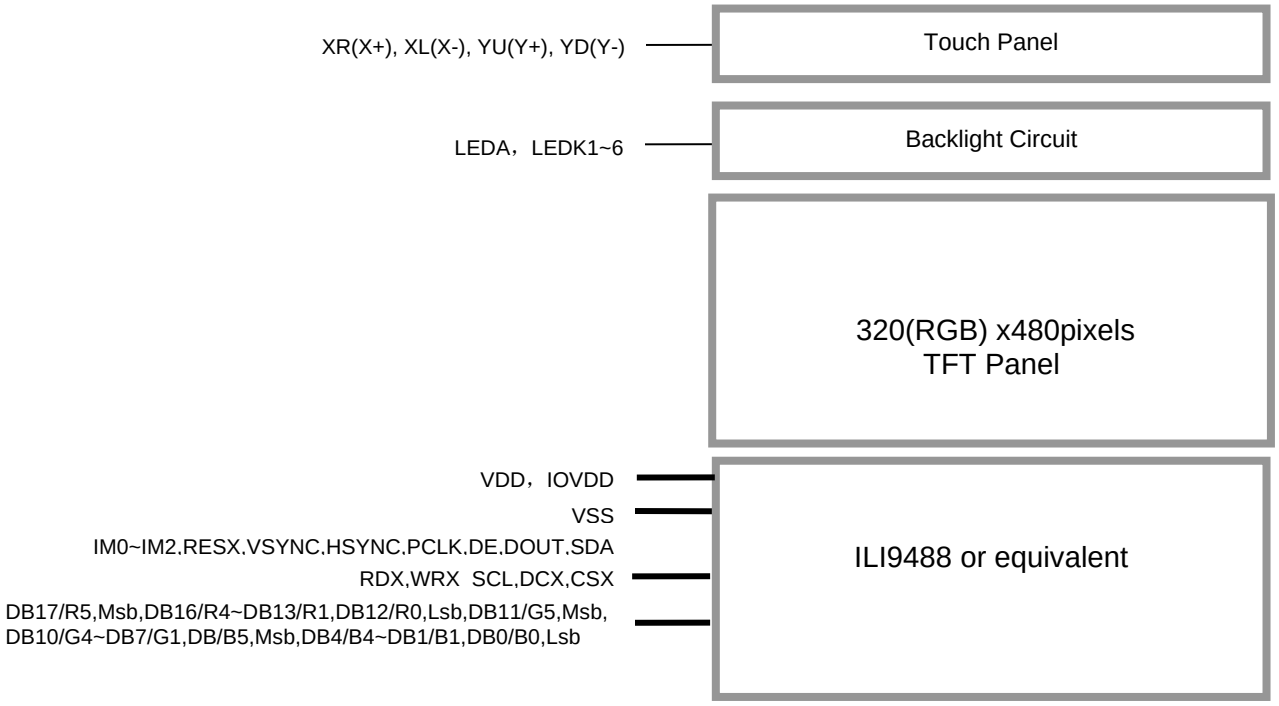
1. Basic Specifications

Screen Size(Diagonal) :	3.5”
Color Depth:	65K/262K Color
Number of dots :	320(RGB)x480
Active Area :	48.96x73.44
Dot Pitch :	0.153x0.153mm
Display Technology :	a-Si TFT active matrix
Display Mode :	Transmissive With Normally white
Pixel Configuration :	RGB Vertical Stripe
Viewing Direction :	12H (*1) (gray scale inverse) 6H (*2)
Polarizer Surface Treatment:	HC
Backlight Type:	LEDs
Outline Dimension :	55.26x 84.69 x 4.6 mm (exclude FPC , see dwg for details)
Operating Temperature :	-20 ~ +70°C (No Condensation)
Storage Temperature :	-30 ~ +80°C (No Condensation)

Note:

*1. For saturated color display content (eg. pure-red, pure-green, pure-blue or pure-colors-combinations).
*2. For “color scales” display content.
*3. Color tone may slightly change by temperature and driving condition.

1.1 Block Diagram



1.2 Terminal Functions

Pin No.	PIN Name	I/O	Descriptions
1	VSS	Power	Negative power supply,0V
2,3	IOVDD	Power	IO Positive Power
4,5	VDD	Power	Positive power supply
6	IM0	Input	MPU system interface mode select
7	IM1	Input	MPU system interface mode select
8	IM2	Input	MPU system interface mode select
9	RESX	Input	Reset signal RESX = L, Initialization is executed RESX = H, Normal running.
10	VSYNC	Input	Vertical sync. signal in RGB mode If no used, please connect this pin to VSS
11	HSYNC	Input	Horizontal sync, signal in RGB mode If no used, please connect this pin to VSS
12	PCLK	Input	Pixel clock signal in RGB mode If no used, please connect this pin to VSS
13	DE	Output	Data enable signal in RGB mode If no used, please fix this pin at VSS level
14	DB17/R5,Msb	I/O	Data Bus
15	DB16/R4	I/O	
:	:	:	
18	DB13/R1	I/O	
19	DB12/R0,Lsb	I/O	
20	DB11/G5,Msb	I/O	
21	DB10/G4	I/O	
:	:	:	
24	DB7/G1	I/O	
25	DB6/G0,Lsb	I/O	
26	DB5/B5,Msb	I/O	
27	DB4/B4	I/O	
:	:	:	
30	DB1/B1	I/O	
31	DB0/B0,Lsb	I/O	
32	VSS	Power	Negative power supply,0V
33	DOUT	Output	Serial data output pin If no used, leave this pin open
34	SDA	I/O	serial data input /output bi-direction pin
35	RDX	Input	serve as a read signal
36	WRX_SCL	Input	(WR) Write data enable pin in DBI Type B (SCL) Write data enable pin in DBI Type C If no used, please connect this pin to IOVDD
37	DCX	Input	Data/Command Selection pin Low: Command High: Parameter
38	CSX	Input	Chip select signal If no used, please connect this pin to IOVDD
39	XR(X+)	Passive	Right Side sense Terminal
40	YD(Y-)		Down Side sense Terminal
41	XL(X-)		Left Side sense Terminal
42	YU(Y+)		Up Side sense Terminal
43	LEDA	Power	LED ANODE
44~49	LEDK	Power	LEDK CATHODE
50	VSS	Power	Negative power supply,0V

IM2	IM1	IM0	Interface	WR/SCL	DATA Bus use	
					Command/Parament	GRAM
0	0	0	DBITYPE-B18-bit (DB_EN='0')	WR	DB7~DB0	DB17 ~DB0:18bits Data
0	0	1	DBI TYPE-B 9-bit	WR	DB7~DB0	DB8 ~DB0: 9bits Data
0	1	0	DBI TYPE-B 16-bit	WR	DB7~DB0	DBI5~DB0:16bits Data
0	1	1	DBI TYPE-B 8-bit	WR	DB7~DB0	DB7 -DB0:8bits Data
1	0	1	DBI TYPE-C Option 1(3 wire)	SCL	SDA/DOUT	
1	1	1	DBI TYPE-C Option 3(4 wire)	SCL	SDA/DOUT	

System interface select

2. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Power Voltage	VDD	-0.3	+3.6	V	V_{SS} = 0V
Input Voltage	V_{IN}	-0.3	+3.6	V	V_{SS} = 0V
Operating Temperature	T_{OP}	-20	+70	°C	No Condensation
Storage Temperature	T_{ST}	-30	+80	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

3. Electrical Characteristics

3.1 DC Characteristics

V_{SS}=0V, T_{OP}=25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition / Application Pin
Operating Voltage	VDD	2.65	3.0	3.6	V	VDD,IOVDD
Input High Voltage	V_{IH}	0.7xV_{DD}	-	V_{DD}	V	IM0~IM2,RESX,VSYNC,HSYNC,PCLK,DB17/R5,Msb, DB16/R4~DB13/R1 ,DB12/R0,Lsb,DB11/G5,Msb, DB10/G4~DB7/G1 ,DB6/G0,Lsb,DB5/B5,Msb, DB4/B4~DB1/B1,DB0/B0,Lsb, SDA,RDX,WRX_SCL,DCX, CSX,
Input Low Voltage	V_{IL}	-0.3	-	0.3xV_{DD}	V	
Output Low Voltage	V_{OL}	0	-	0.99	V	DB17/R5,Msb, DB16/R4~DB13/R1 ,DB12/R0,Lsb,DB11/G5,Msb, DB10/G4~DB7/G1 ,DB6/G0,Lsb,DB5/B5,Msb, DB4/B4~DB1/B1,DB0/B0,Lsb, DE,SDA,DOUT
Operating Current	I_{DD}	-	8	-	mA	VDD (*1)

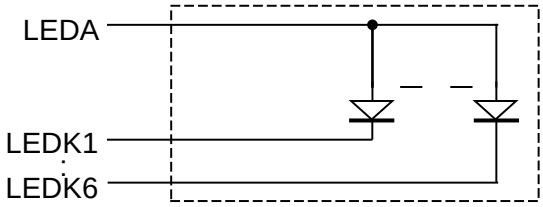
Note: *1. VDD=3.0V

3.2 LED Backlight Circuit Characteristics

LEDK(1~6)=0V, I_{LEDA}=120mA, T_{OP} =25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Forward Voltage	LEDA	-	3.2	-	V	LEDA
Forward Current	I_{LEDA}	-	120	-	mA	LEDA

Cautions:
Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.

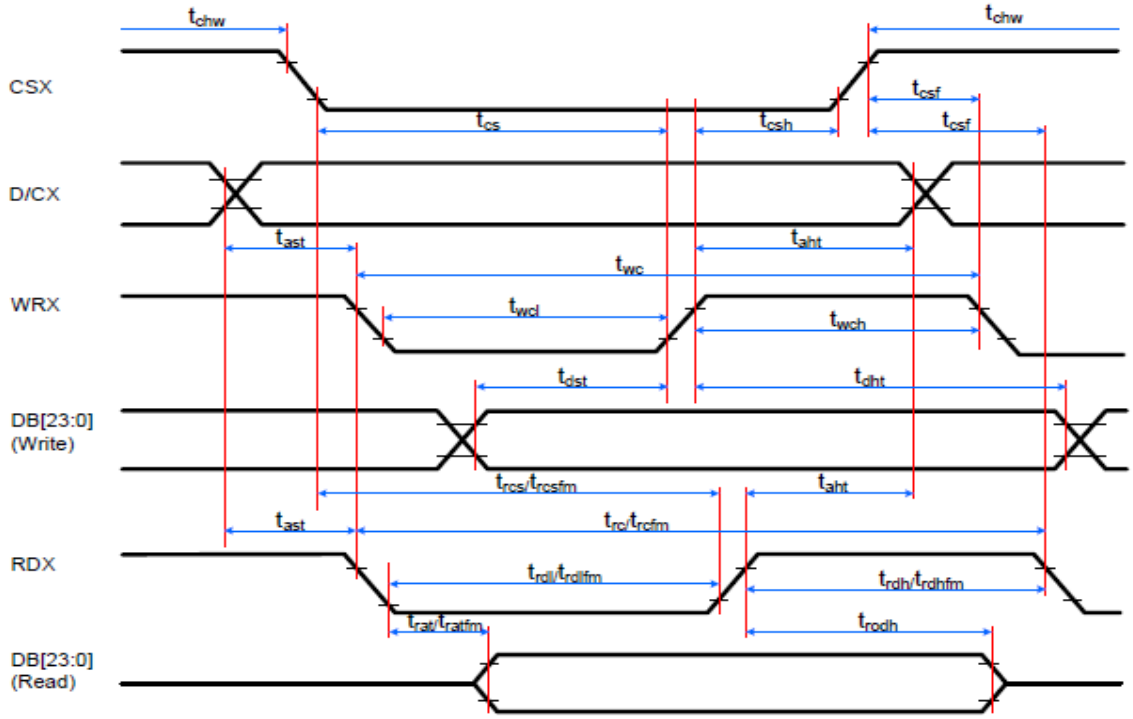


No.of LEDs = 6pcs

4. AC Characteristics

4.1 DBI Type B

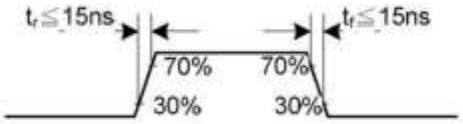
4.1.1 DBI Type B Timing Characteristic



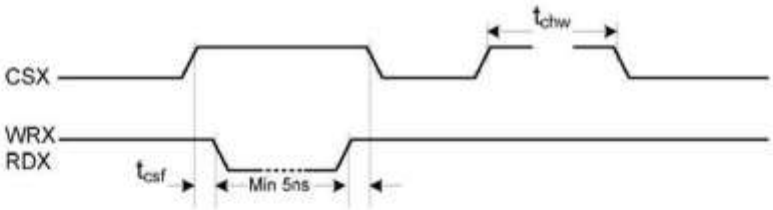
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	taht	Address hold time (Write/Read)	0	-	ns	-
CSX	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
WRX	twc	Write cycle	40	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB [23:0], DB [17:0], DB [15:0], DB [8:0], DB [7:0]	tdst	Write data setup time	10	-	ns	For maximum, CL=30pF For minimum, CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Notes:

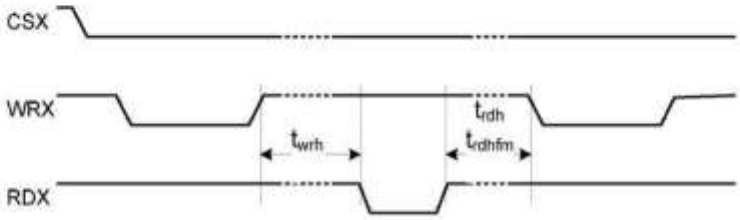
1. Ta = -30 to 70 °C, IOVDD. VDD = 2.5V to 3.3V, VSS = 0V
2. Logic high and low levels are specified as 30% and 70% of IOVDD for input signals.
3. Input signal rising time and falling time:



4. The CSX timing:

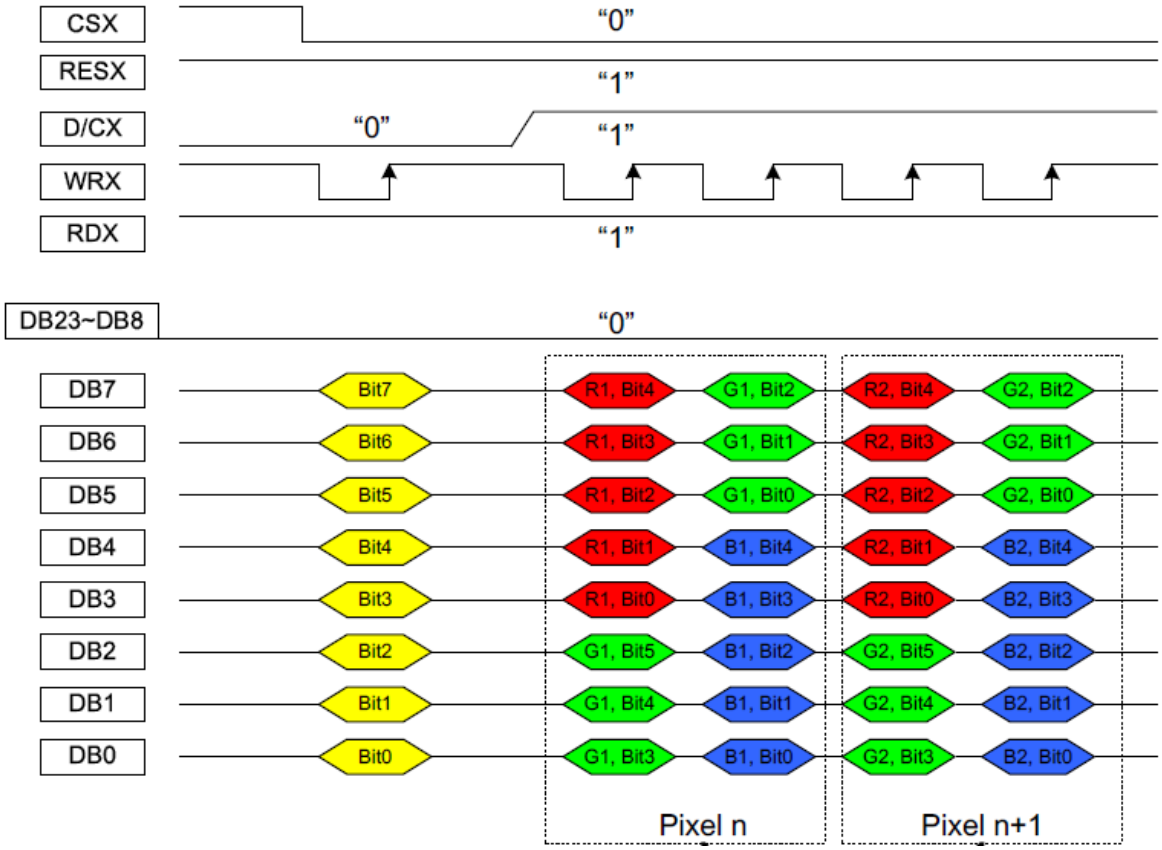


5. The Write to Read or the Read to Write timing:



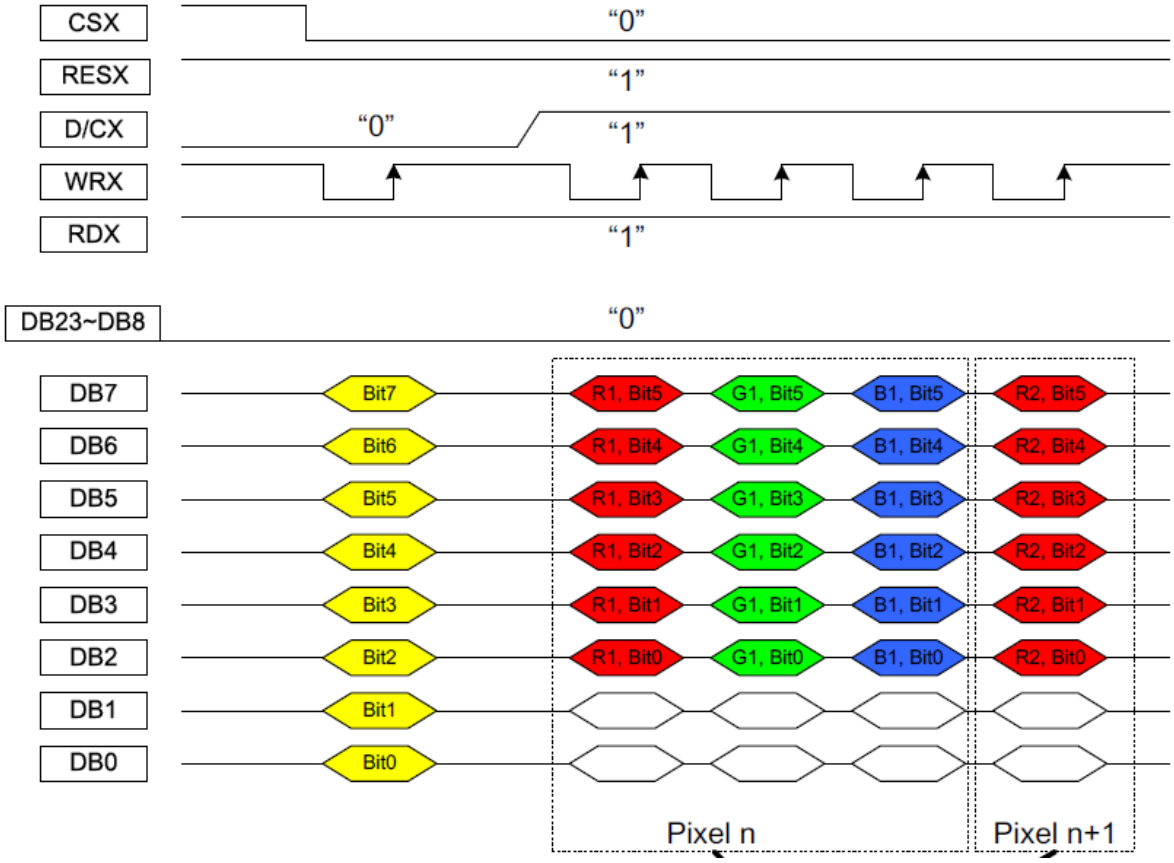
Please refer to IC: ILI9488 data sheet for more details.

8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color

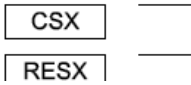


4.1.2 DBI Type B Data Bus

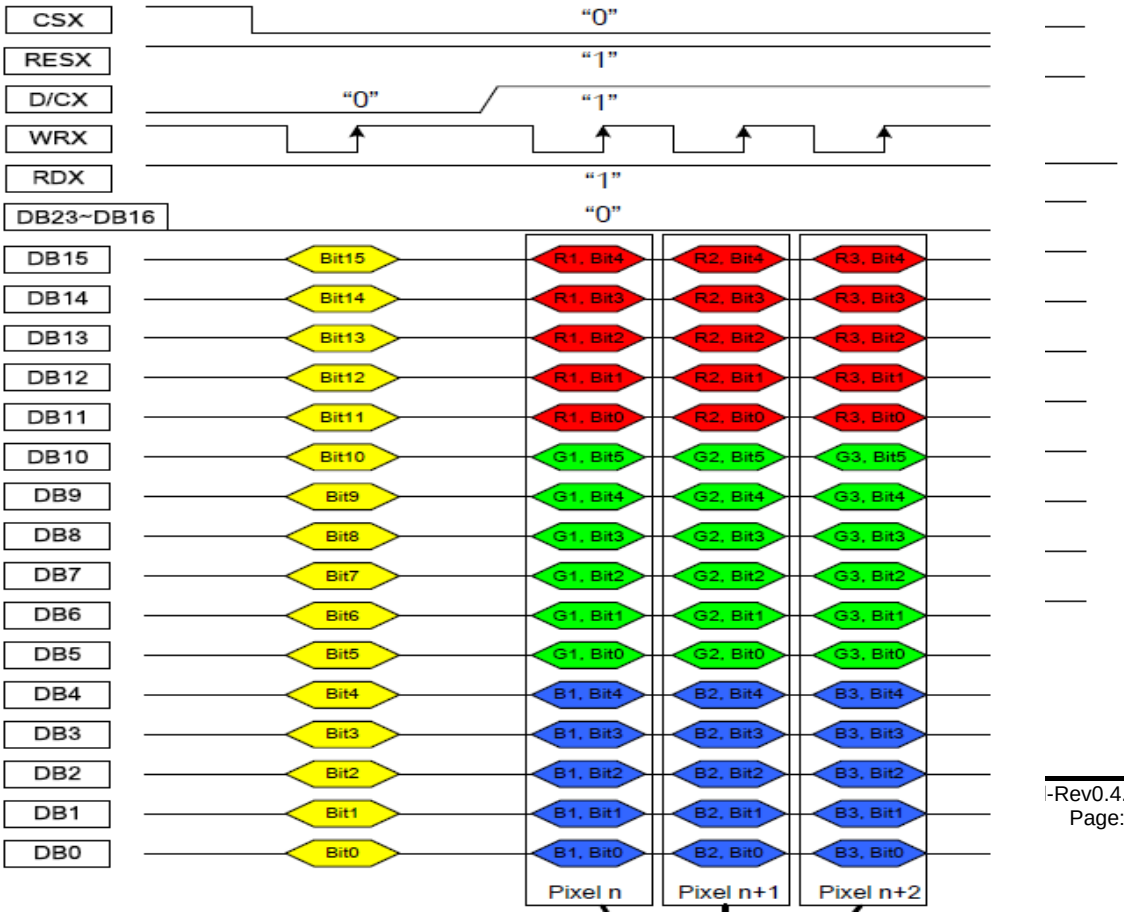
8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



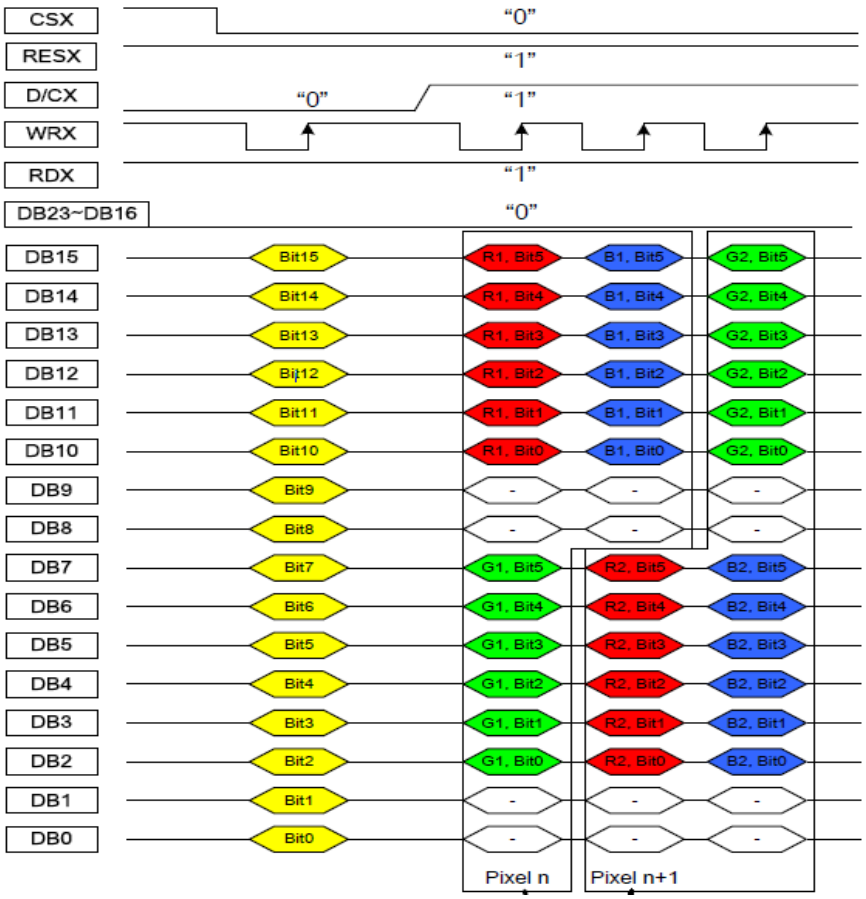
9-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



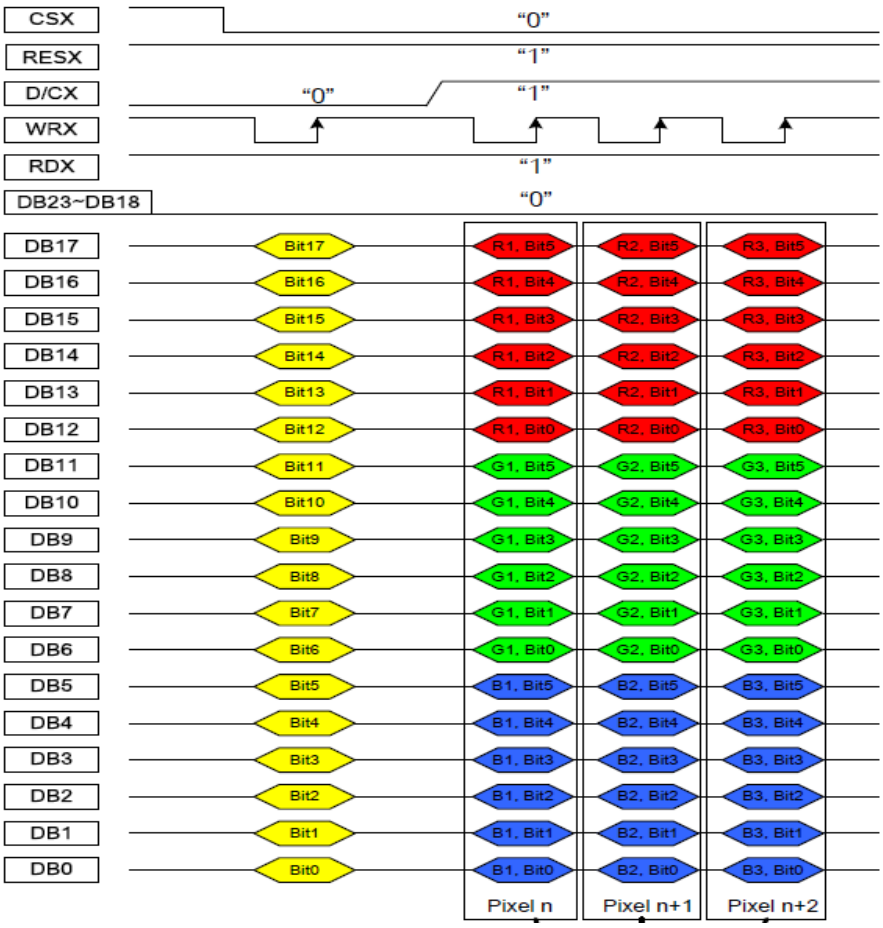
16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color



16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

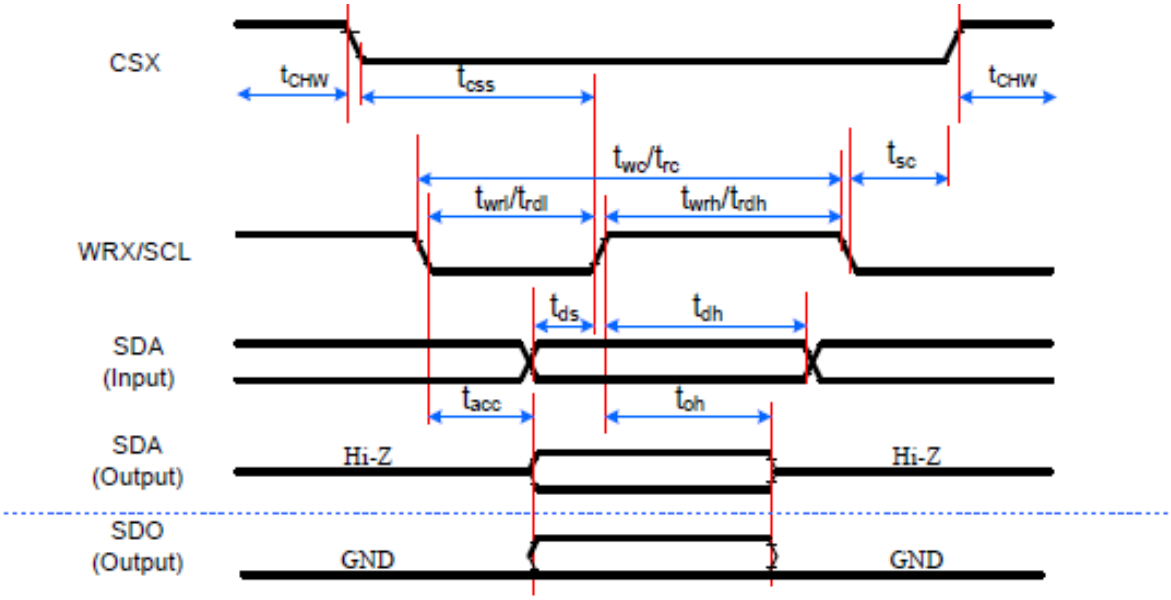


18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



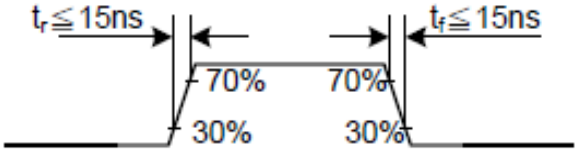
Please refer to IC: ILI9488 data sheet for more details.

4.2 3-Line SPI Interface Timing Characteristic



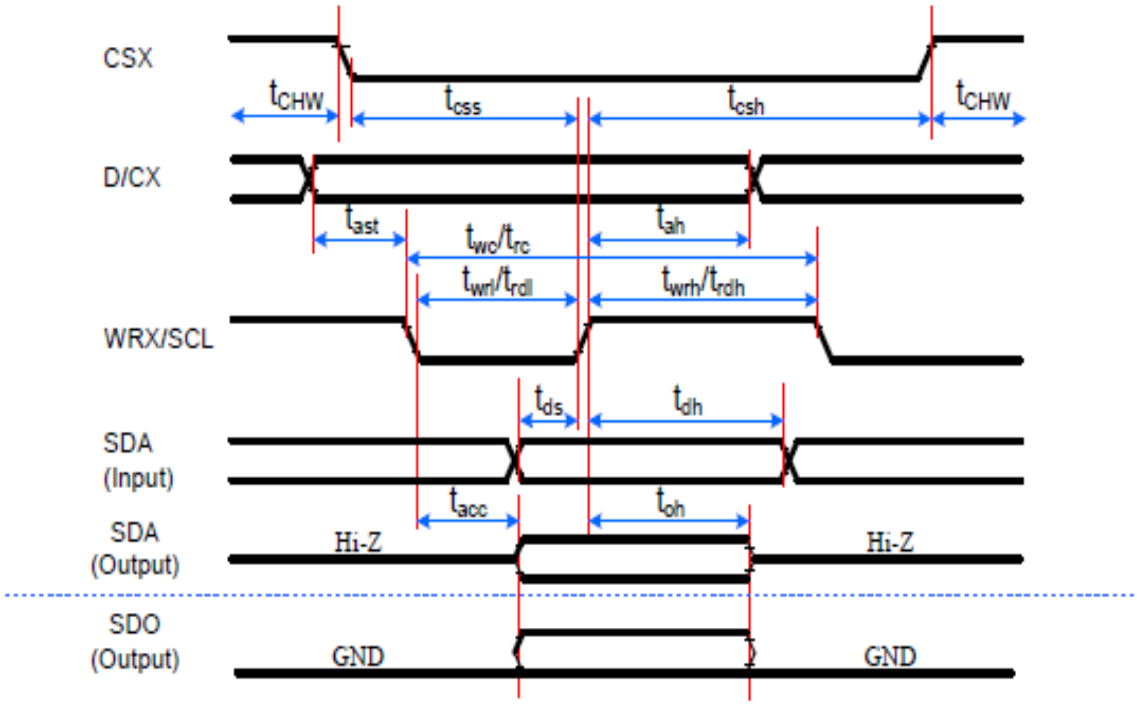
Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchw	CSX H Pulse Width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
	twrl	SCL L Pulse Width (Write)	15	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = -30 to 70 °C, IOVDD,VDD=2.5V to 3.3V,VSS=0V, T = 10+/-0.5ns



Please refer to IC: ILI9488 data sheet for more details.

4.3 4-Line SPI Interface Timing Characteristic



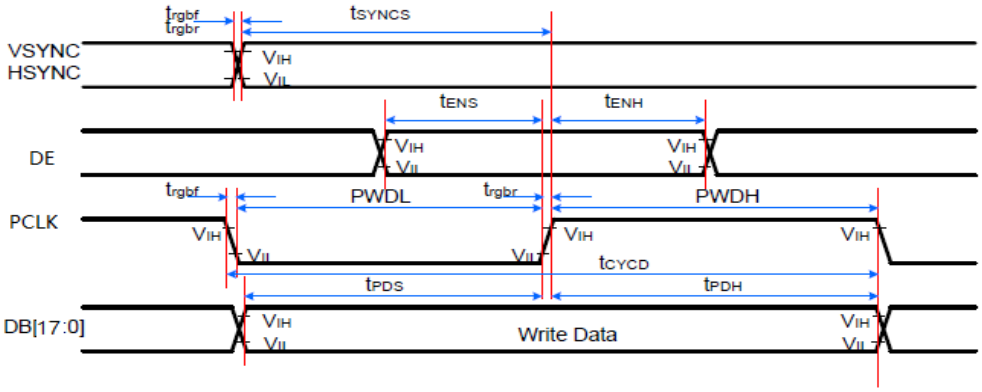
Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS H pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	50	-	ns	
	twrh	SCL H pulse width (Write)	10	-	ns	
	twrl	SCL L pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	-	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note:Ta=-30 to 70℃，IOVDD，VDD=2.5V to 3.3V，VSS=0V，T=10+/-0.5ns.

Please refer to IC: ILI9488 data sheet for more details.

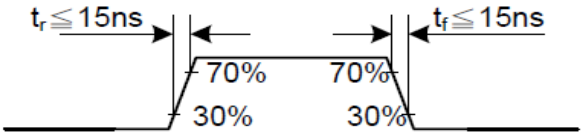
4.4 DPI Interface

4.4.1 DPI Interface Characteristic



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	16-/18-/24-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
DB[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
PCLK	PWDH	DOTCLK high-level period	20	-	ns	
	PWDL	DOTCLK low-level period	20	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, IOVCC , VDD=2.5V to 3.3V, VSS=0V, T=10+/-0.5ns.



Please refer to IC: ILI9488 data sheet for more details.

18-bit DPI interface connection (DB [17:0] is used): set pixel format DPI [2:0] = 3'h6

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
						R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit DPI interface connection (DB [15:0] is used): set pixel format DPI [2:0] = 3'h5

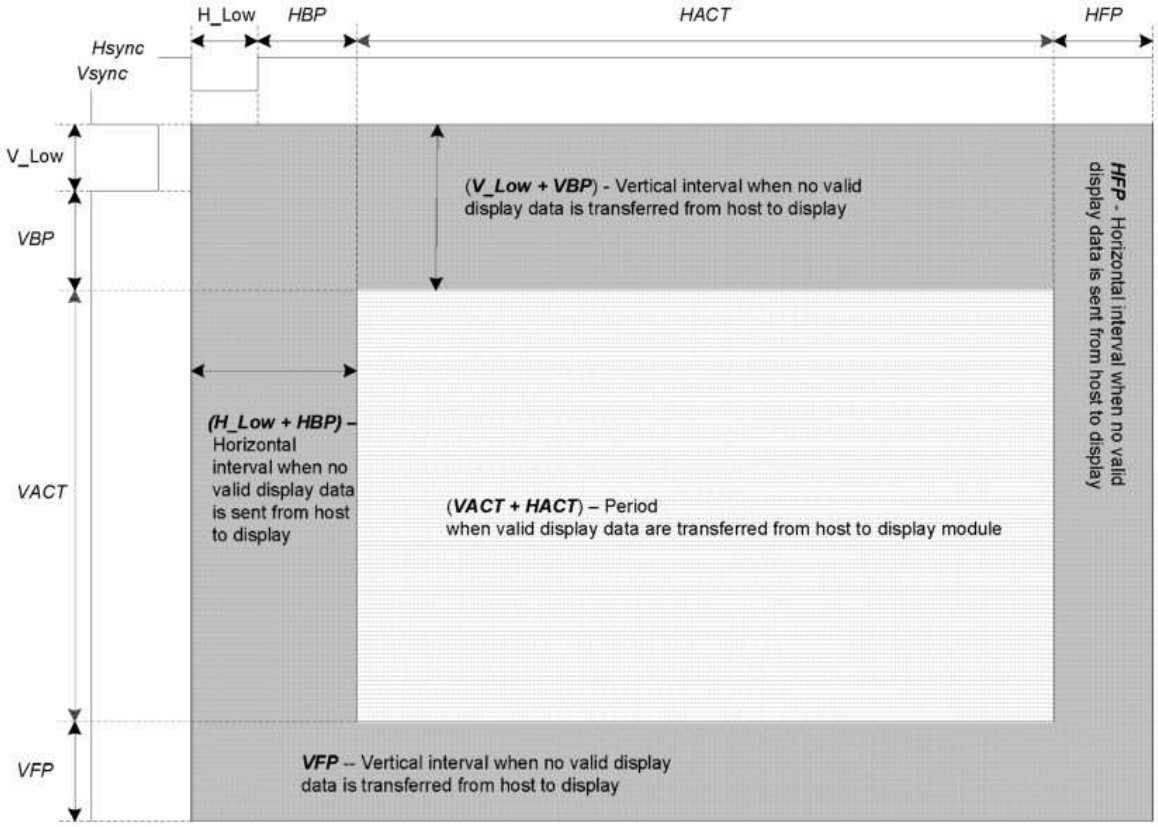
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
								R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

4.4.2 DPI Interface pixel format

The Pixel clock (DCLK) runs all the time without stop. It is used to enter VS, HS, DE and D[17: 0] states when there is a rising edge of the DCLK. The DCLK cannot be used as the internal clock for other functions of the display module.
Vertical synchronization (VS) is used to indicate when a new frame of the display is received. This is low enable and its state is read to the display module by a rising edge of the DCLK signal.
Horizontal synchronization (HS) IS used to indicate when a new line of the frame is received. This is low enable and its state is read to the display module by a rising edge of the DCLK signal.
Data Enable (DE) is used to indicate when the RGB information that should be transferred in the display is received. This is a high enable, and its state is read to the display module by a rising edge of the DCLK signal.
D[17:0] is used to indicate what is the information of the image that is transferred on the display (when DE = 0 (low) and there is a rising edge of DCLK). D[17:0] can be 0(low) or 1(high). These lines are read by a rising edge of the DCLK signal. In RGB interface modes, the input display data is written to GRAM first then outputs the corresponding source voltage according to the gray data from GRAM.

Note：Please refer to IC: ILI9488 data sheet for more details.

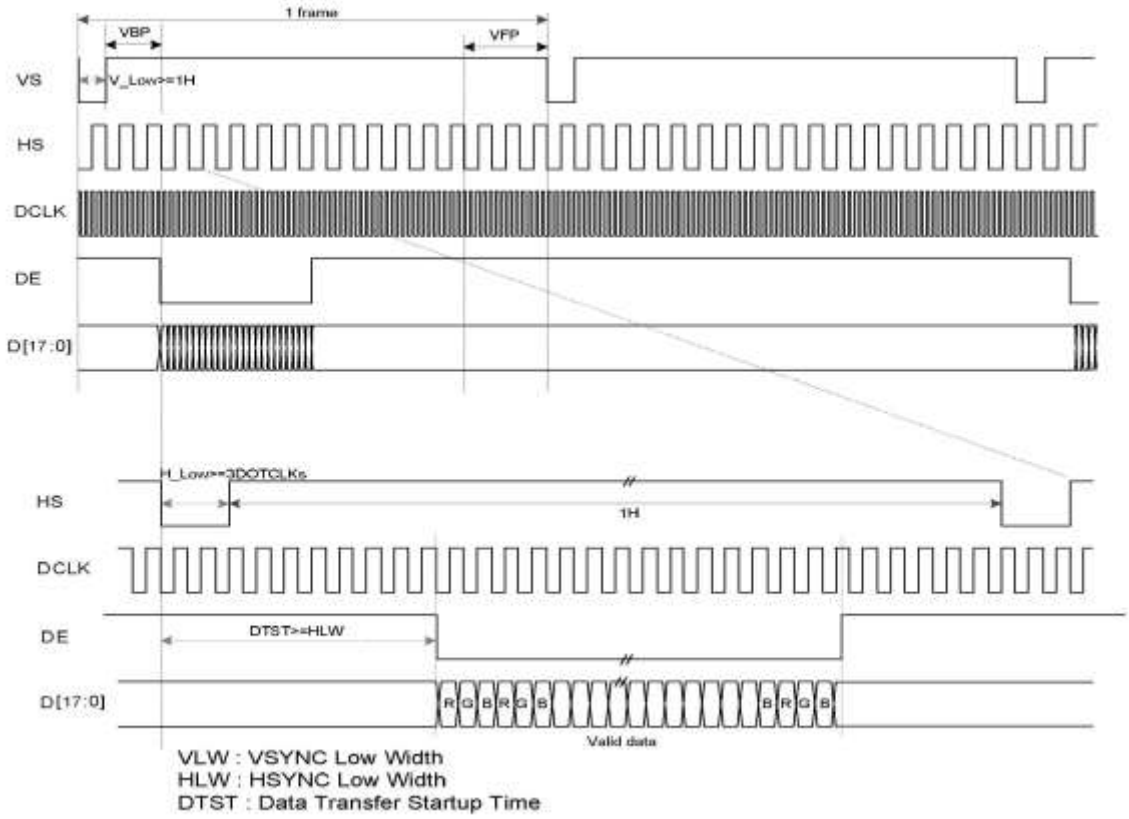
4.4.3 DPI(RGB) Interface timing



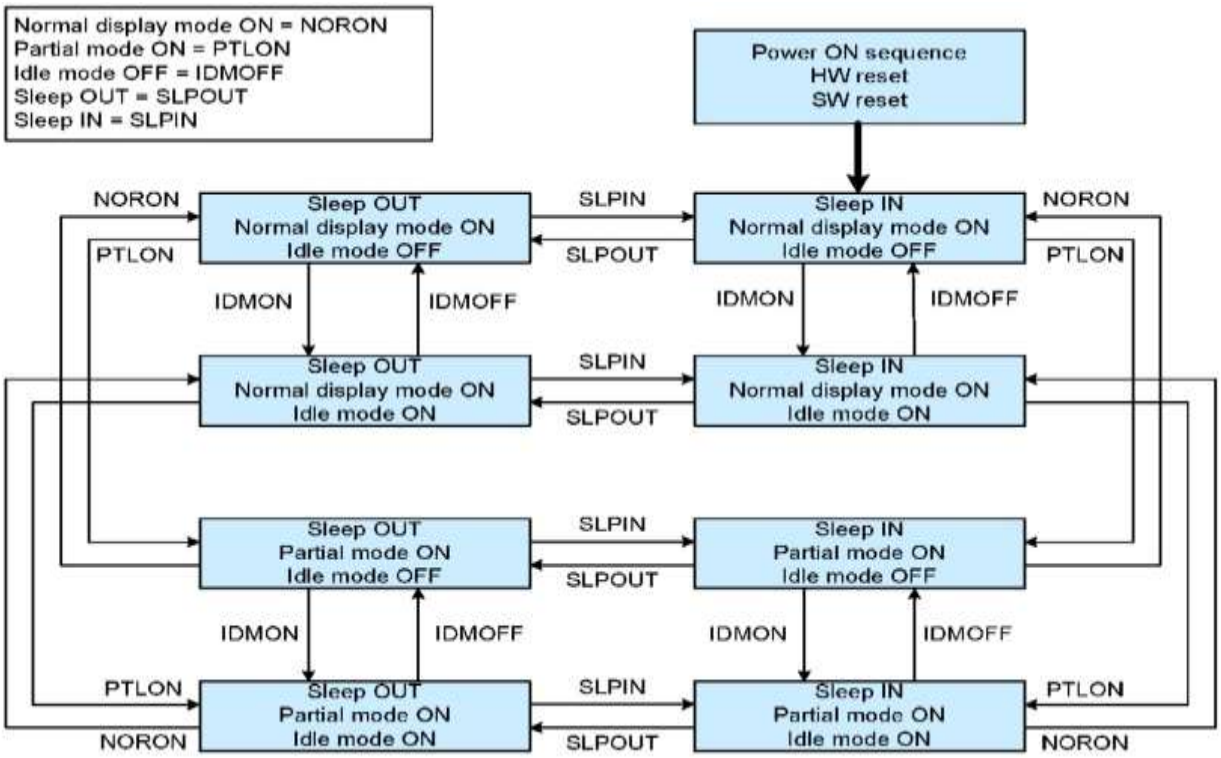
Parameters	Symbols	Min.	Typ.	Max.	Units
Horizontal Synchronization	H_Low	3	-	H_Low+HBP <192	DCLK
Horizontal Back Porch	HBP	3	-		DCLK
Horizontal Front Porch	HFP	3	-	255	DCLK
Horizontal Address	HACT	-	320	-	DCLK
Horizontal Frequency		-	-	33	KHz
Vertical Synchronization	V_Low	1	-	V_Low+VBP+VFP < 32	Line
Vertical Back Porch	VBP	2	-		Line
Vertical Front Porch	VFP	2	-		Line
Vertical Address	VACT	-	480	-	Line
Vertical Frequency		60	-	70	Hz
DCLK cycle		100	-	50	ns
DCLK Frequency		10	-	20	MHz

Example : DCLK = 20Mhz, TE=70Hz, V_Low+VBP=2, VFP=2, H_Low+HBP=100, HFP=170.

Note: VBP[4:0]/HBP[7:0] (Blanking Porch Control, RB5h) define as follows:



4.5 Power ON/OFF Sequence



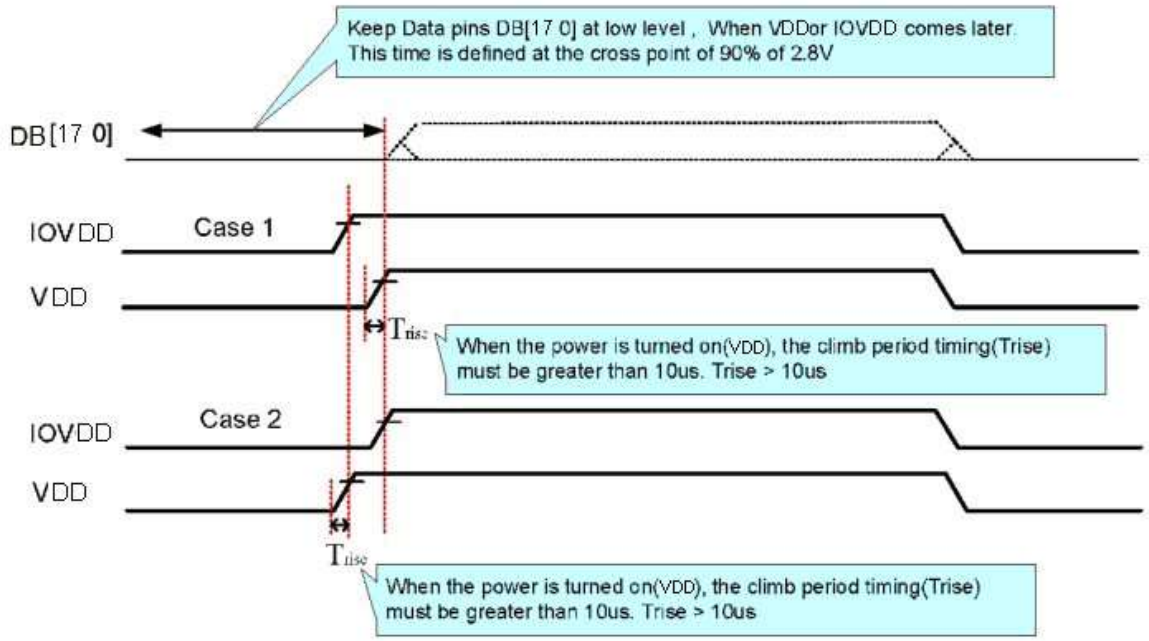
Notes:

1. There are not any abnormal visual effects when one power mode changes to another power mode.
2. There is not any limitation, which is not specified by users, when one power mode changes to another power mode.

IOVDD and VDD can be applied or powered down in any order. During the Power Off sequence ,if the LCD is in the Sleep In mode, VDD and IOVDD must be powered down with a minimum of 120 msec.If the LCD is in the Sleep In mode, VDD and IOVDD can be powered down with a minimum of 0msec after the /RST has been released. /CS can be applied at any time or can be permanently grounded. /RST has priority over /CS.

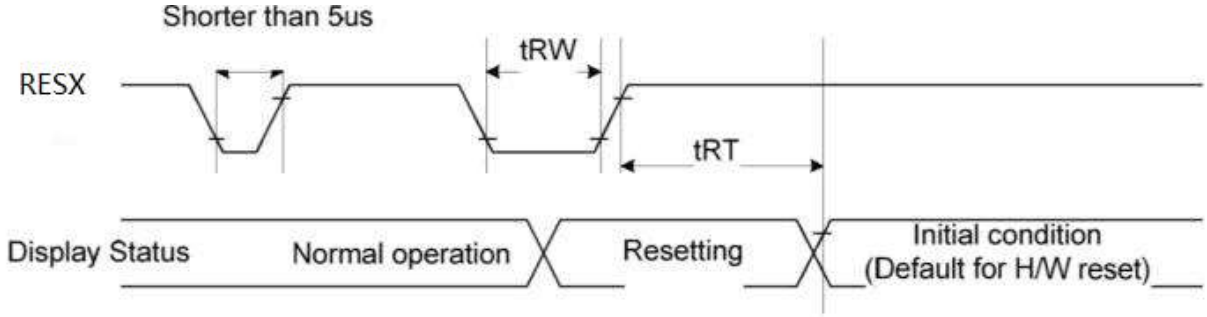
Notes:

1. There will be no damage to the ILI9488 if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequence.
3. There will be no abnormal visible effects on the display between the end of the Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the /RST line is not steadily held by the host during the Power On Sequence as defined in Sections 11.1 and 11.2 (ILI9488 datasheet), then it will be necessary to apply the Hardware /RST after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.
5. When the power is turned on, the climb period timing (Trise) must be greater than 10us.
6. Keep data pins D[17:0] at low level, or IOVDD comes later



Note：Please refer to IC: ILI9488 data sheet for more details.

4.6 Reset timing



Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset LOW pulse width	t_{RW}	1.0	-	-	us
Reset time	T_{RT}	-	-	120	ms

Please refer to IC: ILI9488 data sheet for more details.

5 . Optical Characteristics

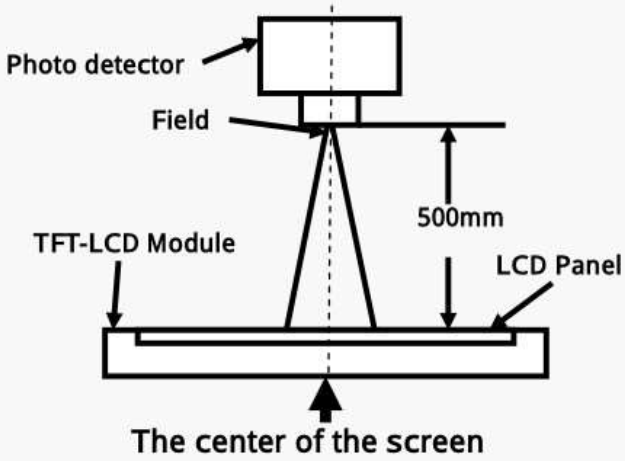
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	60	70		Degree	Note2,3
		θB		50	60			
		θL		60	70			
		θR		60	70			
Contrast Ratio		CR	θ=0°	400	500			Note 3
Response Time		T_{ON}	25℃		25	35	ms	Note 4
		T_{OFF}						
Chromaticity	White	x	Backlight is on		0.286			Note 1,5
		y			0.304			
	Red	x			0.608			Note 1,5
		y			0.336			
	Green	x			0.341			Note 1,5
		y			0.604			
	Blue	x			0.146			Note 1,5
		y			0.073			
Uniformity		U			80		%	Note 6
NTSC					60		%	Note 5
Luminance		L		200			cd/m^2	Note 7

Test Conditions:

1. I_{BLA} = 120 mA, and the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

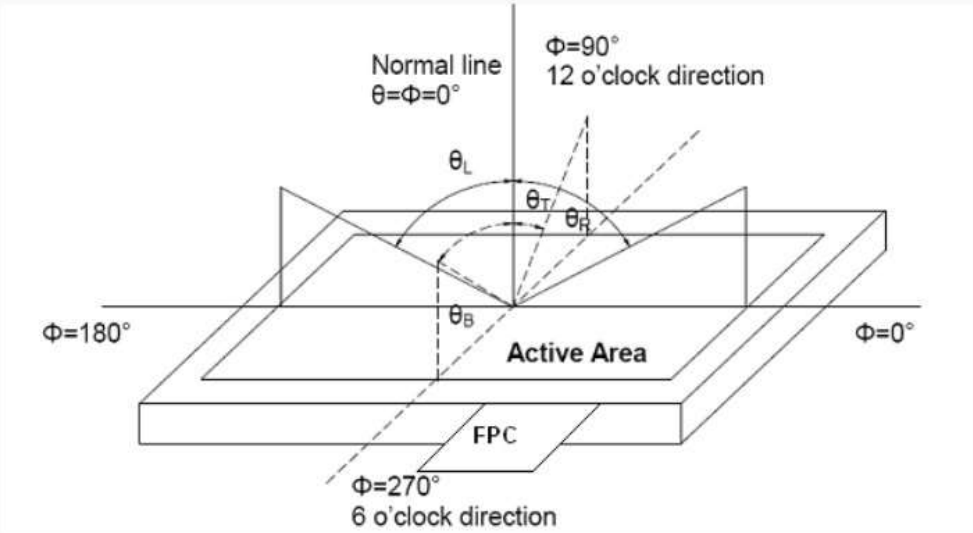
The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

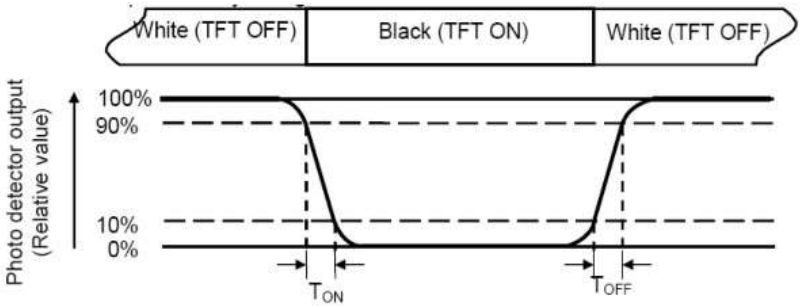
"White state ": The state is that the LCD should drive by Vwhite.

"Black state": The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

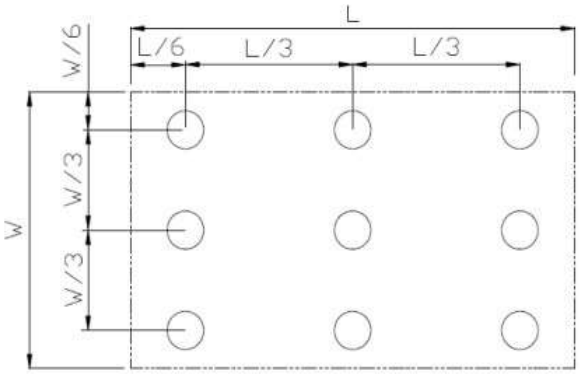
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

6. LCD Module Design and Handling Precautions

- Please ensure V0, VCOM is adjustable, to enable LCD module get the best contrast ratio under different temperatures, view angles and positions.
- Normally display quality should be judged under the best contrast ratio within viewable area. Unexpected display pattern may come out under abnormal contrast ratio.
- Never operate the LCD module exceed the absolute maximum ratings.
- Never apply signal to the LCD module without power supply.
- Keep signal line as short as possible to reduce external noise interference.
- IC chip (e.g. TAB or COG) is sensitive to light. Strong light might cause malfunction. Light sealing structure casing is recommended.
- Make sure there is enough space (with cushion) between case and LCD panel, to prevent external force passed on to the panel; otherwise that may cause damage to the LCD and degrade its display result.
- Avoid showing a display pattern on screen for a long time (continuous ON segment).
- LCD module reliability may be reduced by temperature shock.
- When storing and operating LCD module, avoids exposure to direct sunlight, high humidity, high or low temperature. They may damage or degrade the LCD module.
- Never leave LCD module in extreme condition (max./min storage/operate temperature) for more than 48hr.
- Recommend LCD module storage conditions is 0 C~40 C <80%RH.
- LCD module should be stored in the room without acid, alkali and harmful gas.
- Avoid dropping & violent shocking during transportation, and no excessive pressure press, moisture and sunlight.
- LCD module can be easily damaged by static electricity. Please maintain an optimum anti-static working environment to protect the LCD module. (eg. ground the soldering irons properly)
- Be sure to ground the body when handling LCD module.
- Only hold LCD module by its sides. Never hold LCD module by applying force on the heat seal or TAB.
- When soldering, control the temperature and duration avoid damaging the backlight guide or diffuser which might degrade the display result such as uneven display.
- Never let LCD module contact with corrosive liquids, which might cause damage to the backlight guide or the electric circuit of LCD module.
- Only clean LCD with a soft dry cloth, Isopropyl Alcohol or Ethyl Alcohol. Other solvents (e.g. water) may damage the LCD.
- Never add force to components of LCD module. It may cause invisible damage or degrade the module's reliability.
- When mounting LCD module, please make sure it is free from twisting, warping and bending.
- Do not add excessive force on surface of LCD, which may cause the display color change abnormally.
- LCD panel is made with glass. Any mechanical shock (e.g. dropping from high place) will damage the LCD module.

6. 液晶显示模块设计和使用须知

- 请注意 V0, VCOM 的设定，以确保液晶显示模块在不同的使用温度下以及在不同的视角和位置观察模块显示，均能达到最佳对比度，请务必将应用电路上设置为对比度可调。
- 请注意液晶显示模块的显示品质判定是指在正常对比度下以及视窗(V.A)范围内进行的，非正常对比度下液晶可能会出现非预期的显示不良，应注意区分。
- 请勿在最大额定值以外使用液晶显示模块。
- 请勿在没有接通电源的条件下，给液晶显示模块输送信号。
- 请尽可能缩短信号线的连接，以避免对液晶显示模块的信号干扰。
- 集成电路因 IC 芯片(如 TAB 或 COG)对紫外线极为敏感，强光环境下可能会引起液晶显示模块功能失效，故应采用不透光的外壳。
- 请在液晶显示模块与外壳之间保留足够的空间(可使用衬垫)，以缓冲外力对液晶显示模块的损坏或因受力不均而产生的显示不匀等异常现象。
- 避免液晶显示屏在某一画面下长时间点亮，否则有出现残影的风险；请通过软件每隔一段时间改变一次画面。
- 液晶显示模块的可靠性可能因温度冲击而降低。
- 请勿在阳光直射、高湿、高温或低温下储存和使用液晶显示模块，这将造成液晶显示模块的损坏或失效。
- 请勿在极限环境(最大/最小存储/工作温度)下使用或放置液晶显示模块超过 48 小时以上。
- 液晶显示模块建议存储条件为：0 C~40 C <80%RH。
- 请勿让液晶显示模块存储于带有 酸性，碱性，有害气体环境之中。
- 在运输过程中，请勿让液晶显示模块跌落与猛烈震动，同时避免 异常挤压，高湿度，与阳光照射.
- 液晶显示模块极易受静电损坏，请务必保证液晶显示模块在防静电的工作环境中使用或保存。(如：烙铁正确接地,等)
- 拿取液晶显示模块时需注意操作人员的接地情况。
- 请手持液晶显示模块的边沿取放模块，防止热压纸或 TAB 部位受力。
- 焊接液晶模块时，请注意控制烙铁的温度、焊接时间，以免烫坏导光板或偏光片，导致显示不匀等不良现象发生。
- 请勿使用洗板水等腐蚀性液体接触液晶模块，以免腐蚀导光板或模块电路。
- 仅可使用柔软的干布，异丙醇或乙醇清洁液晶屏表面，其他任何溶剂(如:水)都有可能损坏液晶模块。
- 请勿挤压液晶显示模块上的元器件，以避免产生潜在的损坏或失效而影响产品可靠性。
- 装配液晶显示模块时，请务必注意避免液晶显示

模块的扭曲或变形。

- 请勿挤压液晶显示屏表面，这将导致显示颜色的异常。
- 液晶屏由玻璃制作而成，任何机械碰撞(如从高处跌落)均有可能损坏液晶显示模块。

- Protective film is attached on LCD screen. Be careful when peeling off this protective film, since static electricity may be generated.
- Polarizer on LCD gets scratched easily. If possible, do not remove LCD protective film until the last step of installation.
- When peeling off protective film from LCD, static charge may cause abnormal display pattern. The symptom is normal, and it will turn back to normal in a short while.
- LCD panel has sharp edges, please handle with care.
- Never attempt to disassemble or rework LCD module.
- If display panel is damaged and liquid crystal substance leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes promptly wash it off using soap and water.

- 液晶屏表面带有保护膜，揭除保护膜时需要注意可能产生的静电。
- 因液晶显示屏表面的偏光片极易划伤，安装完成之前请尽量不要揭下保护膜。
- 请缓慢揭除保护膜，在此过程中液晶显示屏上可能会产生静电线，此为正常情况，可在短时间内消失。
- 请注意避免被液晶显示屏的边缘割伤。
- 请不要试图拆卸或改造液晶显示模块。
- 当液晶显示屏出现破裂，内部液晶液体可能流出；相关液体不可吞吃，绝对不可接触嘴巴，如接触到皮肤或衣服，请使用肥皂与清水彻底清洗.

7. RTP Mounting Instructions

- It should bezel touching the RTP Active Area (A.A.) to prevent abnormal touch.It should left gab D=0.2~0.3mm in between. (Figure 4)
- Outer bezel design should take care about the area outside the A.A. Those areas contain circuit wires which is having different thickness. Touching those areas could de-form the ITO film. As a result bezel the ITO film be damaged and shorten its lifetime.
  It is suggested to protect those areas with gasket (between the bezel and RTP).The suggested figures are B≥0.50mm; C≥0.50mm. (Figure 4)
- The bezel side wall should keep space E= 0.2 ~ 0.3mm from the RTP. (Figure 1)

7. 电阻触摸屏安装指导

- 为避免面框直接压在动作区(A.A.)上造成误动作，面框与电阻触摸屏(RTP)之间应留有一定的空隙 D=0.2~0.3mm 之间.(附图 1)
- 设计面框时，要注意用面框保护触摸屏四周的非保证操作区域，因为布线区域在此处形成一台阶，在此区域附近操作时 ITO Film 变形较大，容易导致 ITO 损坏而降低寿命。为保护 RTP 和避免误操作，在 RTP 与面框之间垫缓冲物（Gasket），我们建议设计面框应覆盖动作区的边缘，面框边缘到 V.A.区的距离 B≥0.50mm；垫圈内边缘到 V.A.区的距离 C≥0.50mm. (附图 4)
- 在设计面框与 RTP 组装时，应考虑到面框内侧与 RTP 外侧的间距 E≥0.2mm. (附图 1)

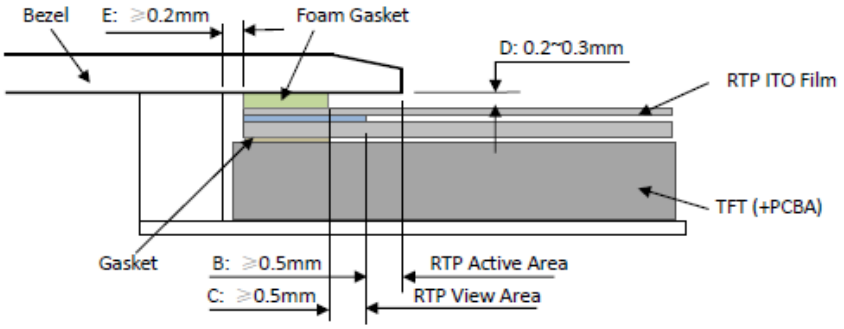


Figure 1

- In general design,
  RTP V.A. should be bigger than the TFT V.A.
  and RTP A.A. should be bigger than the TFT A.A.
  (Figure 2)

- 通常设计时：
  RTP 的可视区 V.A. 应不小于 TFT 的可视区 V.A.
  及 RTP 的动作区 A.A. 应不小于 TFT 的动作区 A.A.
  (附图 2)

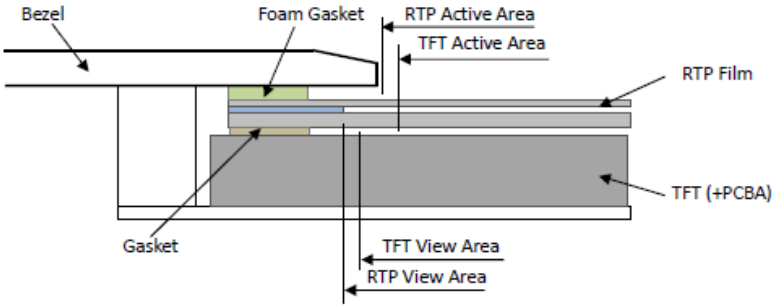
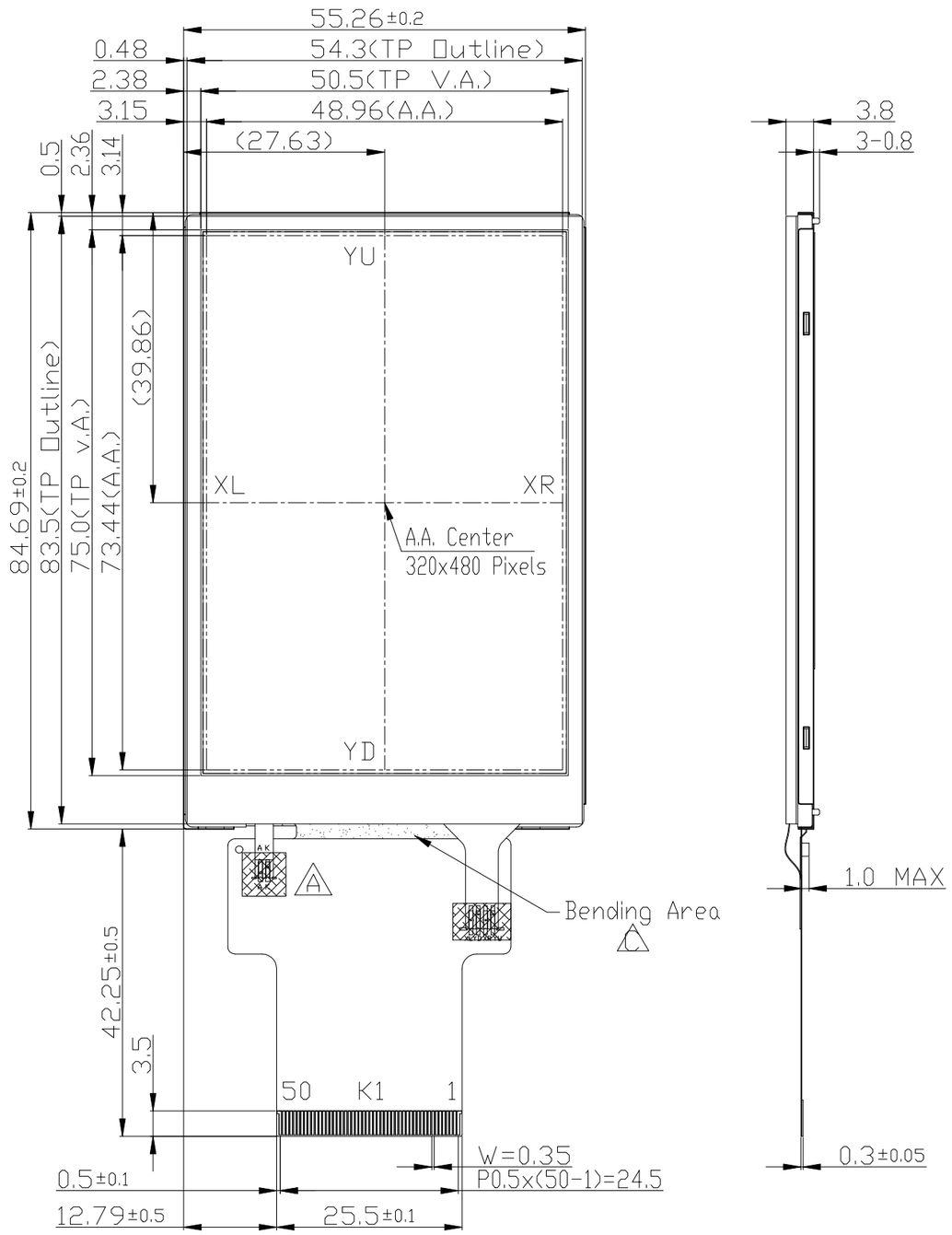


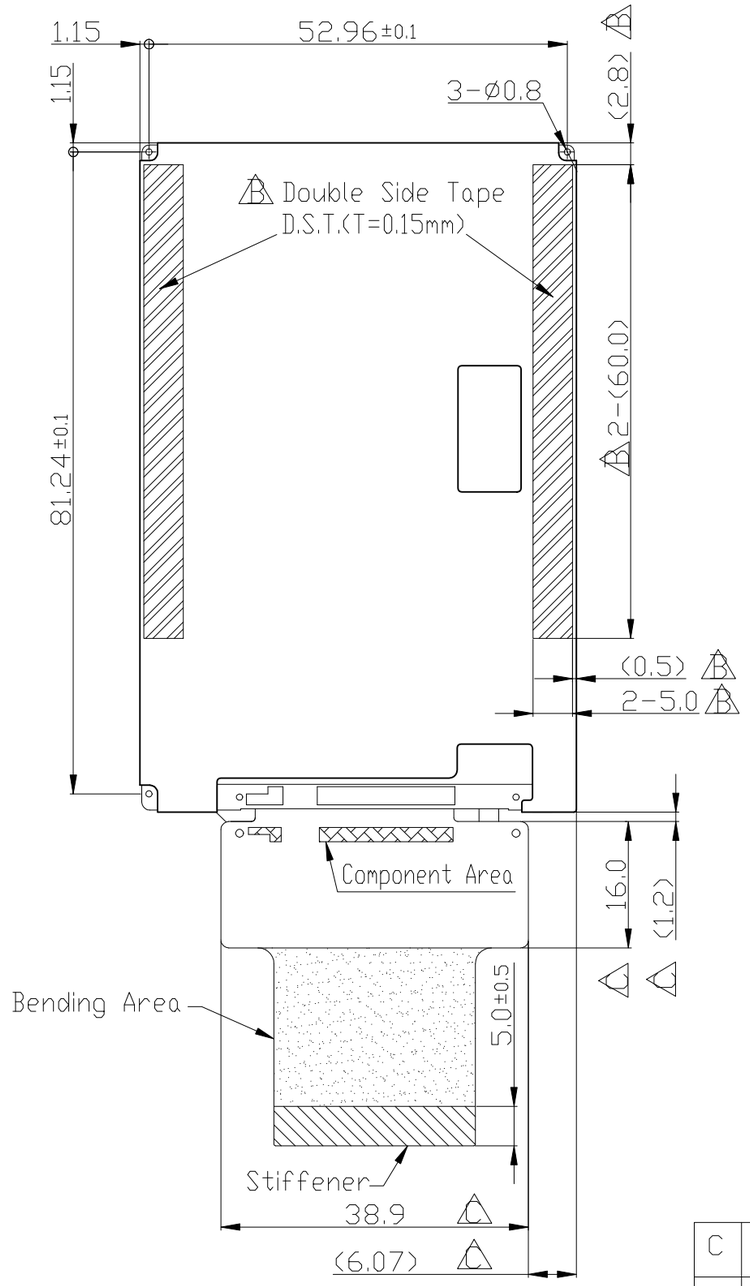
Figure 2

Warranty

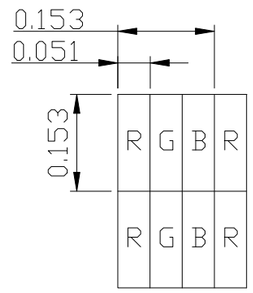
This product has been manufactured to our company's specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

- We cannot accept responsibility for any defect, which may arise form additional manufacturing of the product (including disassembly and reassembly), after product delivery.
- We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
- We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed our company's acceptance inspection procedures.
- When the product is in CCFL models, CCFL service life and brightness will vary according to the performance of the inverter used, leaks, etc. We cannot accept responsibility for product performance, reliability, or defect, which may arise.
- We cannot accept responsibility for intellectual property of a third part, which may arise through the application of our product to our assembly with exception to those issues relating directly to the structure or method of manufacturing of our product.





K1 Terminal		K1 Terminal	
No.	Pin Name	No.	Pin Name
1	VSS	26	DB5/B5,Msb
2	IOVDD	27	DB4/B4
3	IOVDD	28	DB3/B3
4	VDD	29	DB2/B2
5	VDD	30	DB1/B1
6	IM0	31	DB0/B0,Lsb
7	IM1	32	VSS
8	IM2	33	DOUT
9	RESX	34	SDA
10	VSYNC	35	RDX
11	HSYNC	36	WRX_SCL
12	PCLK	37	DCX
13	DE	38	CSX
14	DB17/R5,Msb	39	XR(X+)
15	DB16/R4	40	YD(Y-)
16	DB15/R3	41	XL(X-)
17	DB14/R2	42	YU(Y+)
18	DB13/R1	43	LEDA
19	DB12/R0,Lsb	44	LEDK
20	DB11/G5,Msb	45	LEDK
21	DB10/G4	46	LEDK
22	DB9/G3	47	LEDK
23	DB8/G2	48	LEDK
24	DB7/G1	49	LEDK
25	DB6/G0,Lsb	50	VSS



Pixel Details
Scale=100/1

Note:
*1. LCD Display Type : TFT,Transmissive
*2. Pixel Arrangment : RGB-STRIPE
*3. Color Depth : 262k Color
*4. Operating Voltage(VDD , IOVDD) : 3.0V
*5. Backlight : White LEDs
*6. Backlight Supply : 6x20mA (VF=3.2V, TYP)
*7. Touch Panel Type : Resistive Touch Panel
*8. Foam Gasket must be assemble outside TP VA by 0.5mm
*9. Recommended Connector K1: FH19SC-50S-0.5SH(HIROS) Or Equivalent
*10. Operating Temperature : -20°C~70°C
*11. Storage Temperature : -30°C~80°C

Rev	Note	Date
C	Typing Correction	Li Yongzheng 2023-08-23
B	Add Double Side Tape	Tao Qingwen 2022-09-14
A	Revise BL FPC	Qiu Shaoping 2020-08-11

Dwg Title	LMT035DNJFWD-NNA-1 Outline Dwg		
Dwg No.	MK-006920c-1-1		Date 2020-06-17
Scale 5/4	Tol. ±0.3	Unit mm	Paper Size A3
Approved	Checked	Drawn Qiu Shaoping	

TOPWAY