深圳市拓普微科技开发有限公司
SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LMT024FNHFWA-1

LCD Module User Manual

Prepared by:	Checked by:	Approved by:
Likeke		
Date: 2022-01-09	Date:	Date:

Rev.	Descriptions	Release Date
0.1	Preliminary release	2020-10-12
0.2	Update LED Backlight Circuit Characteristics	2022-01-09

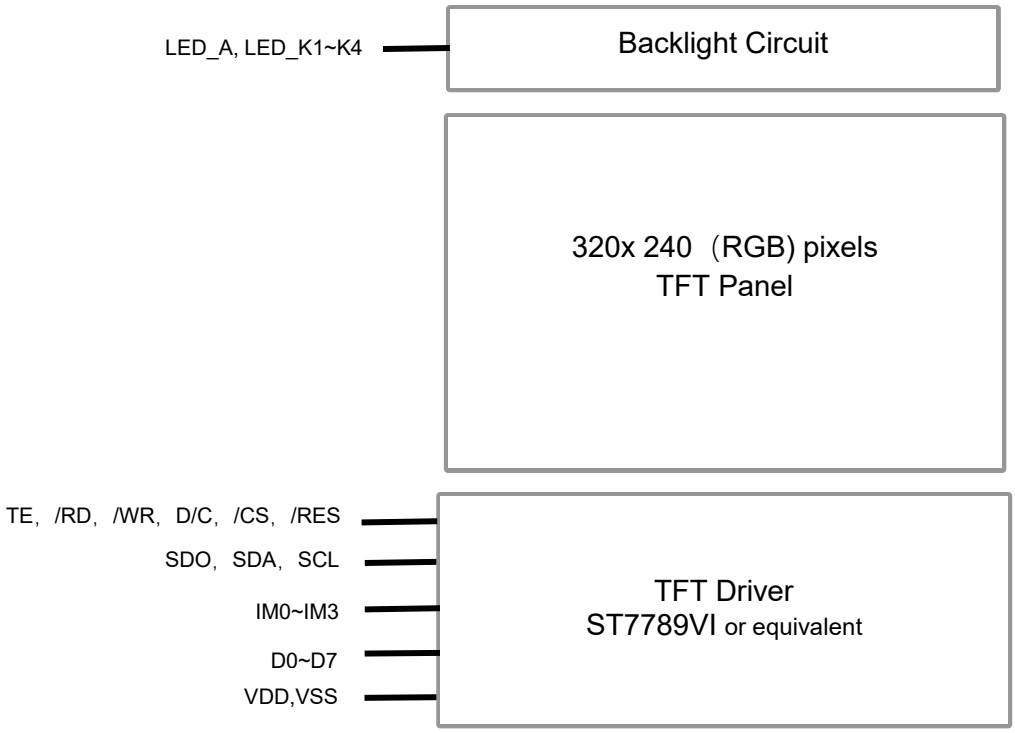
Table of Content

1. Basic Specifications

Screen Size(Diagonal) :	2.4”
Color Depth:	65K/262k color
Number of dots :	320 x240(RGB)
Active Area :	48.96x 36.72 mm
Dot Pitch :	0.153 x 0.153 mm
Display Technology :	a-Si TFT active matrix
Display Mode :	Transmissive with Normally black
Pixel Configuration :	RGB Vertical Stripe
Viewing Direction :	All viewing angle
Backlight Type:	LEDs
Outline Dimension :	62x 43.52x 4.9mm(see dwg for details)
Operating Temperature :	-20 ~ +70°C (No Condensation)
Storage Temperature :	-30 ~ +80°C (No Condensation)

Note:
*1. For saturated color display content (eg. pure-red, pure-green, pure-blue or pure-colors-combinations).
*2. For “color scales” display content.
*3. Color tone may slightly change by temperature and driving condition.

1.1 Block Diagram



1.2 Terminal Functions

Pin No.	PIN Name	I/O	Descriptions	If not use
1	VSS	P	Ground	/
2	NC	P	Not connect. Using for internal OTP power supply.	Open
3	NC(SDO)	I	SPI interface II output signal	Open
4	TE	O	Tearing effect signal is used to synchronize MCU to memory writing	Open
5	D7	I/O	MCU parallel interface data bus	VDD/VSS
6	D6	I/O		
7	D5	I/O		
8	D4	I/O		
9	D3	I/O		
10	D2	I/O		
11	D1	I/O		
12	D0	I/O		
13	VSS(SDA)	I	When IM3:Low,SPI interface input/output pin. When IM3:High,SPI interface input pin. SPI interface input/output pin;	VDD/VSS
14	/RD	I	MCU parallel interface read enable signal	VDD/VSS
15	/WR(D/C)	I	1.MCU parallel interface write enable signal 2.Display data /command selection in 4-line SPI interface	VDD/VSS
16	D/C（SCL）	I	1.MCU parallel interface display data/command selection signal. 2.SPI interface clock signal	VDD/VSS
17	/CS	I	chip select pin,low enable	/
18	/RES	I	chip reset signal ,low active.	/
19	IM0	P	MCU interface mode select pin0	/
20	IM1	P	MCU interface mode select pin1	/
21	IM2	P	MCU interface mode select pin2	/
22	IM3	P	MCU interface mode select pin3	/
23	VDD	P	Power supply for IC I/O system analog,digital and booster circuit	/
24	VSS	P	Ground	/
25	LED_A	P	BL anode signal	/
26	LED_K1	P	BL cathode signal	/
27	LED_K2	P		
28	LED_K3	P		
29	LED_K4	P		
30	VSS	P	Ground	/

Note1: Please add the FPC connector type and matched one if necessary.

Note2:

IM3	IM2	IM1	IM0	Interface	Read Back Data Bus Selection
0	0	0	0	80-8bit parallel I/F	DB[7:0]
0	1	0	1	3-line 9bit serial I/F	SDA: in/out
				2 data lane serial I/F	SDA: in/out, WRX: in
0	1	1	0	4-line 8bit serial I/F	SDA: in/out
1	1	0	1	3-line 9bit serial I/F Ⅱ	SDA: in/ SDO: out
1	1	1	0	4-line 8bit serial I/F Ⅱ	SDA: in/ SDO: out

2. Absolute Maximum Ratings

VSS=0V

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	VDD	-0.3	4.6	V	-
Input Voltage	V_{IN}	-0.3	4.6	V	
Operating Temperature	T_{OP}	-20	+70	°C	Note1
Storage Temperature	T_{ST}	-30	+80	°C	

Note1: Ta means the ambient temperature.
It is necessary to limit the relative humidity to the specified temperature range.
Condensation on the module is not allowed.

3. Electrical Characteristics

3.1 DC Characteristics

VDD=3.3V,VSS=0V, T_{OP}=25°C

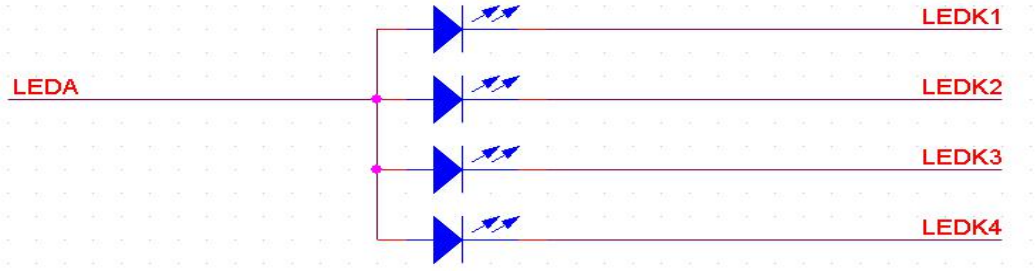
Items	Symbol	MIN.	TYP.	MAX.	Unit	Application Pin
Logic Supply Voltage	IOVDD	3.2	3.3	3.6	V	VDD
Input High Voltage	V_{IH}	0.7 IOVDD	-	0.3 IOVDD	V	SDO,SDA,/RD,/WR, D/C,SCL,/CS,/RES,D0~D7
Input Low Voltage	V_{IL}	-	-	1.0	V	
Output High Voltage	V_{OH}	0.8 IOVDD	-	-	V	D0~D7,TE
Output Low Voltage	V_{OL}	-	-	0.2 IOVDD	V	
Operating Current	I_{VDD}	-	9.3	23.25	mA	

3.2 LED Backlight Circuit Characteristics

T_{OP}=25℃

Items	Symbol	MIN.	TYP.	MAX.	Unit	Note
Forward Voltage	V_F	2.9	3.1	3.4	V	For each LED
Forward Current	If	-	20	-	mA	For each LED
Backlight Power Consumption	W_{BL}	-	248	-	mW	4LEDs
Operating Life Time	T	-	20000	-	Hrs	For each LED

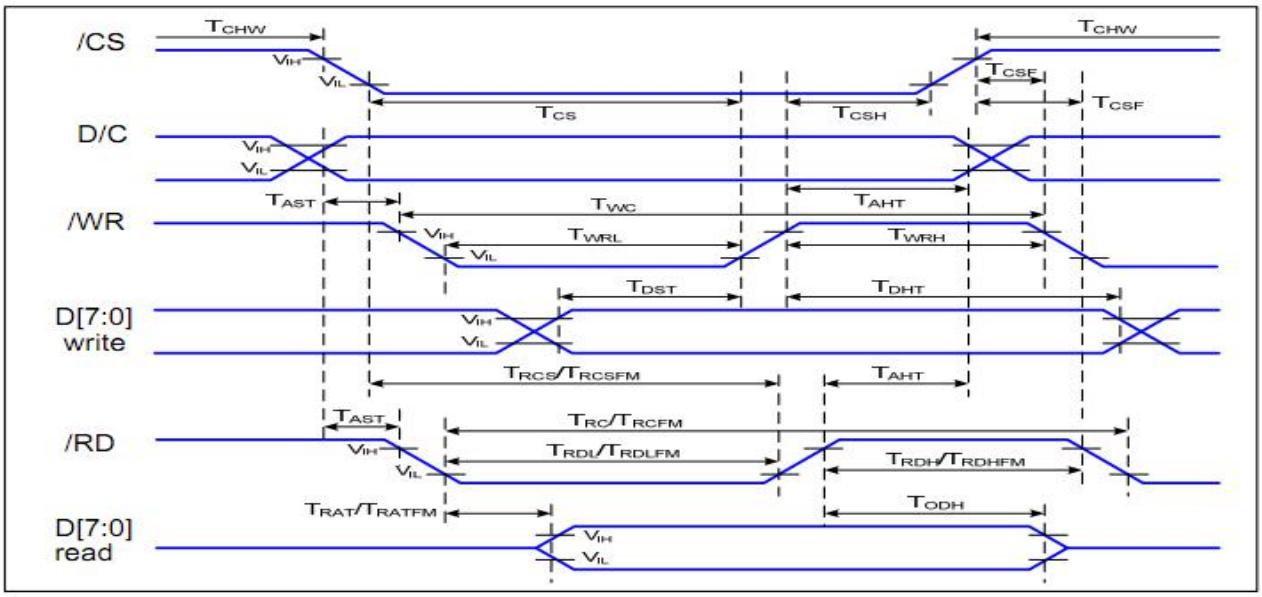
Cautions:
Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.



No. of LEDs = 4pcs

3.3 AC Characteristics

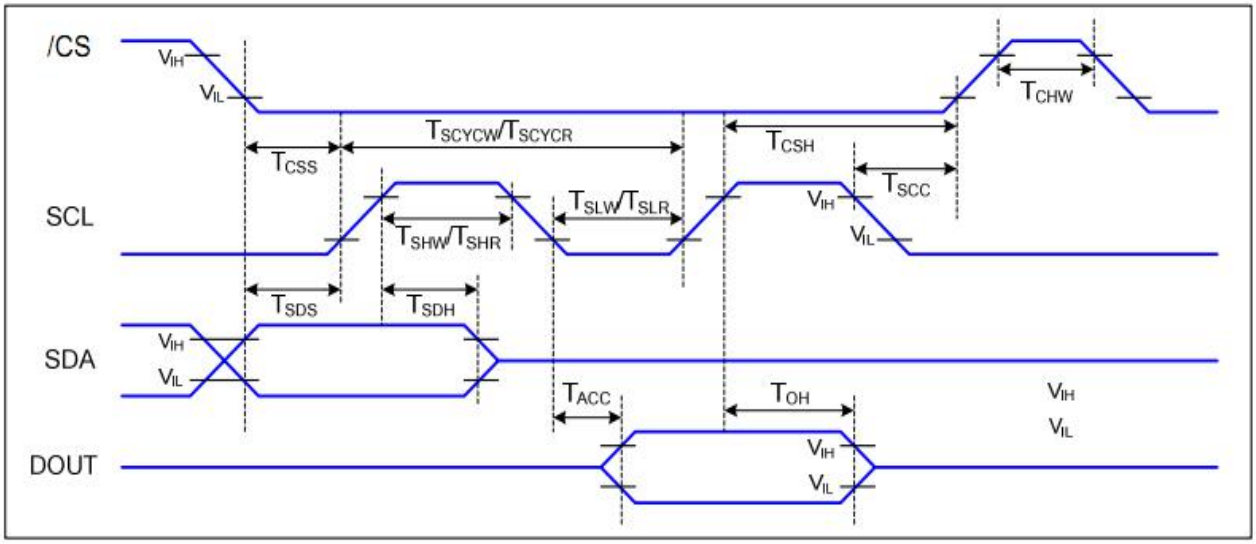
MCU 8bit Timing



VDD=3.3V, VSS=0V, Ta= 25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/C	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
/CS	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
/WR	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
/RD (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[7:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

3 line SPI Timing

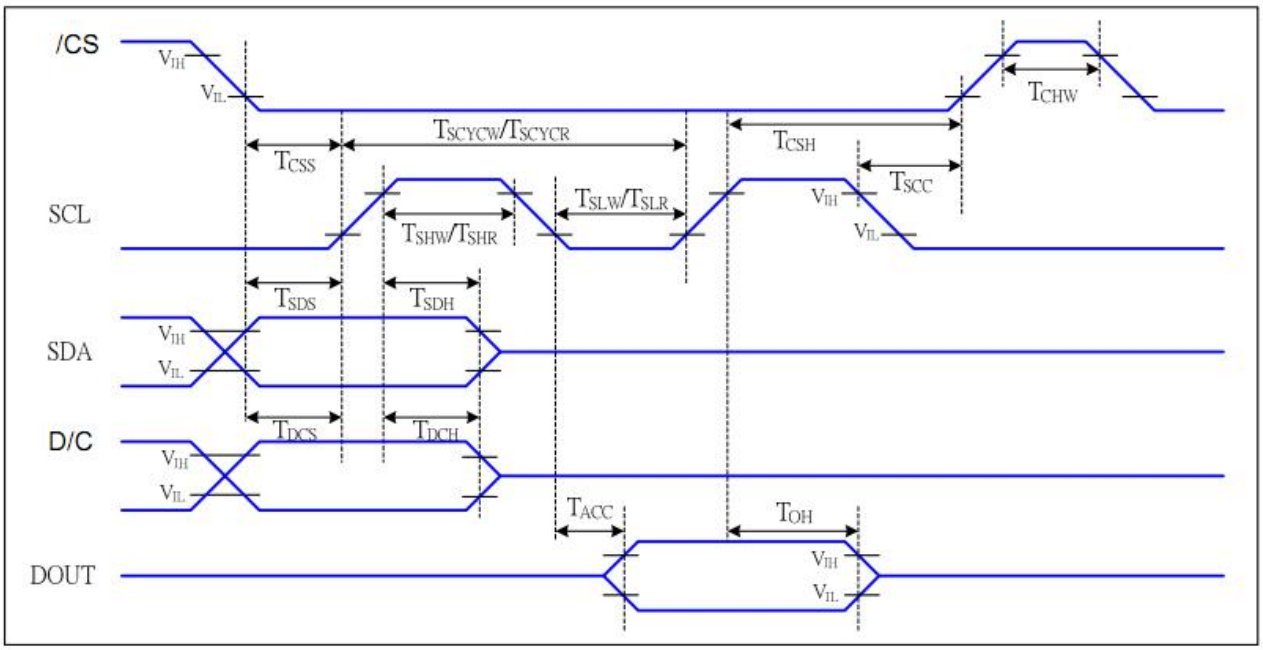


VDD=3.3V, VSS=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
/CS	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	
	T_{SHW}	SCL "H" pulse width (Write)	7		ns	
	T_{SLW}	SCL "L" pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

4 line SPI Timing

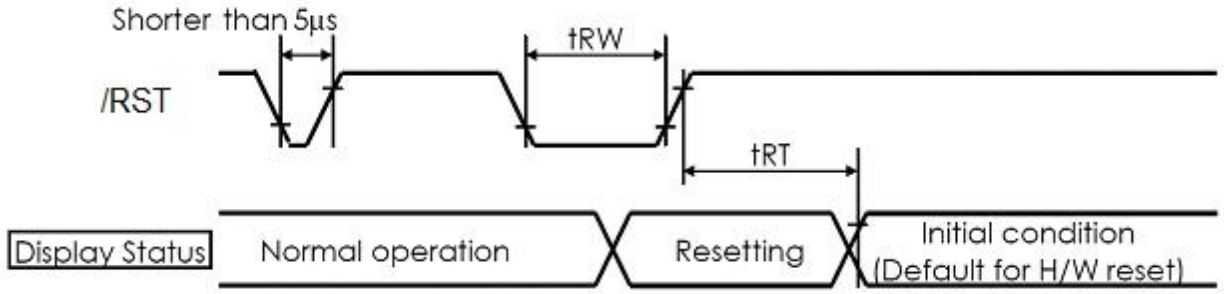


VDD=3.3V, VSS=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
/CS	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	7		ns	
	T_{SLW}	SCL “L” pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
D/C	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Note :
The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

3.4 Rseset Timing



VDD=3.3V,VSS=0V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset LOW pulse width	T_{RW}	10	-	-	us
Reset time	T_{RT}	-	-	120	ms

4. Functions

4.1 Display Commands

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No operation
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read display ID
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read display status
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
	1	1	↑	-	ST15	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
	1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0		-
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read display power
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	0	0		
RDD MADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read display
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	MY	MX	MV	ML	RGB	MH	0	0		-
RDD COLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read display pixel
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0		-
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read display image
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	VSSON	0	INVON	0	0	GC2	GC1	GC0		-
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read display signal
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	↑	-	TEON	TEM	0	0	0	0	0	0		-
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read display self-diagnostic result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	D7	D6	0	0	0	0	0	0		-
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display Inversion off
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display Inversion on
GAMSET	0	↑	1	-	0	0	1	0	0	0	0	1	(26h)	Display Inversion on
	1	↑	1	-	0	0	0	0	GC3	GC2	GC1	GC0		
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start:
	1	↑	1		XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		0≤XS≤X
	1	↑	1		XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address start:
	1	↑	1		XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		S≤XE≤X
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start:
	1	↑	1		YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		0≤YS≤Y
	1	↑	1		YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address start:
	1	↑	1		YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		S≤YE≤Y
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Read data
	1	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial sart/end address set
	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address: (0, 1,2, ..P)
	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0, 1,2, 3, , P)
	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Vertical scrolling definition
	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8		
	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8		
	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
	1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8		
	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0		
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect line on
	1	↑	1	-	-	-	-	-	-	-	-	TEM		
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
	1	↑	1	-	MY	MX	MV	ML	RGB	0	0	0		-
VSCRSADD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Vertical scrolling start address
	1	↑	1	-	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8		
	1	↑	1	-	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0		
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
	1	↑	1	-	0	D6	D5	D4	0	D2	D1	D0		Interface format
RAMWRC	0	↑	1	-	0	0	1	1	1	1	0	0	(3Ch)	Memory write continue
	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRDC	0	↑	1	-	0	0	1	1	1	1	1	0	(3Eh)	Memory read continue
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		
	1	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
TESCAN	0	↑	1	-	0	1	0	0	0	1	0	0	(44h)	Set tear scanline
	1	↑	1	-	N15	N14	N13	N12	N11	N10	N9	N8		
	1	↑	1	-	N7	N6	N5	N4	N3	N2	N1	N0		
RDTESCAN	0	↑	1	-	0	1	0	0	0	1	0	1	(45h)	Get scanline
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	-	-	-	-	-	-	N9	N8		
	1	1	↑	-	N7	N6	N5	N4	N3	N2	N1	N0		
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	(51h)	Write display brightness
	1	↑	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
RDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	(52h)	Read display brightness value
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	(53h)	Write CTRL display
	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0		
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	(54h)	Read CTRL value display
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	0	BCTRL	0	DD	BL	0	0		

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
WRCACE	0	↑	1	-	0	1	0	1	0	1	0	1	(55h)	Write content adaptive brightness control and Color enhancemnet
	1	↑	1	-	CECTRL	0	CE1	CE0	0	0	C1	C0		
RDCABC	0	↑	1	-	0	1	0	1	0	1	1	0	(56h)	Read content adaptive brightness control
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	CECTRL	0	0	0	0	C1	C0		
WRCABCMB	0	↑	1	-	0	1	0	1	1	1	1	0	(5Eh)	Write CABC minimum brightness
	1	↑	1	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDCABCMB	0	↑	1	-	0	1	0	1	1	1	1	1	(5Fh)	Read CABC minimum brightness
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDABCSDR	0	↑	1	-	0	1	1	0	1	0	0	0	(68h)	Read Automatic Brightness Control Self-Diagnostic Result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	D7	D6	0	0	0	0	0	0		-
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

Note: Please refer to Sitronix ST7789VI data sheet for more details.

4.2 Power off the LCD Module

It recommends that enter Sleep Mode before power off the LCD module.

4.3 Refreshing The LCD Module

It recommends that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.

5. Optical Characteristics

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	70	80	-	Degree	Note2,3
		θB		70	80	-		
		θL		70	80	-		
		θR		70	80	-		
Contrast Ratio		CR	θ= 0°	600	800	-		Note 3
Response Time		TON	25℃	-	20	30	ms	Note 4
		TOFF						
Chromaticity	**White**	x	Backlight is on	-	-	-		Note 1,5
		y		-	-	-		
	Red	x		-	-	-		Note 1,5
		y		-	-	-		
	Green	x		-	-	-		Note 1,5
		y		-	-	-		
	Blue	x		-	-	-		Note 1,5
		y		-	-	-		
Uniformity		U		-	80%	-	%	Note 6
NTSC				65%	70%	-	%	Note 5
Luminance		L		250	300	-	cd/㎡	Note 7

Test Conditions:

1.ILEDA= 80mA, and the ambient temperature is 25℃.

2. The test systems refer to Note 1 and Note 2.

6. Precautions for Use of LCD Modules

6.1 Handling Precautions

6.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc

6.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

6.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

6.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

6.1.5 If the display surface is contaMinated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Ketone
- Water
- Aromatic solvents

6.1.6 Do not attempt to disassemble the LCD Module.

6.1.7 If the logic circuit power is off, do not apply the input signals.

6.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

6.1.8.1 Be sure to ground the body when handling the LCD Modules.

6.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

6.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

6.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

6.2 Storage precautions

6.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

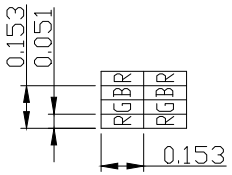
6.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃~40℃Relatively humidity:≤80%

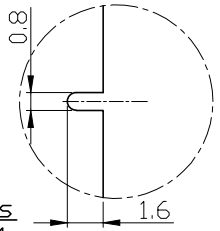
6.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

6.3 Transportation Precautions

6.3.1 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.



#A Details
Scale=50/1



#D Details
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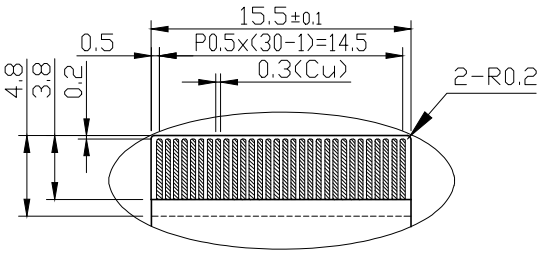
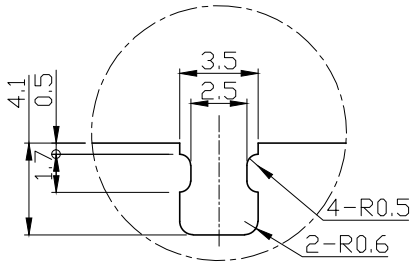
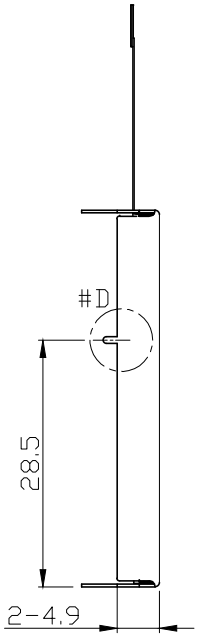
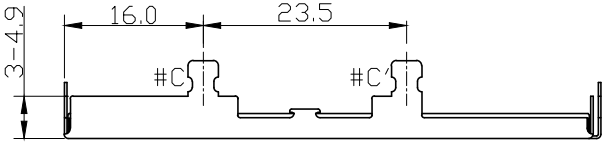


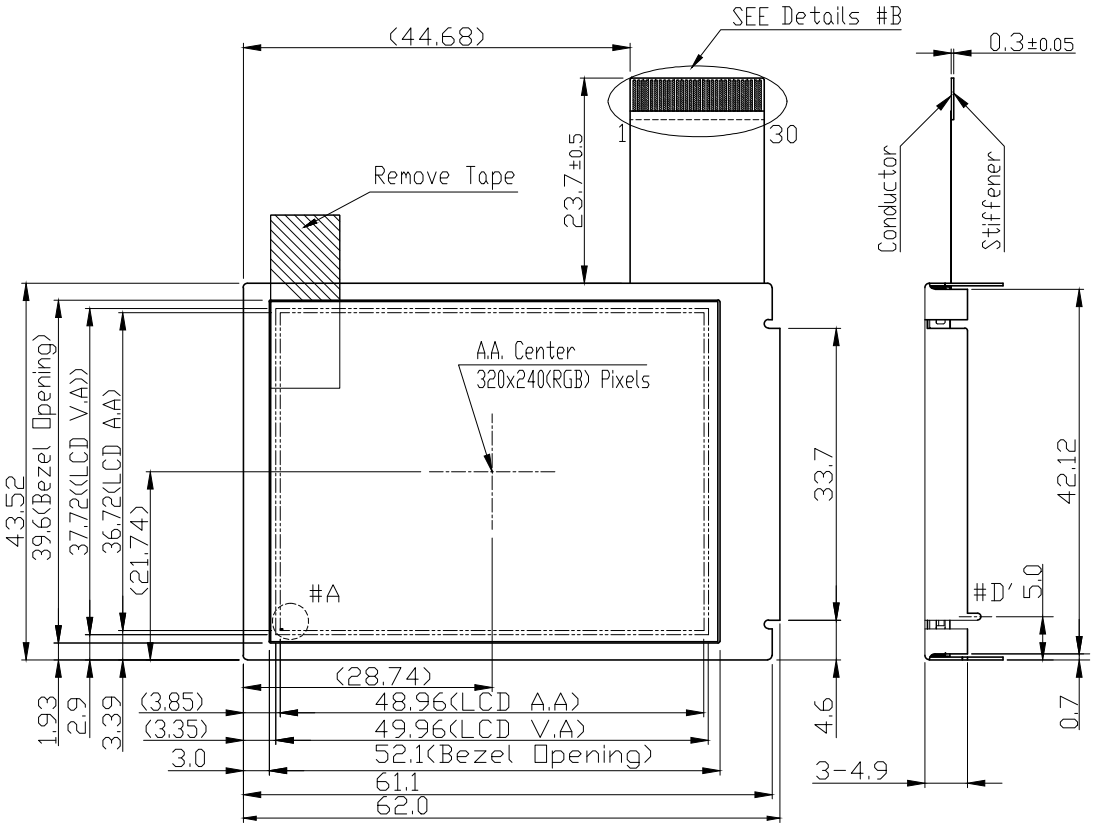
#B Details
Scale=2/1

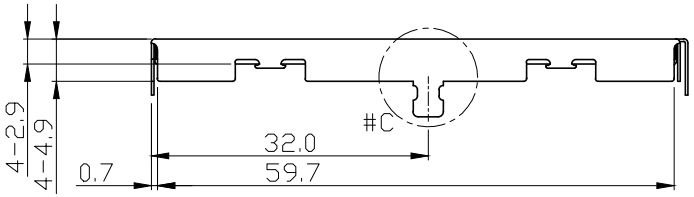


#C Details
Scale=4/1









Terminal	
No	Pin Name
1	VSS
2	NC
3	NC(SDO)
4	TE
5	D7
6	D6
7	D5
8	D4
9	D3
10	D2
11	D1
12	D0
13	VSS(SDA)
14	/RD
15	/WR(D/C)
16	D/C(SCL)
17	/CS
18	/RES
19	IM0
20	IM1
21	IM2
22	IM3
23	VDD
24	VSS
25	LED_A
26	LED_K1
27	LED_K2
28	LED_K3
29	LED_K4
30	VSS

Note:
*1. LCD Display Type : TFT, Transmissive(Full View)
*2. Pixel Arrangment : RGB-STRIPE
*3. Signal Interface : MCU_8 bits/SPI
*4. Color Depth : 262k Colors
*5. Operating Voltage : 3.3V
*6. Logic Voltage : 3.3V
*7. Backlight : White LEDs
*8. Backlight Supply : 4x20mA (VF=3.1V, TYP)
*9. Recommended Connector : P0.5x30Pin FFC Socket Or Equivalent
*10. Operating Temperature : -20°C~70°C
*11. Storage Temperature : -30°C~80°C

C		
B		
A		
Rev	Note	Date

Dwg Title	LMT024FNHFWA-1 Outline Dwg			
Dwg No.	MK-007077-1-1			Date 2020-10-10
Scale 3/2	Tol. ±0.3	Unit mm	Paper Size A3	
Approved	Checked		Drawn Luo Lin	

TOPWAY