MODEL NO : TM035PDHG09

MODEL VERSION: 00

SPEC VERSION : V1.0

ISSUED DATE: 2020.09.28

□Preliminary Specification
■Final Product Specification

Customer : 拓普微

Approved by	Notes

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This technical specification is subjected to change without notice

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Record of Revision

Rev	Issued Date	Description	Editor
1.0	2020-09-28	Preliminary Specification Release	Yanzhong_kong

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1 General Specifications

Feature		Spec
Display Spec.	Size	3.5 inch
	Resolution	320(RGB) x 480
	Technology Type	a-Si
	Pixel Configuration	R.G.B. Vertical Stripe
	Pixel pitch(mm)	0.153(H)x0.153(V)
	Display Mode	TM with Normally White
	Surface Treatment	HC
	Viewing Direction	6 o'clock
	Gray Scale Inversion Direction	12 o'clock
Mechanical Characteristics	LCM (W x H x D) (mm)	54.76 x 84.19 x 2.0
	Active Area(mm)	48.96x73.44
	With /Without TSP	Without TSP
	Matching Connection Type	ZIF
	LED Numbers	6 LEDs
	Weight (g)	13.3
Electrical Characteristics	Interface	MCU/RGB+SPI
	Color Depth	65K/262K
	Driver IC	ILI9488

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180 degree shift.

Note 2: Requirements on Environmental Protection: Q/S0002+HF

Note 3: LCM weight tolerance: ± 5%

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2 Input/Output Terminals

Pin No.	Symbol	I/O	Function	Remark
1	GND	P	Ground	
2	IOVCC	p	A supply voltage to the digital circuit. Connect to an external power supply of 1.65 ~ 3.6V.	
3	IOVCC	p		
4	VCI	P	A supply voltage to the analog circuit. Connect to an external power supply of 2.5 ~ 3.6V. supply of 2.5 ~ 3.6V.	
5	VCI	P		
6	IM0	I	Select the interface mode	
7	IM1	I		
8	IM2	I		
9	RESX	I	Reset input signal	
10	VSYNC	I	Frame synchronizing signal Fix to DGND level when not in use.	
11	HSYNC	I	Line synchronizing signal Fix to DGND level when not in use.	
12	PCLK	I	Dot clock signal Fix to DGND level when not in use.	
13	DE	I	A data ENABLE input signal Fix to DGND level when not in use.	
14	DB17/R5,Msb	I	Data Bus	
15	DB16/R4	I	Data Bus	
16	DB15/R3	I	Data Bus	
17	DB14/R2	I	Data Bus	
18	DB13/R1	I	Data Bus	
19	DB12/R0,Lsb	I	Data Bus	
20	DB11/G5,Msb	I	Data Bus	
21	DB10/G4	I	Data Bus	
22	DB9/G3	P	Data Bus	
23	DB8/G2	I	Data Bus	
24	DB7/G1	I	Data Bus	
25	DB6/G0,Lsb	I	Data Bus	
26	DB5/B5,Msb	I	Data Bus	
27	DB4/B4	I	Data Bus	
28	DB3/B3	I	Data Bus	
29	DB2/B2	I	Data Bus	

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30	DB1/B1	I	Data Bus	
31	DB0/B0,Lsb	I	Data Bus	
32	GND	p	Ground	
33	DOUT	O	Serial data output Leave the pin open when not in use.	
34	SDA	I/O	serial data input/output bi-direction pin Fix to DGND level when not in use.	
35	RDX	I	serve as a read signal Fix to IOVCC level when not in use.	
36	WRX_SCL	I	(WR) Write data enable pin in DBI Type B (SCL) Write data enable pin in DBI Type C If no used, please connect this pin to IOVCC	
37	DCX	I	Data/command selection pin If no used, please connect this pin to IOVCC	
38	CSX	I	Chip select signal If no used, please connect this pin to IOVCC	
39	XR(X+)	-	NC	
40	YD(Y-)	-	NC	
41	XL(X-)	-	NC	
42	YU(Y+)	-	NC	
43	LEDA	P	LED ANODE	
44~49	LEDK	P	LED CATHODE	
50	GND	P	Ground	

Note1: I/O definition：I-----Input O---Output P----Power/ Ground NC---Not Connected

IM2	IM1	IM0	Interface
0	0	0	MIPI-DBI Type B 24-bit bus (DB_EN = 1)
0	0	0	MIPI-DBI Type B 18-bit bus (DB_EN = 0)
0	0	1	MIPI-DBI Type B 9-bit bus
0	1	0	MIPI-DBI Type B 16-bit bus
0	1	1	MIPI-DBI Type B 8-bit bus
1	0	1	MIPI-DBI Type C Option 1 (3-line SPI)
1	1	0	MIPI DSI
1	1	1	MIPI-DBI Type C Option 3 (4-line SPI)

Table 2.1 Select the interface mode

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3 Absolute Maximum Ratings

GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Power Voltage	VCI	-0.3	3.6	V	Note1
Logic supply voltage	IOVCC	-0.3	3.6	V	
Operating Temperature	Top	-20	70	℃	
Storage Temperature	Tst	-30	80	℃	
Relative Humidity Note2	RH	--	≤95	%	Ta≤40℃
		--	≤85	%	40℃ <Ta≤50℃
		--	≤55	%	50℃ <Ta≤60℃
		--	≤36	%	60℃ <Ta≤70℃
		--	≤24	%	70℃ <Ta≤80℃
Absolute Humidity	AH	--	≤70	g/m³	Ta>70℃

Table 3.1 Absolute Maximum Ratings

Note1:

1. Even if the absolute maximum rating of one of the above parameters is exceeded only for a short while, the quality of the product may be degraded. Therefore, be sure to use the product within the range of the absolute maximum ratings.

2. Do not apply to automotive products.

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4 Electrical Characteristics

4.1 LCD module

Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Logic Signal Input /Output Voltage		IOVCC	1.65	1.8	3.6	V	
Power Supply Voltage		VCI	2.5	2.8	3.6	V	
Input Signal Voltage	High Level	VIH	0.7*IOVCC	-	IOVCC	V	
	Low Level	VIL	-0.3	-	0.3*IOVCC	V	
Output Signal Voltage	High Level	VOH	0.8*IOVCC	-	IOVCC	V	
	Low Level	VOL	0	-	0.2*IOVCC	V	
(Panel+LSI) Power Consumption		Black Mode	-	TBD	-	mW	
		Sleeping Mode	-	TBD	-	mW	

Table 4.1 LCD module electrical characteristics

Notes:

1. Ta = -40 to 85 °C (no damage up to 85℃ (at maximum)), IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, DGND=0V.
2. Supply the digital IOVCC voltage equal to or less than the analog VCI voltage.

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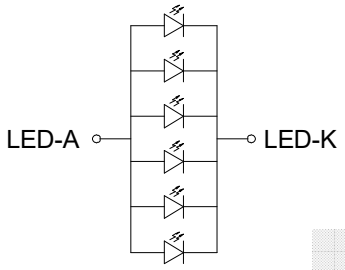
4.2 Backlight Unit

Ta=25℃

Item	Symbol	Min	Typ	Max	Unit	Remark
Forward Current	I_F	-	20	-	mA	1 LED
Forward Voltage	V_F	-	3.2	-	V	1 LED
Backlight Power Consumption	W_{BL}	-	384	-	mW	6 LEDs in parallel
LED lifetime			30,000		hrs	

Note1: Figure below shows the connection of backlight LED.



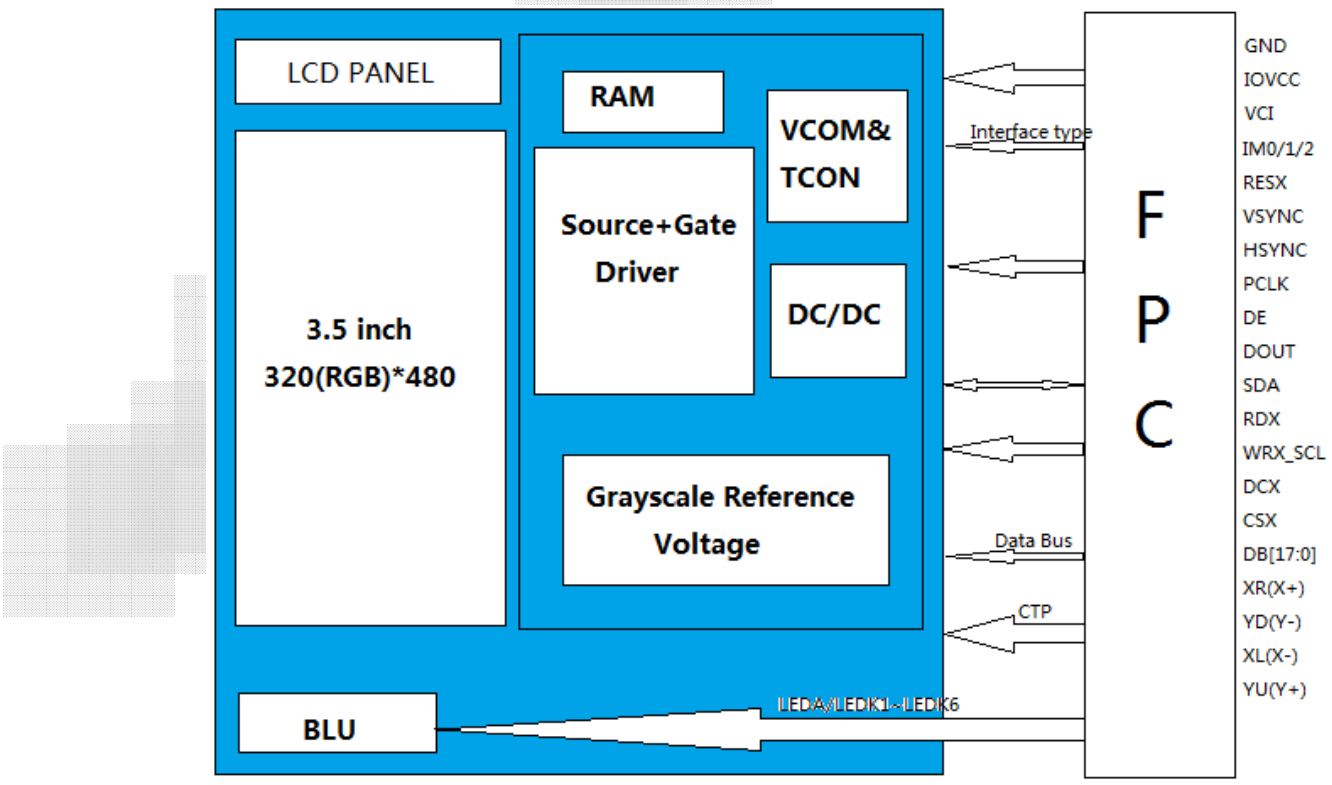
Note 2: 1LED: V_F =3.2V I_F =20mA

Note 3: : I_F is defined for one LED.

Optical performance should be evaluated at Ta=25℃ only.

If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

4.3 Block Diagram



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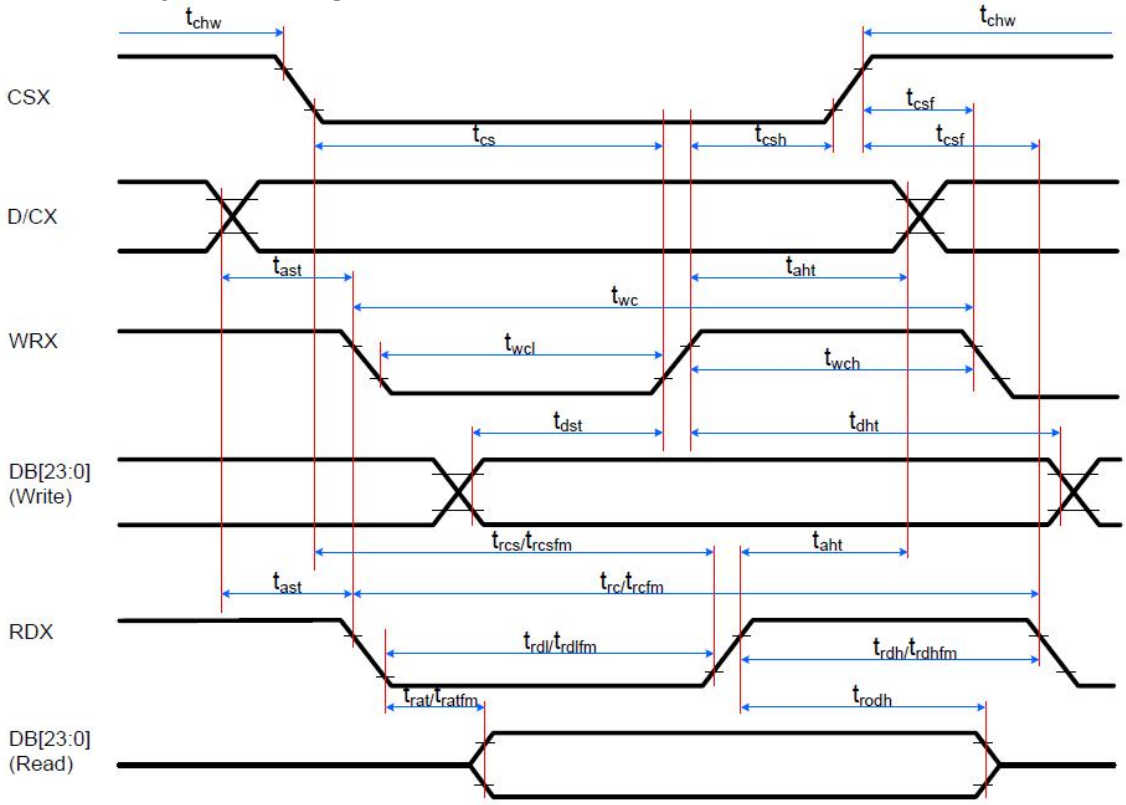
5 Timing Chart

5.1 DBI Type B

5.1.1 DBI Type B Timing Characteristic



Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	taht	Address hold time (Write/Read)	0	-	ns	-
CSX	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
WRX	twc	Write cycle	40	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB [23:0], DB [17:0], DB [15:0], DB [8:0], DB [7:0]	tdst	Write data setup time	10	-	ns	For maximum, CL=30pF For minimum, CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

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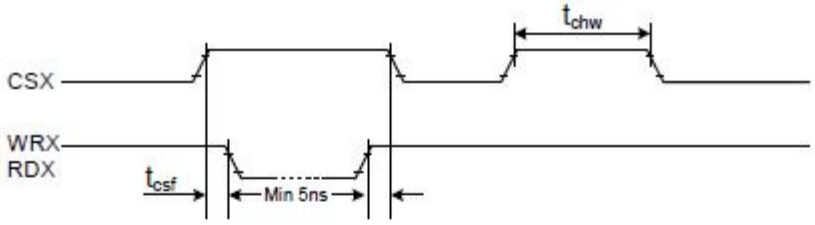
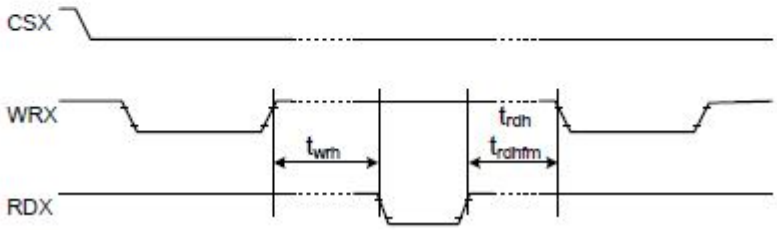
Notes:

1. Ta = -40 to 85 °C, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V
2. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.
3. Input signal rising time and falling time:

7. The CSX timing:



8. The Write to Read or the Read to Write timing:



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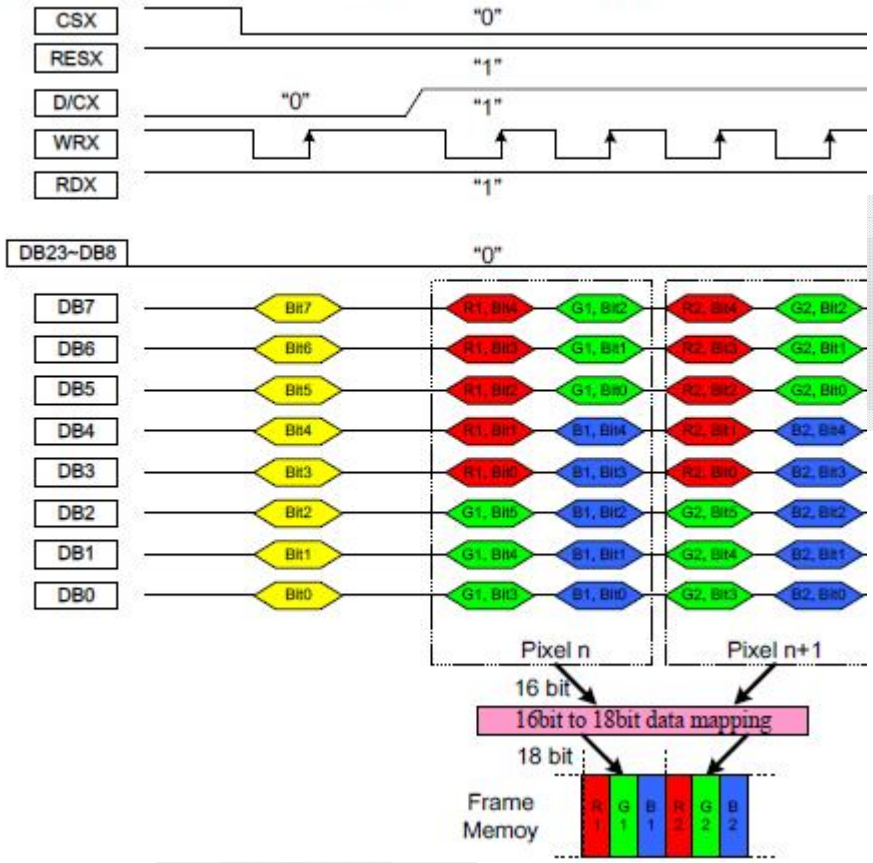
5.1.2 DBI Type B Data Bus

8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color



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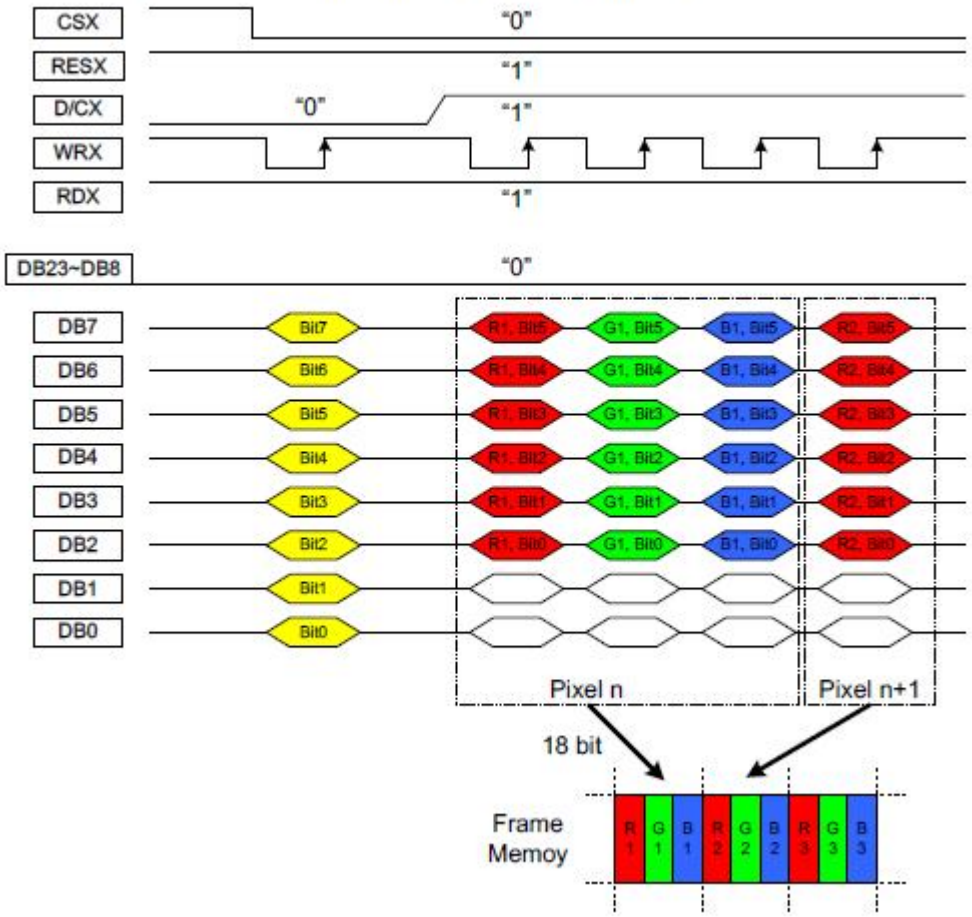
8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



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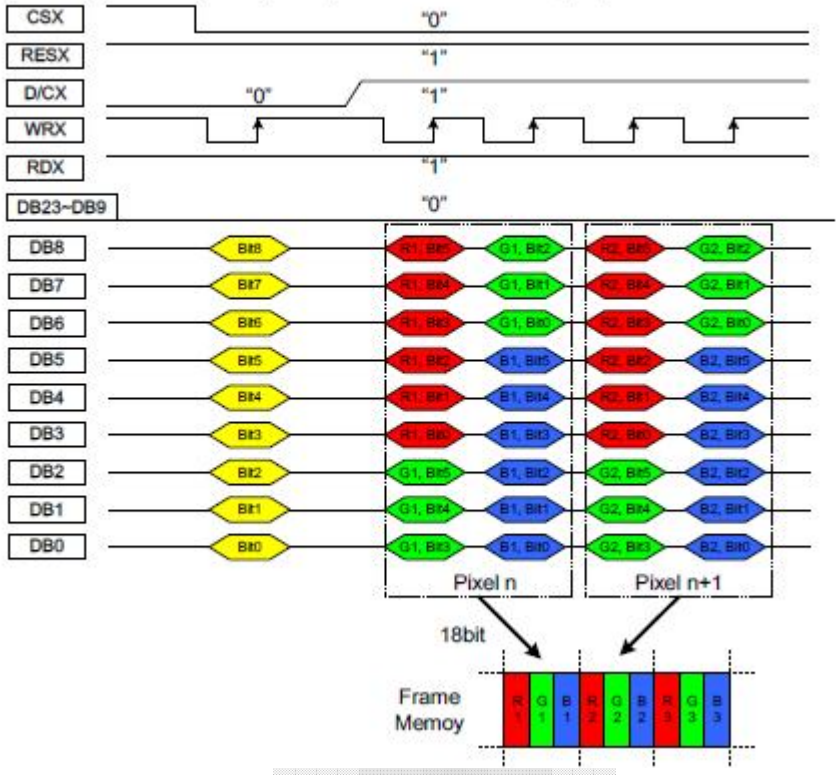
9-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



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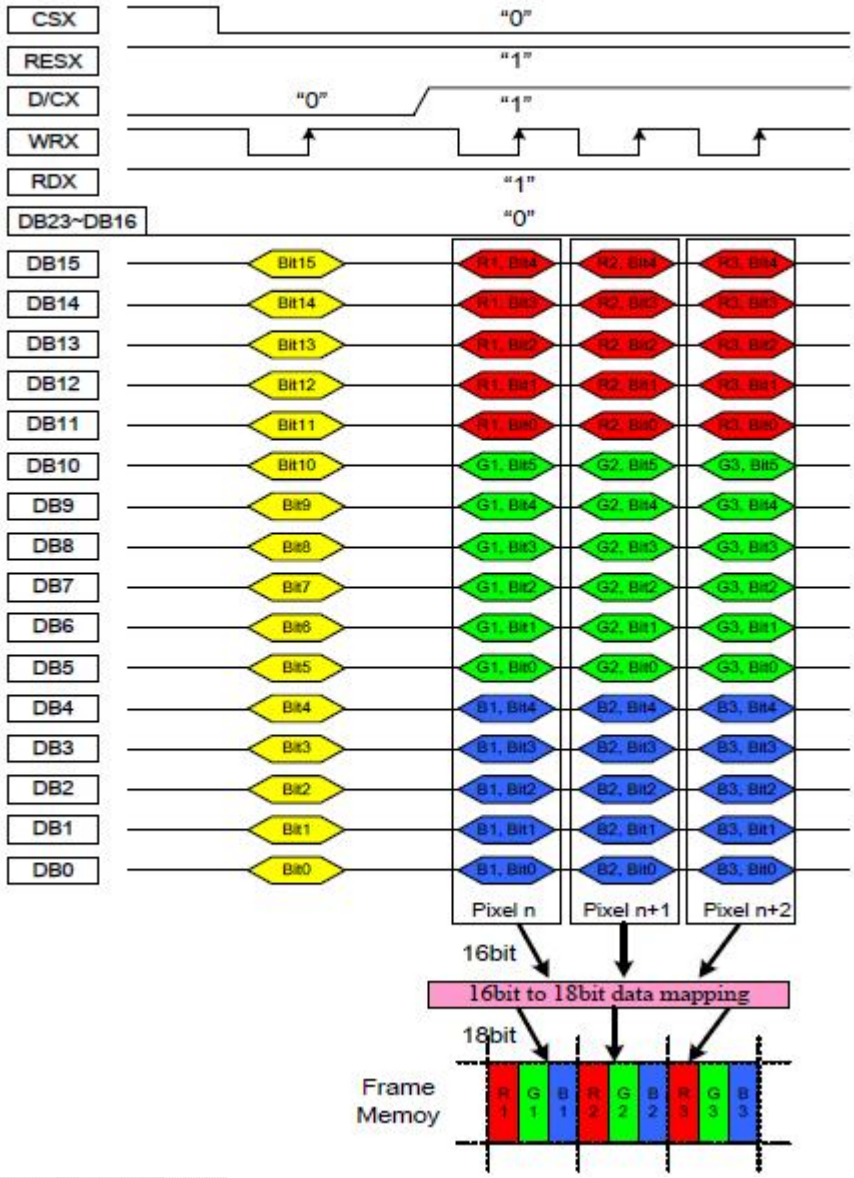
16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color



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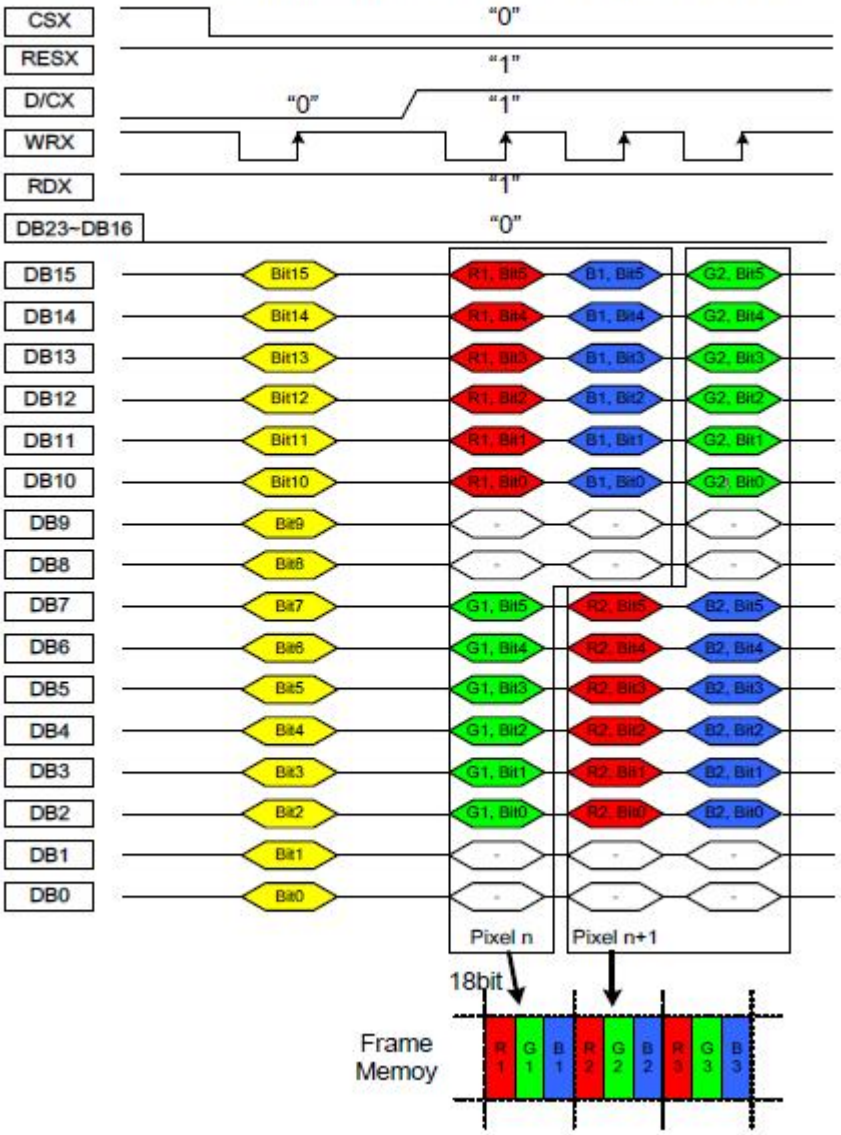
16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



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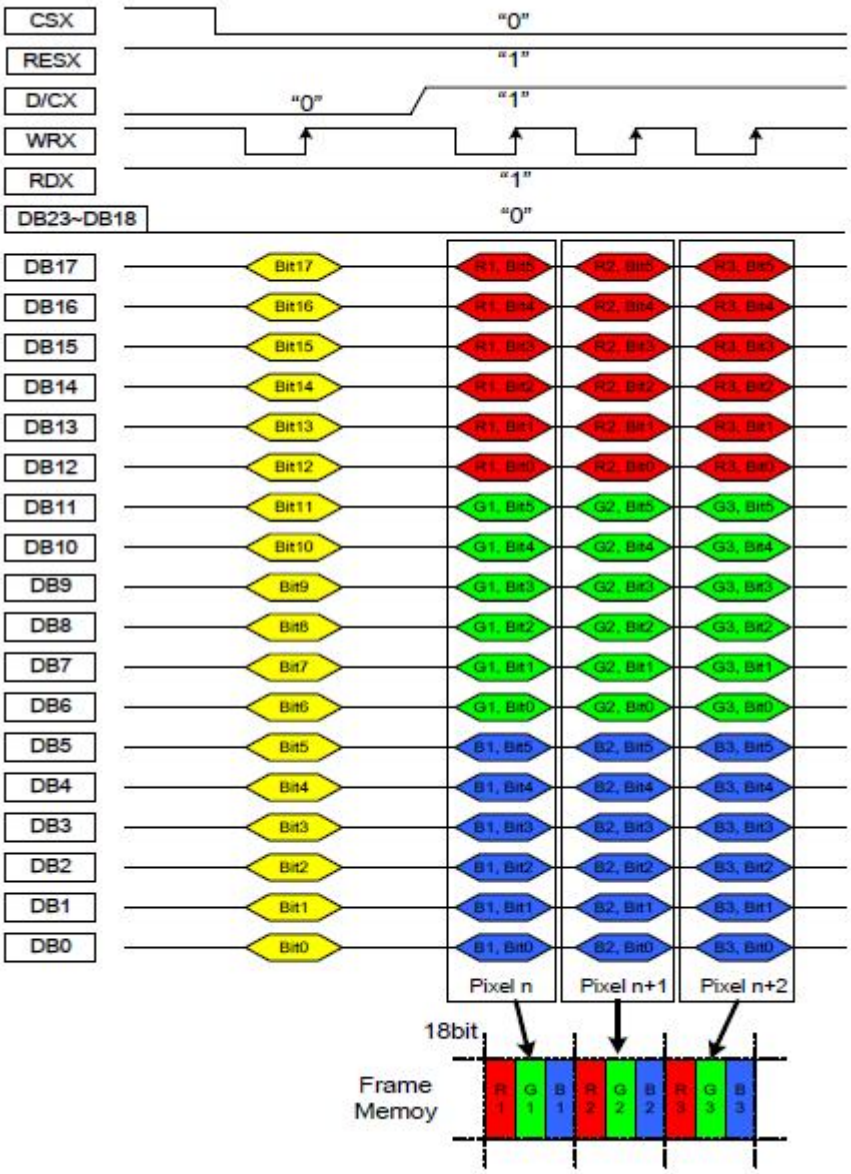
18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



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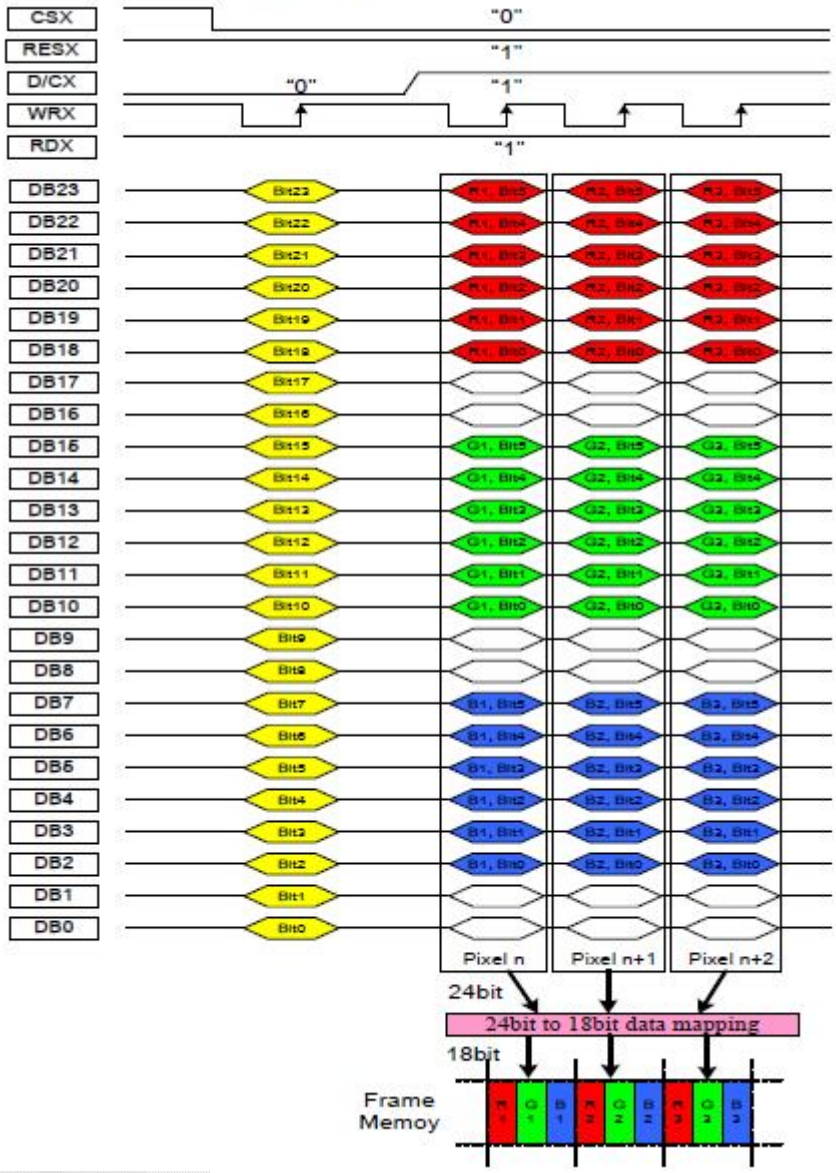
24-bit Data Bus for 24-bit/pixel (RGB 8-8-8 Bits Input), 262K-color



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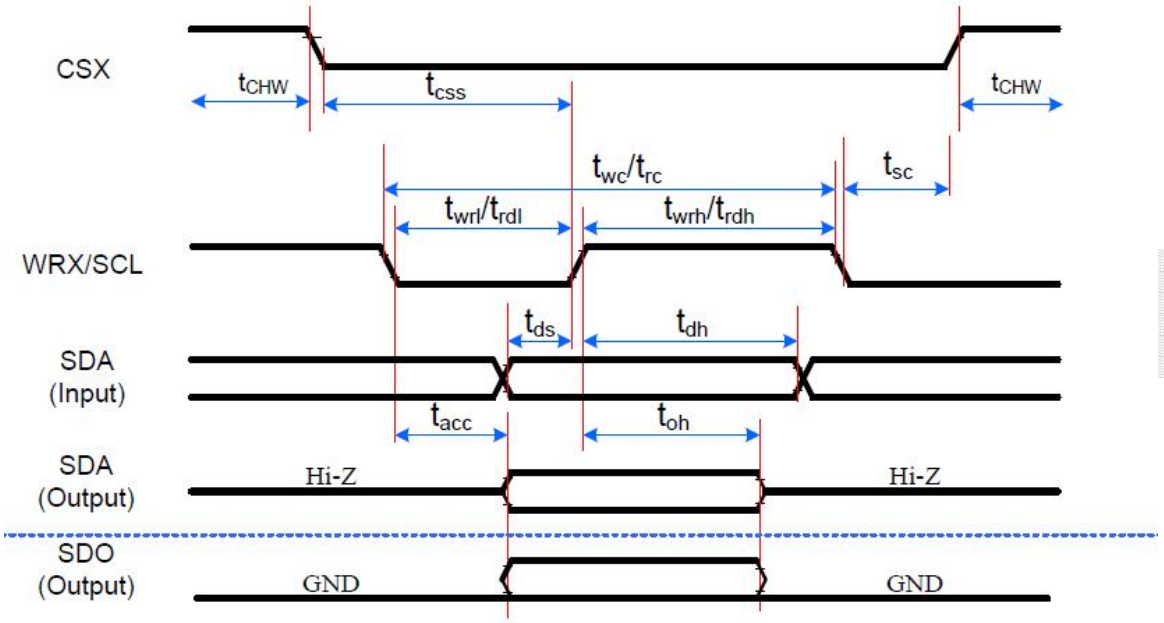
5.2 3-Line SPI Interface Timing Characteristic



Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchw	CSX H Pulse Width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
	twrl	SCL L Pulse Width (Write)	15	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	toh	Output disable time (Read)	15	50	ns	

Note: Ta = -40 to 85 °C, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns

5.3 4-Line SPI Interface Timing Characteristic

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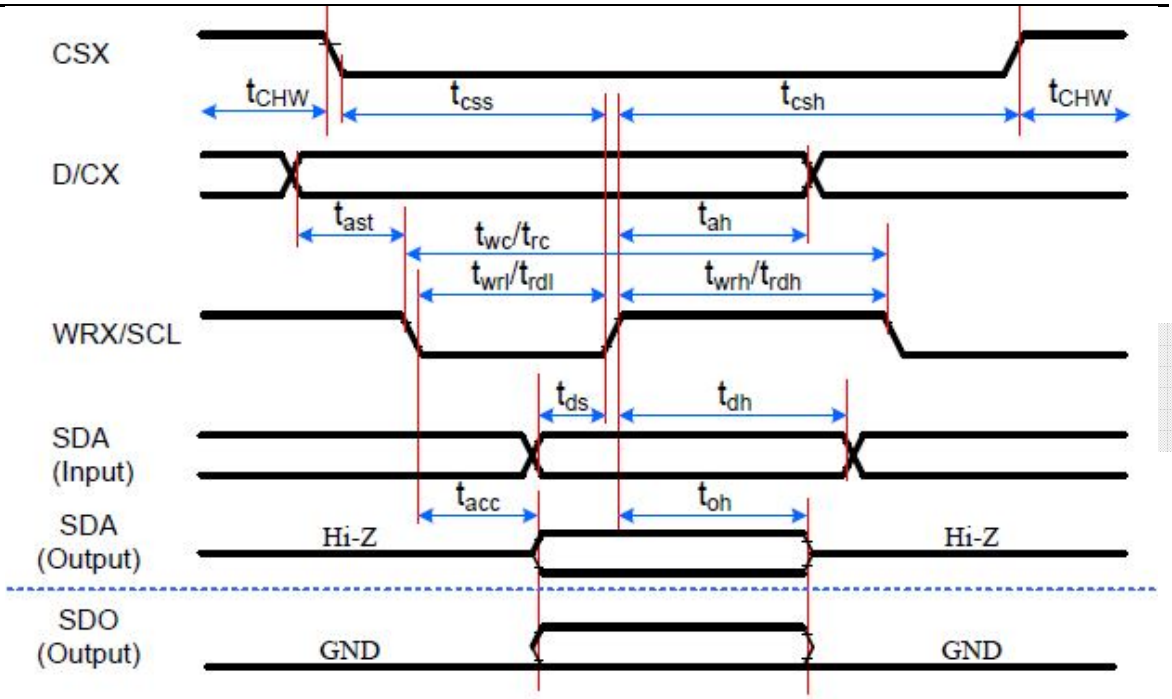

Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS H pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	50	-	ns	
	twrh	SCL H pulse width (Write)	10	-	ns	
	twrl	SCL L pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	-	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	tod	Output disable time (Read)	15	50	ns	

Notes:

3. Ta = -40 to 85 °C, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns.

2. Does not include signal rising and falling times.

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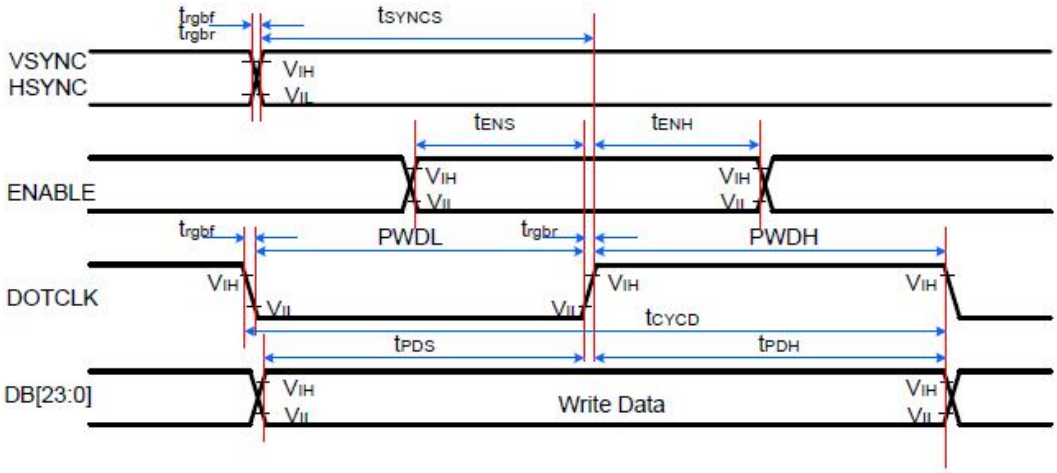
5.4 DPI Interface

5.4.1 DPI Interface Characteristic

DPI (Display Parallel 16-/18-/24-bit interface) Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	16-/18-/24-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB [23:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	20	-	ns	
	PWDL	DOTCLK low-level period	20	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -40 to 85 °C, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V

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5.4.2 DPI Interface pixel format

24-bit DPI interface connection (DB [23:0] is used): set pixel format DPI [2:0] = 3'h7

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R[7]	R[6]	R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

18-bit DPI interface connection (DB [17:0] is used): set pixel format DPI [2:0] = 3'h6

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
						R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit DPI interface connection (DB [15:0] is used): set pixel format DPI [2:0] = 3'h5

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
								R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

The Pixel clock (DOTCLK) runs all the time without stop. It is used to enter VSYNC, HSYNC, ENABLE and DB [23:0] states when there is a rising edge of the DOTCLK. The DOTCLK cannot be used as the internal clock for other functions of the display module.

Vertical synchronization (VSYNC) is used to indicate when a new frame of the display is received. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to indicate when a new line of the frame is received. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Data Enable (ENABLE) is used to indicate when the RGB information that should be transferred in the display is received. This is a high enable, and its state is read to the display module by a rising edge of the DOTCLK signal.

DB [23:0] is used to indicate what is the information of the image that is transferred on the display (when ENABLE = 0 (low) and there is a rising edge of DOTCLK). DB [23:0] can be 0 (low) or 1 (high). These lines are read by a rising edge of the DOTCLK signal. In RGB interface modes, the input display data is written to GRAM first then outputs the corresponding source voltage according to the gray data from GRAM.

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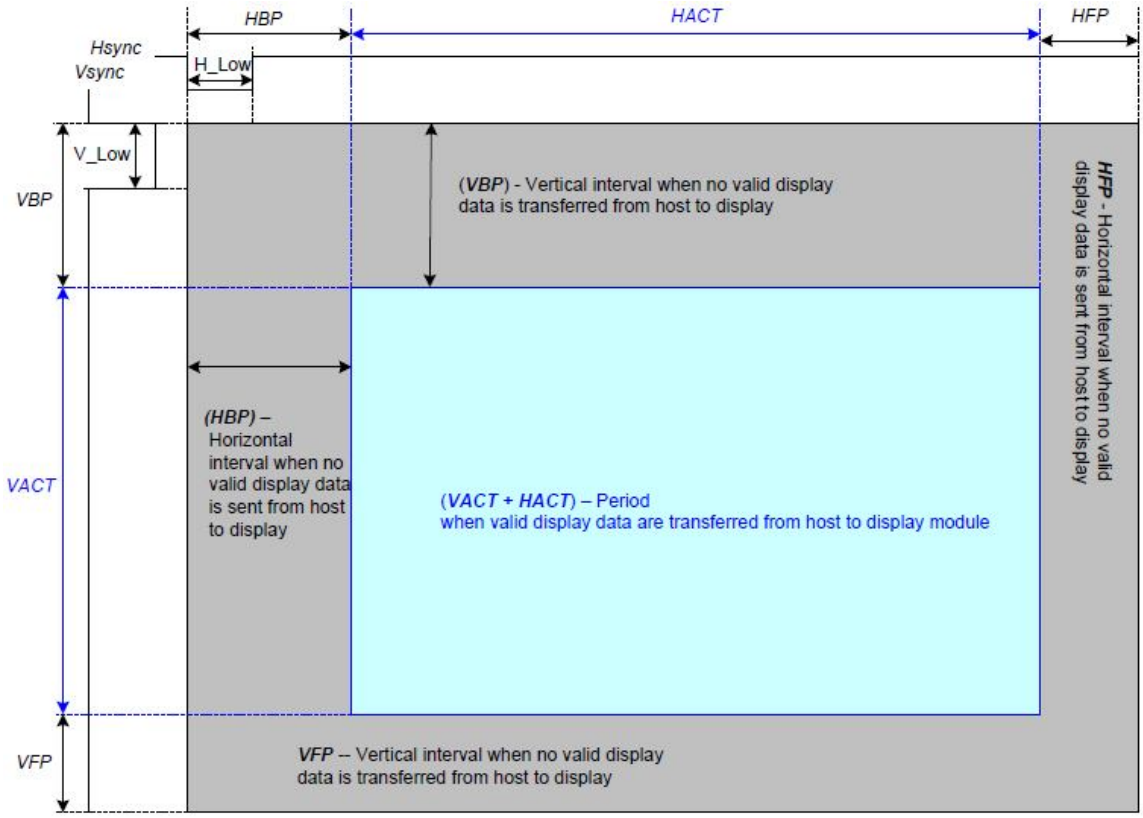
5.4.3 DPI(RGB) Interface timing



DPI Parameters Setting(BYPASS bit = 0)

Parameters	Symbols	Min.	Typ.	Max.	Units
Horizontal Synchronization	H_Low	3	-	H_Low < HBP	DOTCLK
Horizontal Back Porch	HBP	3	-	192	DOTCLK
Horizontal Front Porch	HFP	3	-	255	DOTCLK
Horizontal Address	HACT	-	320	-	DOTCLK
Horizontal Frequency		-	-	33	KHz
Vertical Synchronization	V_Low	1	-	V_Low < VBP	Line
Vertical Back Porch	VBP	2	-	V_Low+VBP+VFP < 32	Line
Vertical Front Porch	VFP	2	-		Line
Vertical Address	VACT	-	480	-	Line
Vertical Frequency		60	-	70	Hz
DOTCLK cycle		100	-	50	ns
DOTCLK Frequency		10	-	20	MHz

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DPI Parameters Setting(BYPASS bit = 1)

Parameters	Symbols	Min.	Typ.	Max.	Units
Horizontal Synchronization	H_Low	3	-	H_Low < HBP	DOTCLK
Horizontal Back Porch	HBP	20	-	192	DOTCLK
Horizontal Front Porch	HFP	70	-	255	DOTCLK
Horizontal Address	HACT	-	320	-	DOTCLK
Horizontal Frequency		-	-	33	KHz
Vertical Synchronization	V_Low	1	-	V_Low < VBP	Line
Vertical Back Porch	VBP	2	-	V_Low+VBP+VFP < 32	Line
Vertical Front Porch	VFP	2	-		Line
Vertical Address	VACT	-	480	-	Line
Vertical Frequency		60	-	70	Hz
DOTCLK cycle		83.3	-	50	ns
DOTCLK Frequency		12	-	20	MHz

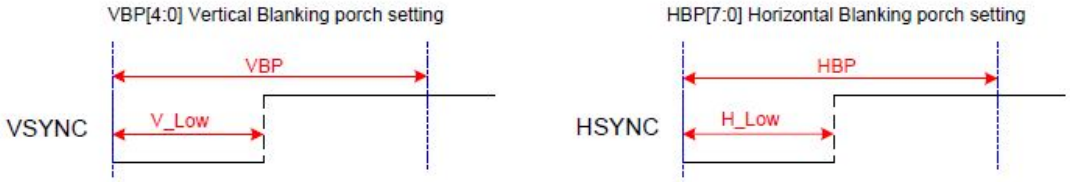
$$\text{Frame Rate} = \frac{\text{DOTCLK}}{(\text{Display Pixel}+\text{HBP}+\text{HFP}) \times (\text{Display line}+\text{VBP}+\text{VFP})}$$

Display line : The number of gate-lines

Display pixel :The number of pixels in one gate-line

Example：DOTCLK = 20Mhz, TE=70Hz, VBP=2, VFP=2, HBP=100, HFP=170.

Note: VBP[4:0]/HBP[7:0] (Blanking Porch Control, RB5h) define as follows:



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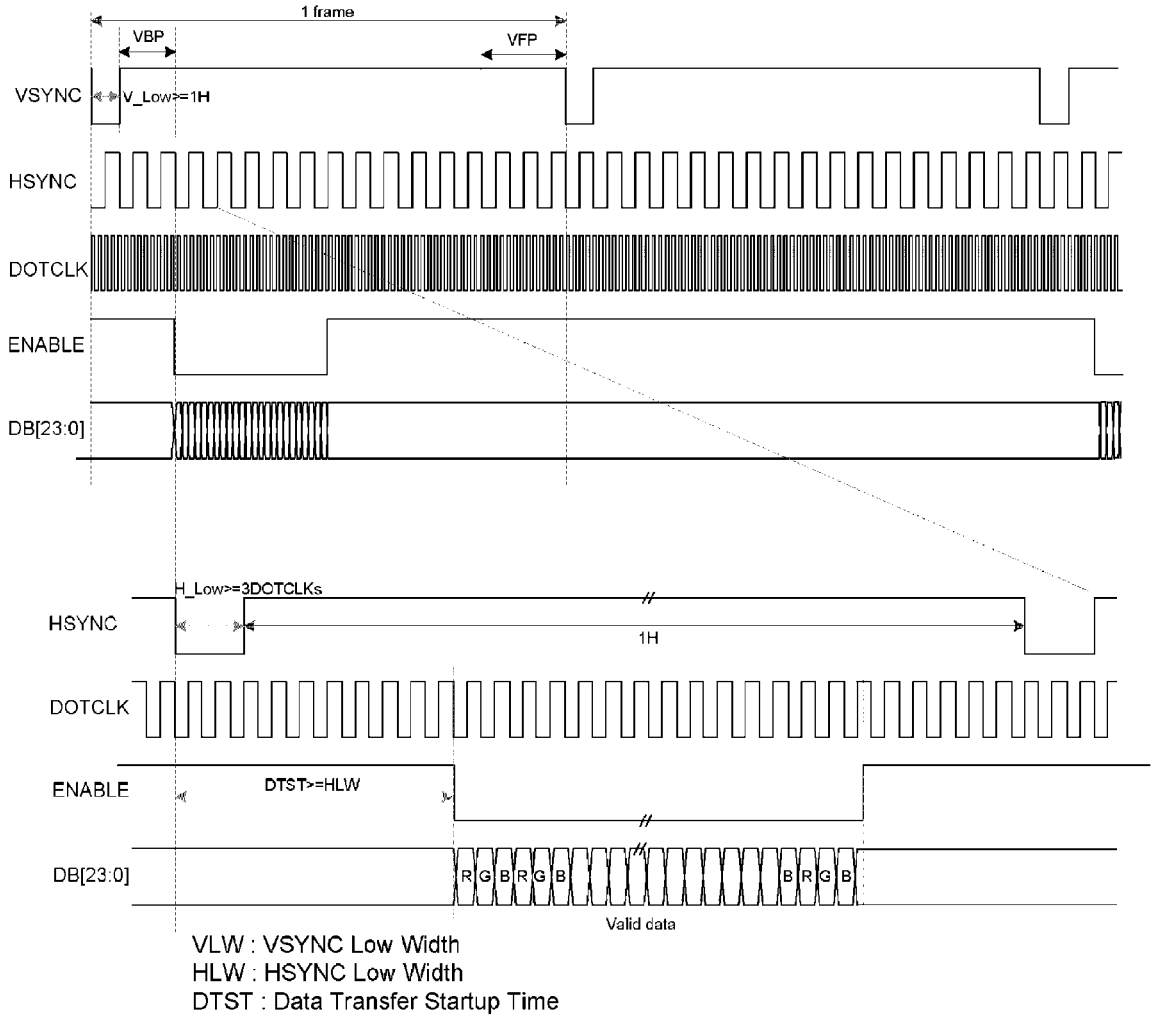

Note: VSPL = 0, HSPL = 0, DPL = 0 and EPL = 0 of Interface Mode Control B0h command.

5.4.4 DPI（RGB Interface）Data Bus

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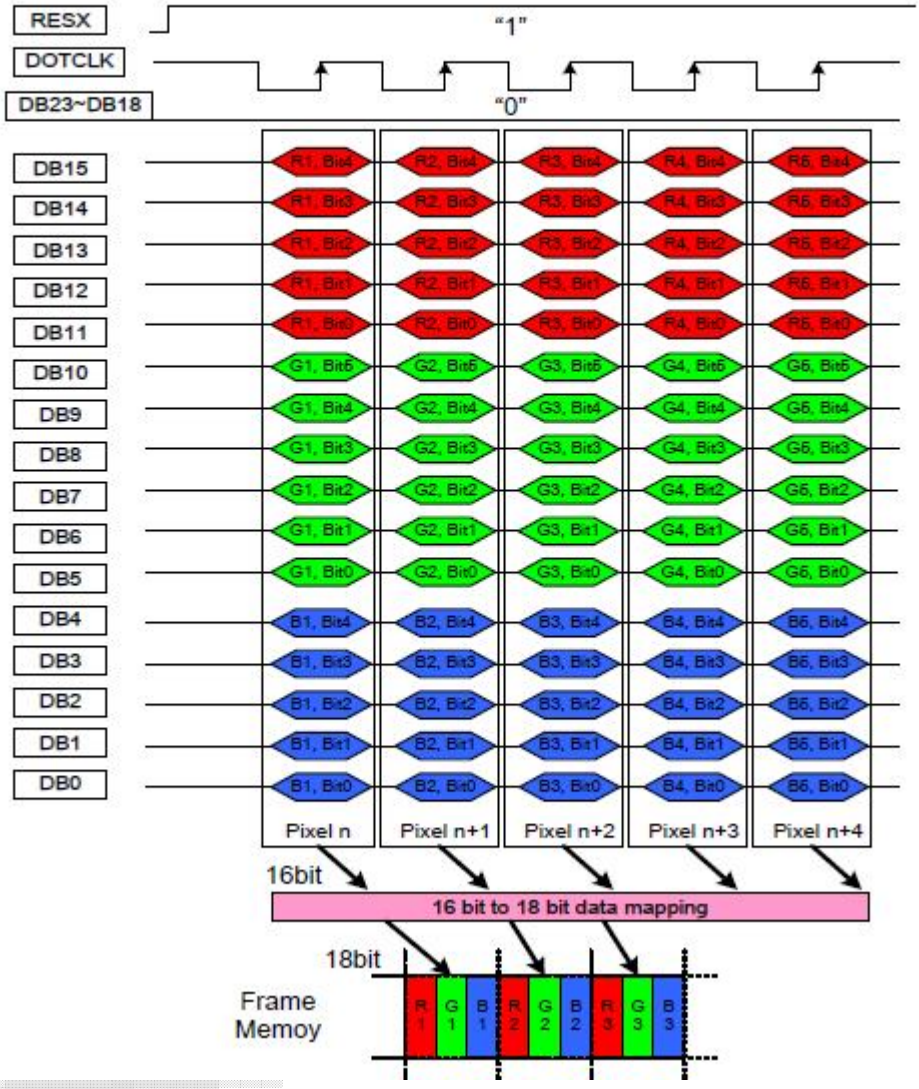
16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits as 101. The display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. Display data is transferred to the internal GRAM through the 16-bit RGB data bus in synchronization with the display operation.



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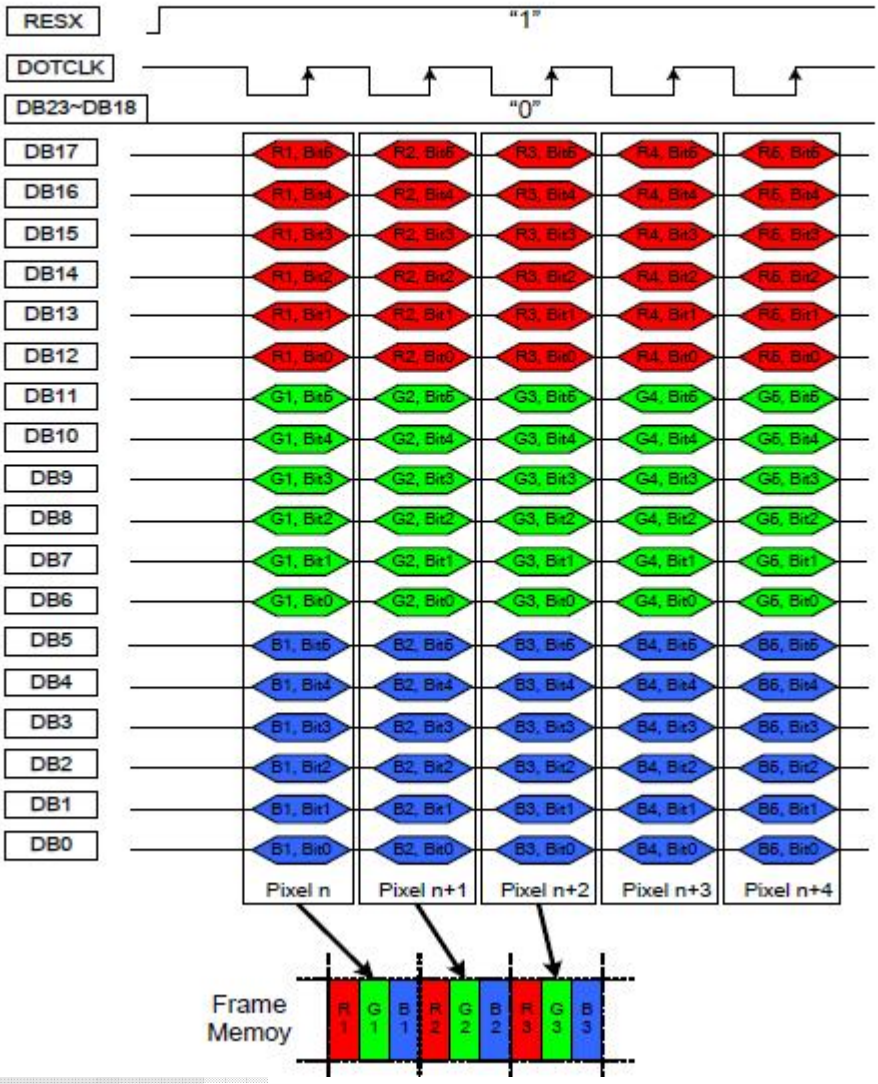
18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits as 110. The display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. Display data is transferred to the internal GRAM through the 18-bit RGB data bus in synchronization with the display operation.



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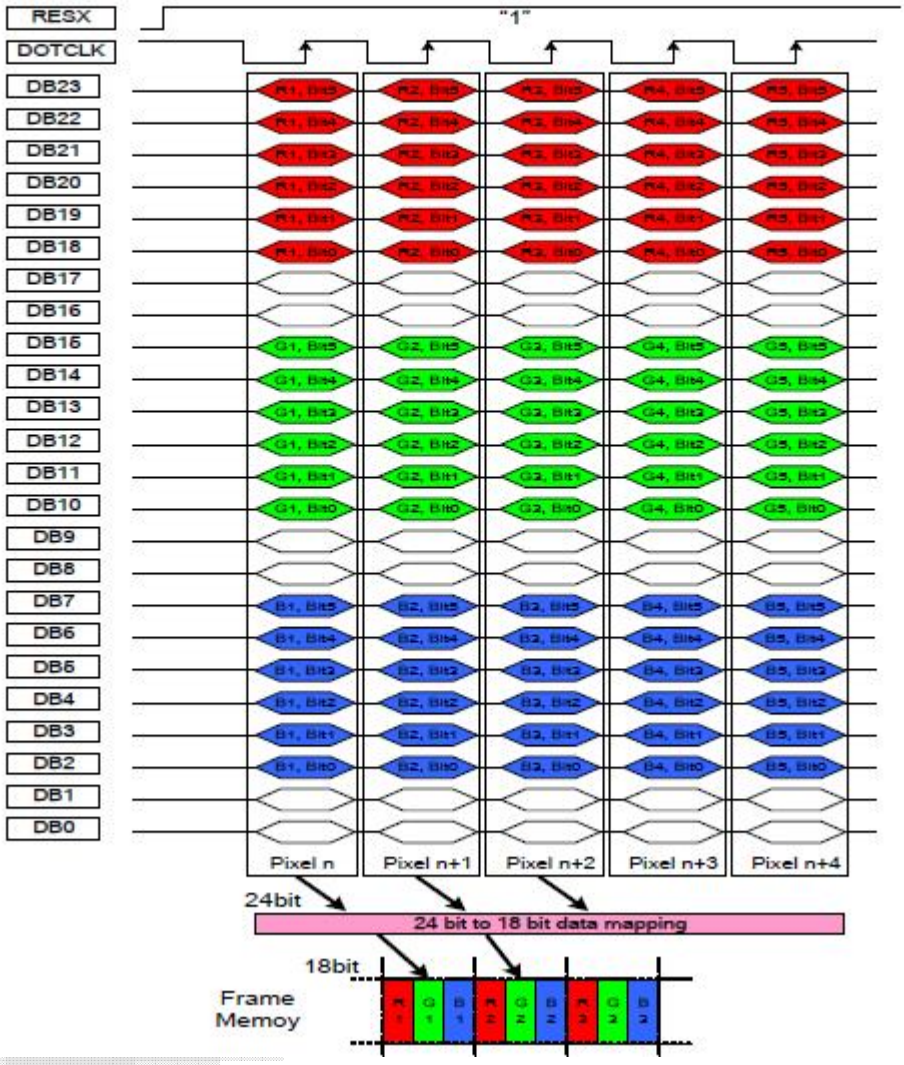
24-bit Parallel RGB Interface

18-bit/pixel

The 24-bit RGB interface is selected by setting the DPI [2:0] bits to 111 and DB_EN to 1. The display operation is synchronized with VSYNC, HSYNC, ENABLE, and DOTCLK signals. Display data is transferred to the internal GRAM through the 18-bit RGB data bus in synchronization with the display operation.



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24-bit/pixel Constrained by Dither and Bypass

The 24-bit RGB interface is selected by setting the DPI [2:0] bits as 111, DB_EN as 1, Dither_Enable as 1, and Bypass as 1. The display operation is synchronized with VSYNC, HSYNC, ENABLE and DOTCLK signals.

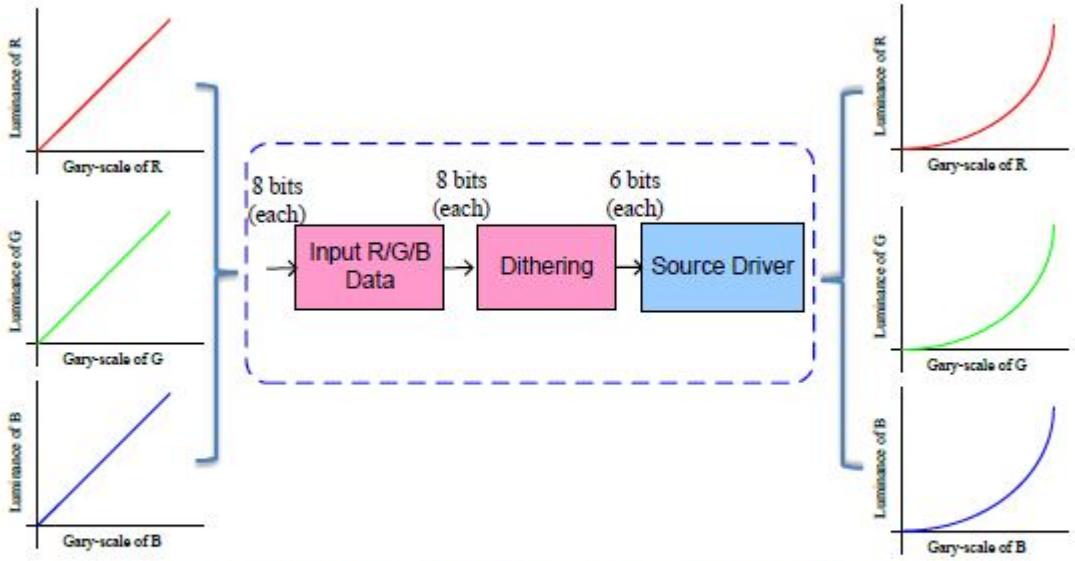

Figure 122: 24-bit/pixel 16.7M Colors Order on the DPI Interface

Notes:

2. To configure the Bypass, please refer to the Section 5.3.7 Display Function Control (B6h).
3. 1-time transfer is used to transmit 1 pixel data to the 24-bit color depth information.

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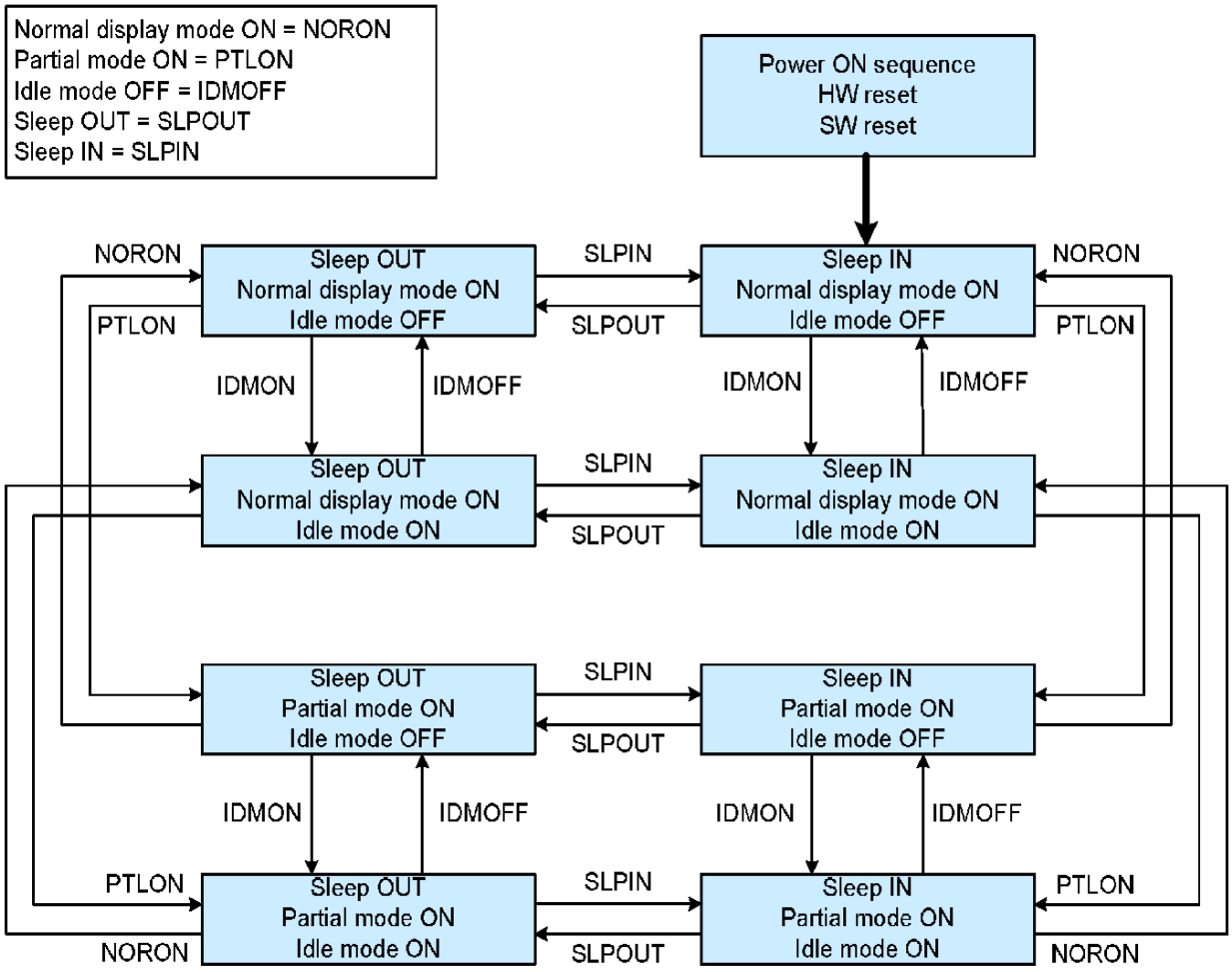
5.5 Power ON/OFF Sequence



Notes:

1. There are not any abnormal visual effects when one power mode changes to another power mode.
2. There is not any limitation, which is not specified by users, when one power mode changes to another power mode.

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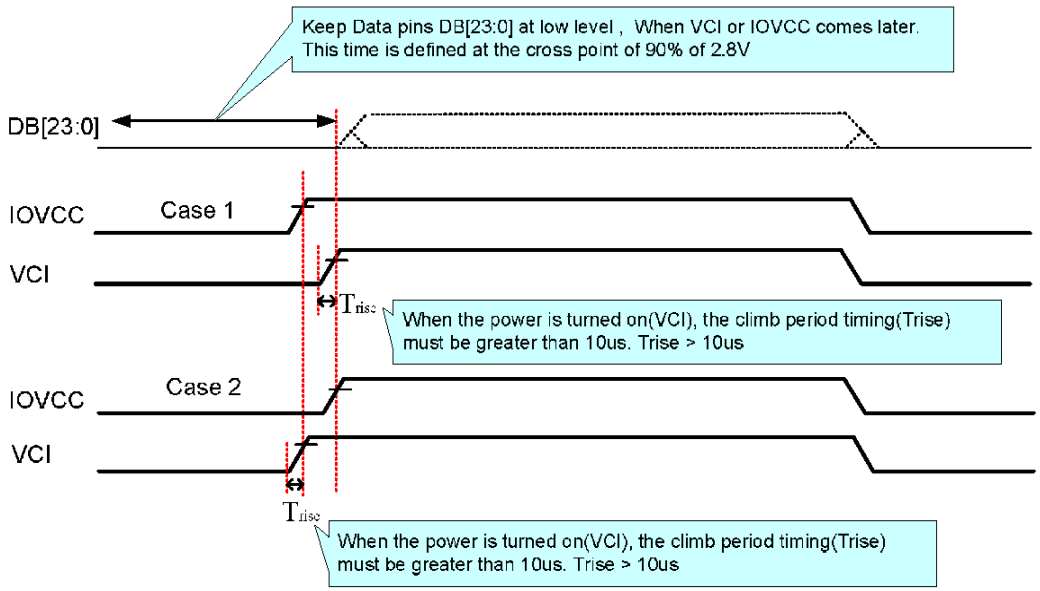
IOVCC and VCI can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VCI and IOVCC must be powered down with a minimum of 120msec. If the LCD is in the Sleep In mode, VCI and IOVCC can be powered down with a minimum of 0msec after the RESX has been released.
CSX can be applied at any time or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ILI9488 if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequence.
3. There will be no abnormal visible effects on the display between the end of the Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 11.1 and 11.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.
5. When the power is turned on, the climb period timing(Trise) must be greater than 10us.
6. Keep data pins DB[23:0] at low level, when VCI or IOVCC comes later



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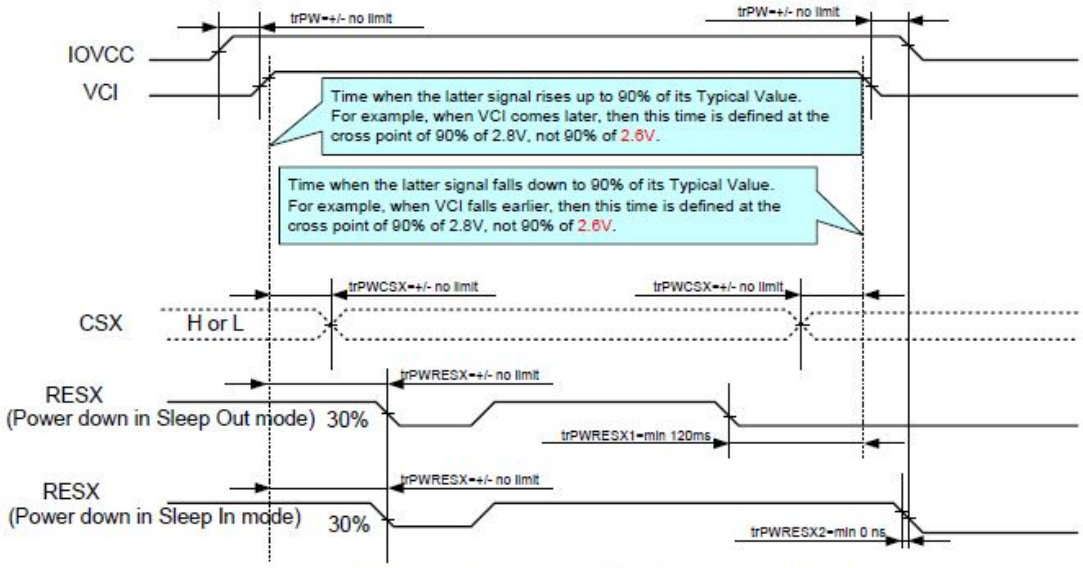
Case 1 – RESX Line is Held High or Unstable by Host at Power ON

If the RESX line is held High or unstable by the host during Power On, then Hardware Reset must be applied after both VCI and IOVCC have been applied. Otherwise, the correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note: Unless otherwise specified, timings herein show the cross point at 50% of the signal power level.

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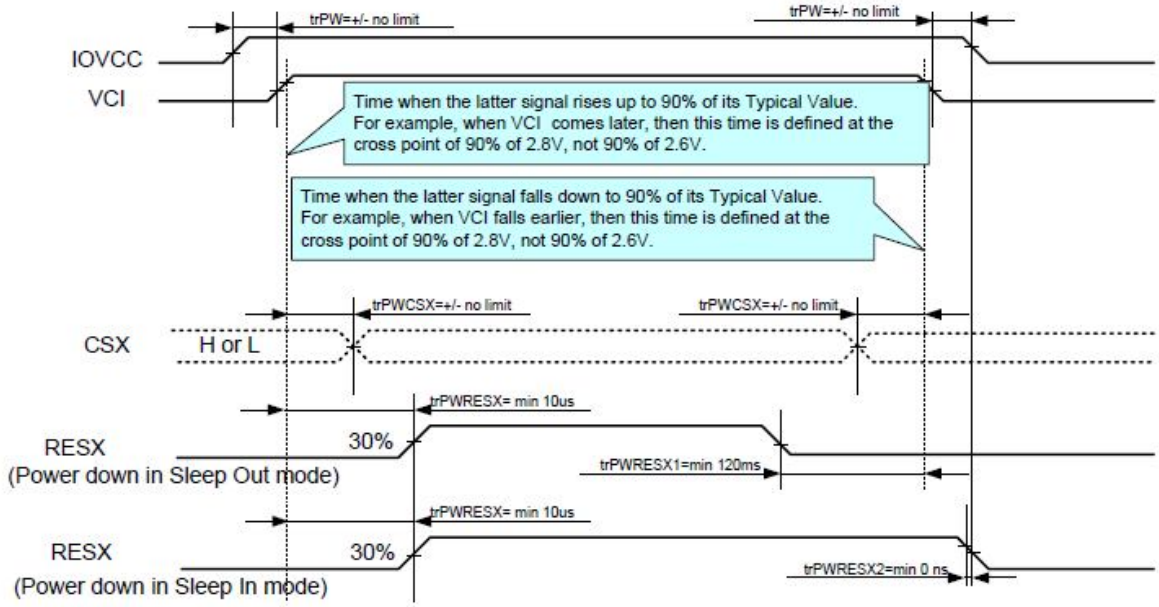
Case 2 – RESX Line is Held Low by Host at Power ON

If the RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for a minimum of 10µsec after both VCI and IOVCC have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note: Unless otherwise specified, timings herein show the cross point at 50% of the signal power level.

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5.6 Reset timing

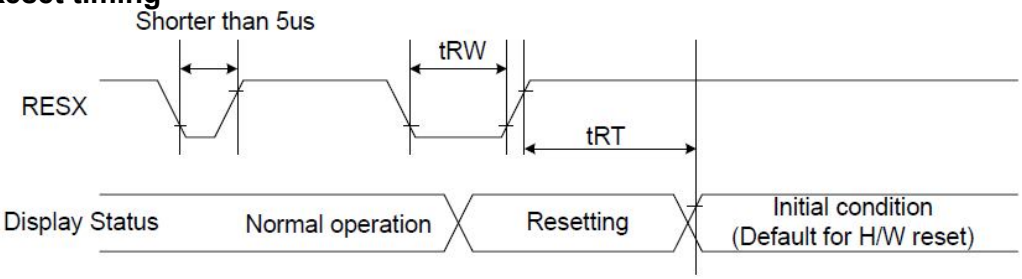


Table 39: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

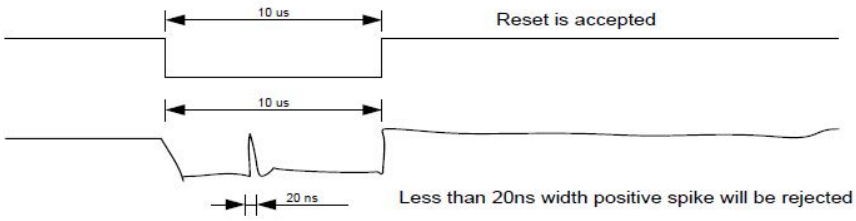
Notes:

1. The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
2. According to the Table 40, a spike due to an electrostatic discharge on the RESX line does not cause irregular system reset.

Reset Description

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Reset period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains the blank state in the Sleep In mode.) and then return to the default condition for the Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:



Positive Noise Pulse during Reset Low

5. When Reset is applied during the Sleep In Mode.
6. When Reset is applied during the Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. The Sleep Out command also cannot be sent in 120msec.

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6 Optical Characteristics

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	60	70		Degree	Note2,3
		θB		50	60			
		θL		60	70			
		θR		60	70			
Contrast Ratio		CR	θ=0°	400	500			Note 3
Response Time		T_{ON}	25℃		25	35	ms	Note 4
		T_{OFF}						
Chromaticity	White	x	Backlight is on		0.286			Note 1,5
		y			0.304			
	Red	x			0.608			Note 1,5
		y			0.336			
	Green	x			0.341			Note 1,5
		y			0.604			
	Blue	x			0.146			Note 1,5
		y			0.073			
Uniformity		U			80		%	Note 6
NTSC					60		%	Note 5
Luminance		L		250	300		cd/m^2	Note 7

Test Conditions:

1. I_F= **20** mA, and the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

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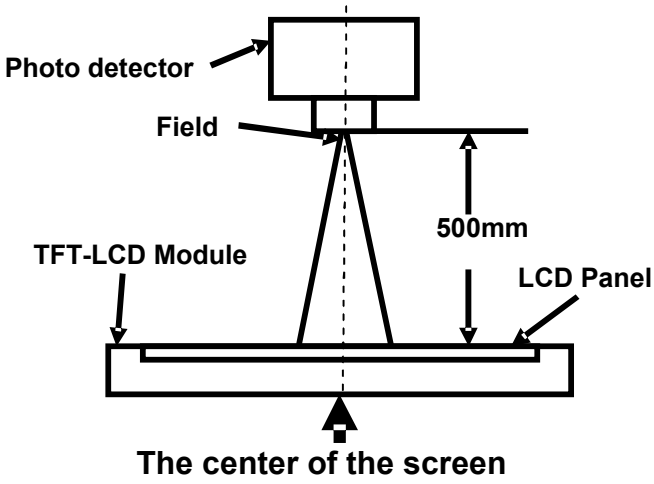
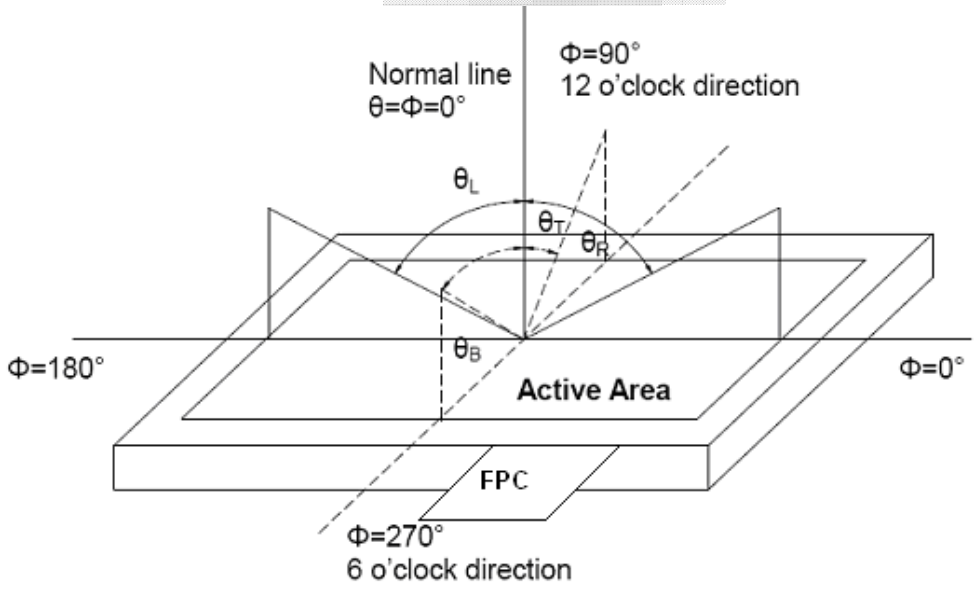
Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD.



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

"White state ": The state is that the LCD should drive by Vwhite.

"Black state": The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

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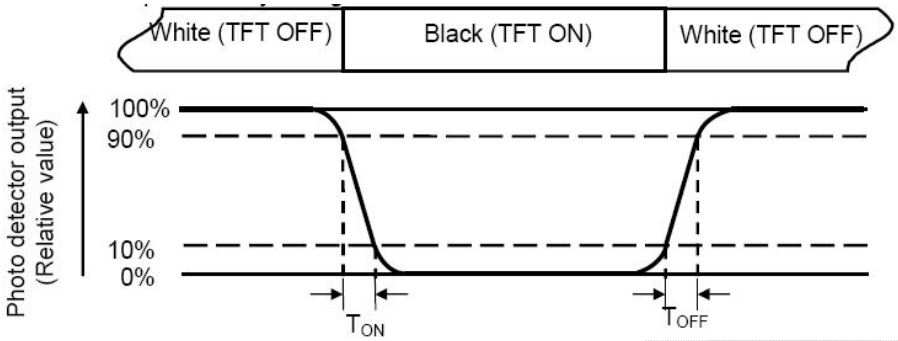
Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

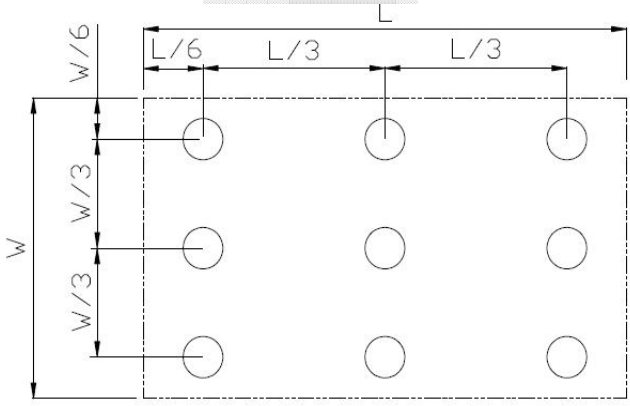
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

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Shenzhen TOPWAY Technology CO.,Ltd.

7 Environmental / Reliability Test

No	Test Item	Condition	Remarks
No	Test Item	Condition	Remarks
1	High Temperature Operation	Ta=+70℃, 120hrs	IEC60068-2-2:2007 GB2423.2-2008
2	Low Temperature Operation	Ta=-20℃, 120hrs	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	Ta=+80℃, 120hrs	IEC60068-2-2:2007 GB2423.2-2008
4	Low Temperature Storage	Ta=-30℃, 120hrs	IEC60068-2-1:2007 GB2423.1-2008
5	High Temperature and Humidity Operation	Ta=+60℃, 90% RH 120hrs hours	IEC60068-2-78 :2012 GB/T2423.3—2016
6	Thermal Shock (non-operation)	-30℃ 30 min~+70℃ 30 min, Change time:5min, 20 Cycles	Start with cold temperature, End with high temperature, IEC60068-2-14:2009 GB 2423.22-2012
7	Electro Static Discharge (Operation)	C=150pF, R=330 ， 5points/panel Air:±4KV, 5times; Contact:±4KV, 5 times; （Environment: 15℃～35℃, 30%～60%, 86Kpa～106Kpa）	IEC61000-4-2:2001 GB/T17626.2-2006

Note1: Ta is the ambient temperature of sample.

Note2: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

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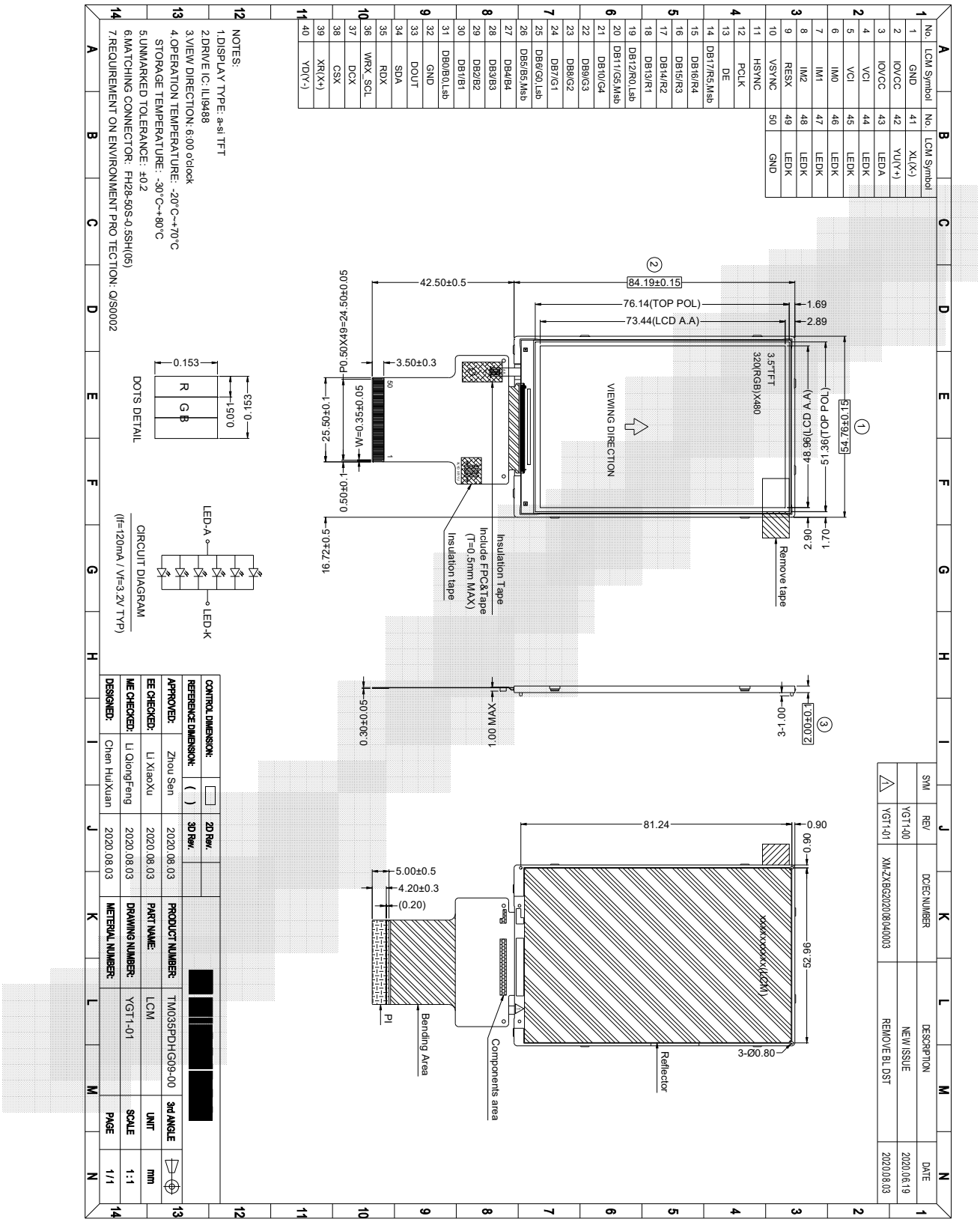
8 Mechanical Drawing



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9 Packing Drawing

Per Carton

No	Item	Model (Materiel)	Dimensions(mm)	Unit Weight(Kg)	Quantity	Remark
1	LCM	TM035PDHG09-00	84.19*54.76*2.00	TBD	144	TM035PDHG09-00
2	Tray	PET	356*256*14.5	TBD	27	1150357260
3	EPE	EPE	196.78*191.54*2	0.002	24	1680370570
4	EPE（珍珠棉1）	MBZ-ZZML1	336*246*6	0.01	6	1680104800
5	EPE（珍珠棉2）	MBZ-ZZM15	375*275*10	0.014	4	1680267110
6	EPE（珍珠棉3）	MBZ-ZZM16	250*280*12	0.015	2	1680267120
7	Carton	QX18A	395*290*315	0.58	1	1680104790
8	ESD bag（防静电真空包装袋）	JD13	400*520	0.042	3	1680213550
9	Total Weight	TBD				

(1) LCM quantity per tray:6
(2) Total LCM quantity per group:48 (8trays×per tray 6 and 1 empty tray)
(3) Total LCM quantity in Carton: Number of PET trays 24× quantity per tray 6 = 144
Note: Please refer to the data from “estimated report about the dimension and stack of Carton ” about stacking carton

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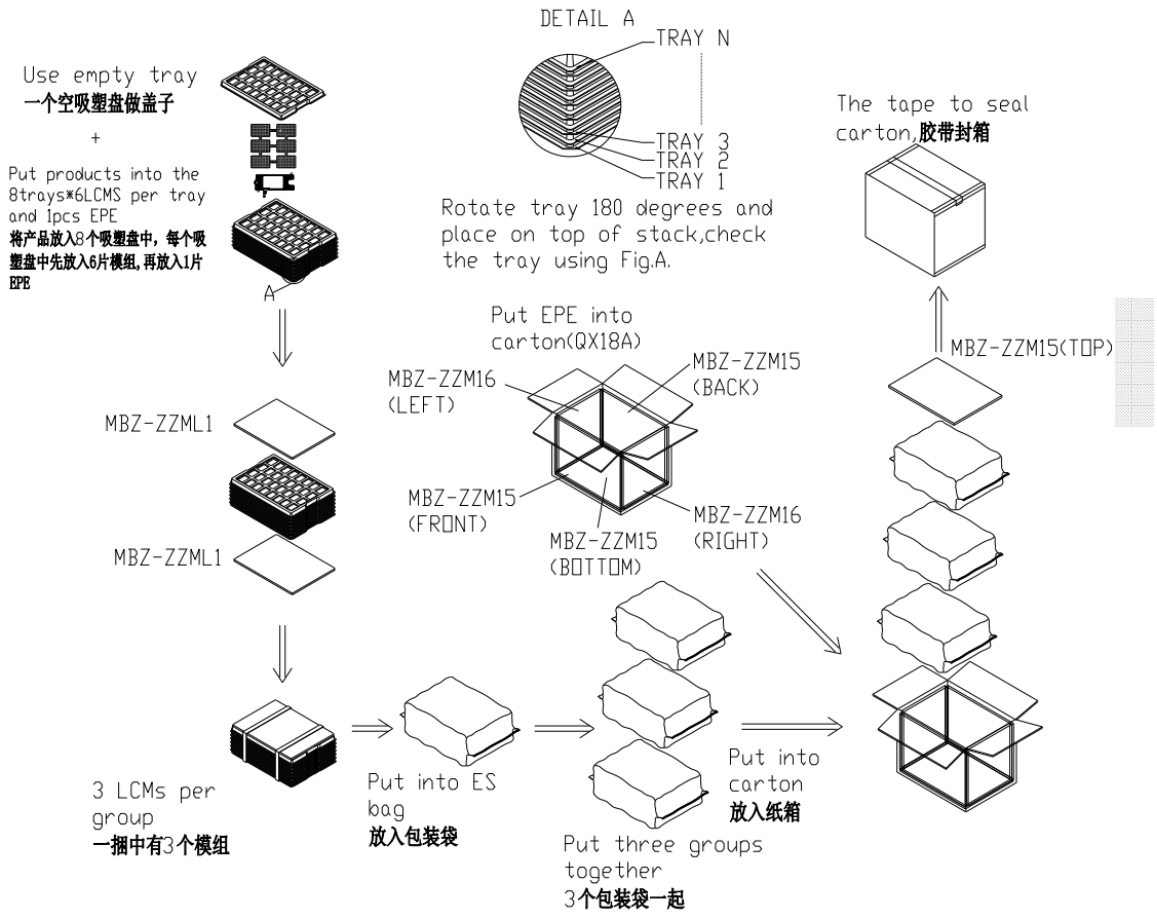

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10 Precautions for Use of LCD Modules

10.6 Handling Precautions

10.6.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.6.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.6.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.6.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.6.5 If the display surface is contaMinated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

10.6.6 Do not attempt to disassemble the LCD Module.

10.6.7 If the logic circuit power is off, do not apply the input signals.

10.6.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1 Be sure to ground the body when handling the LCD Modules.

10.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.7 Storage precautions

10.7.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.7.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

10.7.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.8 Transportation Precautions

10.8.1 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

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