深圳市拓普微科技开发有限公司
SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LMT050FNCFWA

LCD Module User Manual

Prepared by:	Checked by:	Approved by:
Chenzhonghua		
Date: 2024-04-24	Date:	Date:

Rev.	Descriptions	Edit	Release Date
0.1	Preliminary	Chenzhonghua	2024-04-24

Table of Content

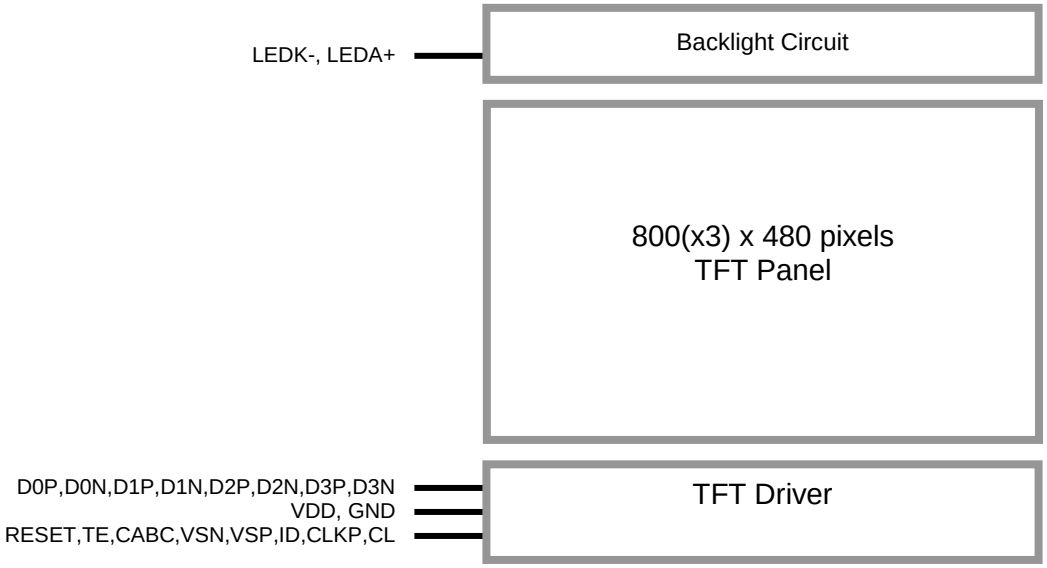
1. General Specification

Screen Size(Diagonal) :	5.0 inch
Resolution :	800(RGB) x 480
Signal Interface :	MIPI
Color Depth :	16.7M color (24bit)
Pixel Pitch :	0.135 x 0.135 (mm)
Pixel Configuration :	RGB Stripe
Display Mode :	Transmissive / normal Black
Surface Treatment :	Clear HC(3H)
Viewing Direction :	Full
Outline Dimension :	136.00x78.81x7.0 (mm) (exclude FPC, see attached drawing for details)
Active Area :	108 x 64.8 (mm)
Backlight :	9 LEDs
Operating Temperature :	-20 ~ +70°C
Storage Temperature :	-30 ~ +80°C

Note:

*1. Color tone may slightly change by Temperature and Driving Condition.

2. Block Diagram



3. Terminal Functions

3.1 Interface

Match connector type CN1: 62684-3211D0ALF

Pin No.	Pin Name	I/O	Descriptions
1	GND	P	Power Ground (0V)
2	GND	P	Power Ground (0V)
3	ID(GND)	O	ID
4	LEDK	P	Backlight LED Cathode supply
5	LEDA	p	Backlight LED Anode supply
6	NC	-	No connection
7	D0N	I	MIPI D0-
8	D0P	I	MIPI D0+
9	GND	P	Power Ground (0V)
10	D1N	I	MIPI D1-
11	D1P	I	MIPI D1+
12	GND	p	Power Ground (0V)
13	CLKN	I	MIPI CLK-
14	CLKP	I	MIPI CLK+
15	GND	P	Power Ground (0V)
16	D2N	I	MIPI D2-
17	D2P	I	MIPI D2+
18	GND	P	Power Ground (0V)
19	D3N	I	MIPI D3-
20	D3P	I	MIPI D3+
21	GND	P	Power Ground (0V)
22	IOVCC	P	Power supply(3.3v)
23	IOVCC	P	Power supply(3.3v)
24	GND	P	Power Ground (0V)
25	VSP	P	Positive Source Power
26	VSN	P	Negative Source Power
27	GND	P	Power Ground (0V)
28	CABC	O	backlight control
29	TE	O	Serves TE (Tearing Effect) pin
30	RESET	I	LCD Reset pin
31	GND	P	Power Ground (0V)
32	GND	P	Power Ground (0V)

Note: I/O Definition

I—Input, O—Output, P—Power/Ground

4. Absolute Maximum Ratings

GND=0V, Ta = 25℃

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	IOVCC	-0.3	+5.5	V	GND = 0V
Supply Voltage	VSP	-0.3	+6.6	V	
Supply Voltage	VSN	0.3	-6.6	V	
Logic Input voltage range	VIN	-0.3	IOVCC+0.3	V	
Logic Output voltage range	VO	-0.3	IOVCC+0.3	V	
Differential Input voltage	HSSI_CLK_P/N, HSSI_DATA0_P/N, HSSI_DATA1_P/N HSSI_DATA2_P/N HSSI_DATA3_P/N	-0.3	1.8	V	
Operating Temperature	T_{OP}	-20	+70	℃	No Condensation
Storage Temperature	T_{ST}	-30	+80	℃	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

5. Electrical Characteristics

5.1 DC Characteristics

IOVCC =3.3V, GND=0V, Ta =25℃

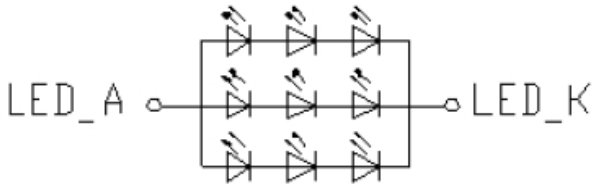
Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Operating Voltage	IOVCC	3.2	3.3	3.4	V	
Operating Voltage	VSP	5.4	5.5	5.6	V	
Operating Voltage	VSN	-5.6	-5.5	-5.4	V	
Input High Voltage	V_{IH}	0.7 IOVCC	-	IOVCC	V	
Input Low Voltage	V_{IL}	GND	-	0.3VDD	V	
Output Signal Low Voltage	V_{oH}	0.8 IOVCC	-	IOVCC	V	
Output Signal High Voltage	V_{OL}	GND	-	0.2 IOVCC	V	
Operating Current (*1)	I_{IOVCC}	-	25	-	mA	white pattern

5.2 LED Backlight Circuit Characteristic

I_{VLED}=60mA, Ta=25℃

Items	Symbol	MIN.	TYP.	MAX.	Unit	Note
Forward Voltage	VLED	8.1	9.0	9.9	V	
Forward Current	I_{VLED}	-	60	-	mA	
Life Time	-	20,000	-	-	hrs	

Cautions:
Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.



LED circuit

6. MIPI DC Characteristics

6.1 DC Characteristics for DSI LP Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-RX, Vin=0~1.3V	-	-	10	μA
Logic low level input current	I_{IL}	LP-RX, Vin=0~1.3V	-10	-	-	μA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	300	Vps

Note 1) VDDI=1.65~3.6V, DVSS=VSSAM=AVSS=VSSB=VSSR=0V, Ta=-30 to 70 ºC (to +85 ºC no damage).
Note 2) DSI high speed is off.
Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

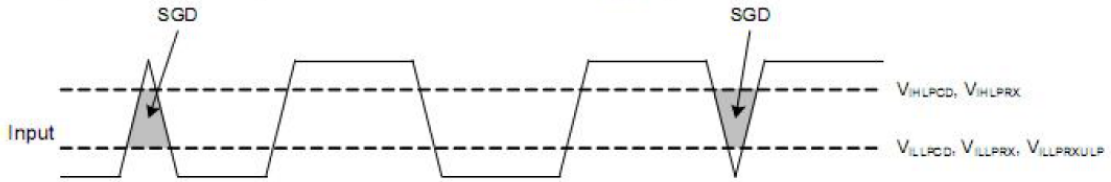


Fig. 7.2.2 Spike/Glitch rejection-DSI

6.2 DC Characteristics for DSI HS Mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	CLKP/N Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DnP/N Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	CLKP/N Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DnP/N Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	CLKP/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DnP/N Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	CLKP/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DnP/N Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	CLKP/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DnP/N Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	CLKP/N, DnP/N Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	CLKP/N, DnP/N Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	CLKP/N, DnP/N Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	CLKP/N, DnP/N Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	CLKP/N, DnP/N Note 5, Note 6	-	-	60	pF

Notes:

1. Ta = -30℃ to 70℃ (to +85℃ no damage) , VCI = 2.5V to 6.6V, VDDI = 1.65V to 3.6V

2. Includes 50mV (-50mV to 50mV) ground difference

3. Without VCMRCLKM450/VCMRDATAM450

4. Without 50mV (-50mV to 50mV) ground difference

5. n = 0 and 1

6. For higher bit rates, a 14pF capacitor will be needed to meet the common-mode return loss specification.

7. AC Characteristics

7.1 MIPI DSI Timing Characteristics

7.1.1 High Speed Mode

(DVSS=VSSAM=AVSS=VSSB=VSSR=0V, VDDI=1.65V to 3.6V, Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	3.32	-	5	ns	4 Lane (Note 2)
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous half ($UI = UI_{INSTA} = UI_{INSTB}$)	1.66	-	2.5	ns	4 Lane (Note 2)
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15xUI	-	-	ps	
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3xUI	ps	

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is 2.4Gbps for 24-bit data format, 1.8Gbps for 18-bit data format and 1.6Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.

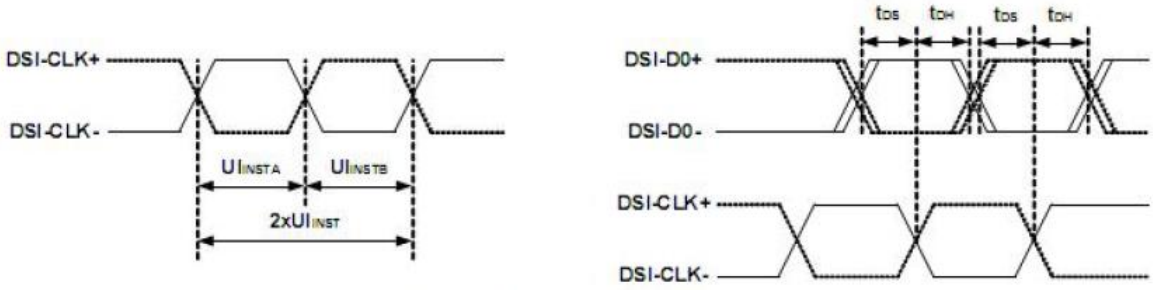


Fig. 7.3.1 DSI clock channel timing

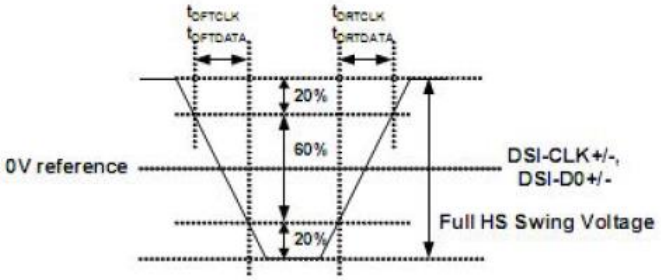


Fig. 7.3.2 Rising and fall time on clock and data channel

7.1.2 Low Power Mode

(DVSS=VSSAM=AVSS=VSSB=VSSR=0V, VDDI=1.65V to 3.6V, Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	-	$5xT_{LPXD}$	-	ns	Input
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	-	$4xT_{LPXD}$	-	ns	Output

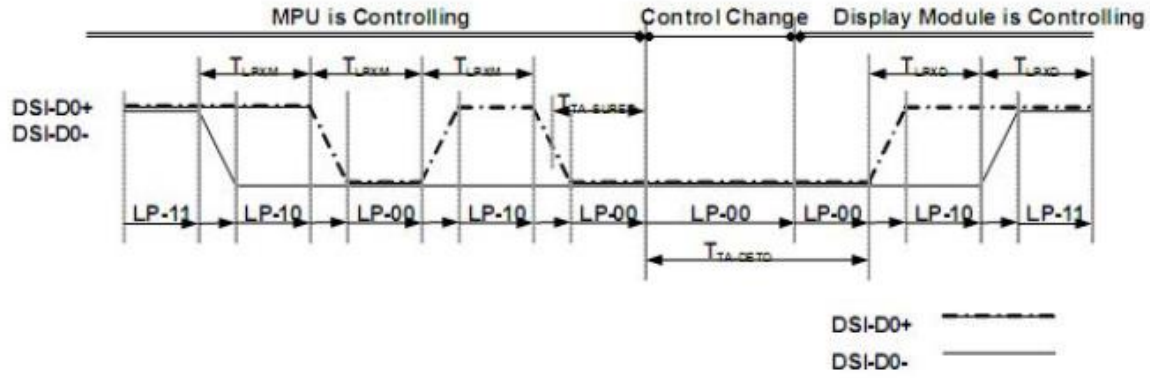


Fig. 7.3.3 Bus Turnaround (BTA) from MPU to display module Timing

Fig. 7.3.3 Bus Turnaround (BTA) from MPU to display module Timing

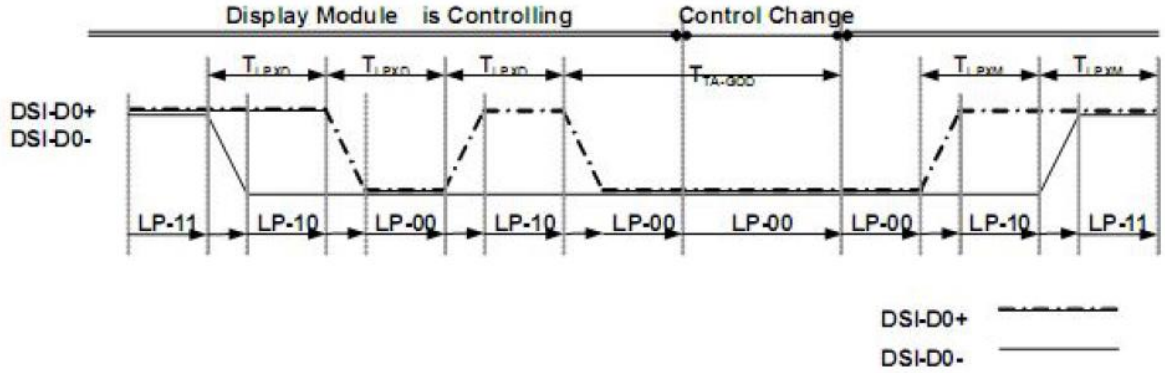


Fig. 7.3.4 Bus Turnaround (BTA) from display module to MPU Timing

7.1.3 DSI Bursts

(DVSS=VSSAM=AVSS=VSSB=VSSR=0V, VDDI=1.65V to 3.6V, Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	T_{LPX}	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	$T_{HS-TERM-EN}$	Time to enable data receiver line termination measured from when Dn crosses V_{ILMAX}	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	$T_{CLK-POS}$	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as $T_{HS-EXIT}$ from each other in continuous clock mode. In discontinuous mode, the break is longer which account $T_{CLK-POS}$, $T_{CLK-TRAIL}$ and $T_{HS-EXIT}$, before activity in clock and data lanes again.

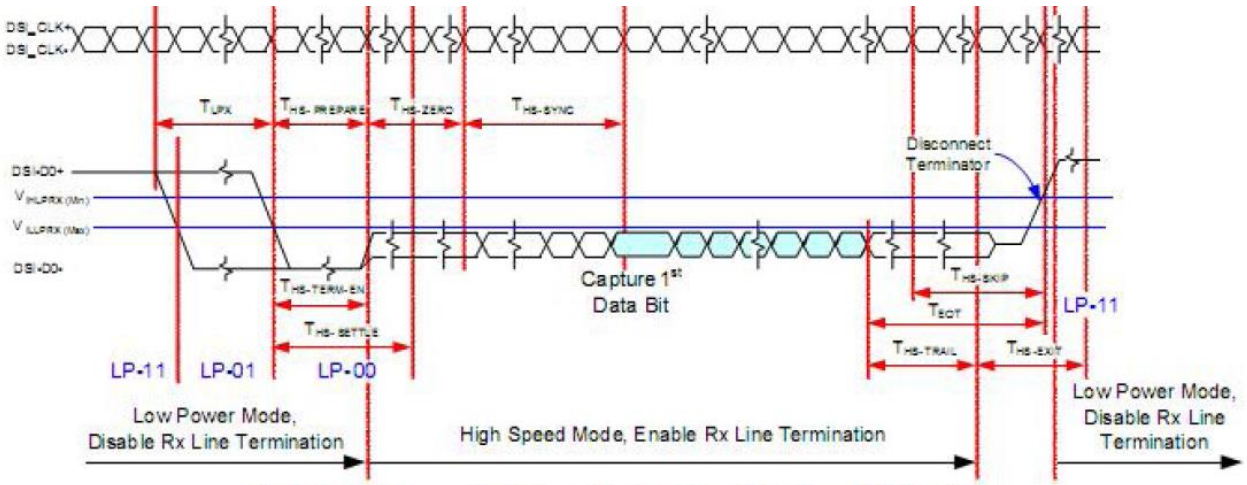


Fig. 7.3.5 Data lanes-Low Power Mode to/from High Speed Mode Timing

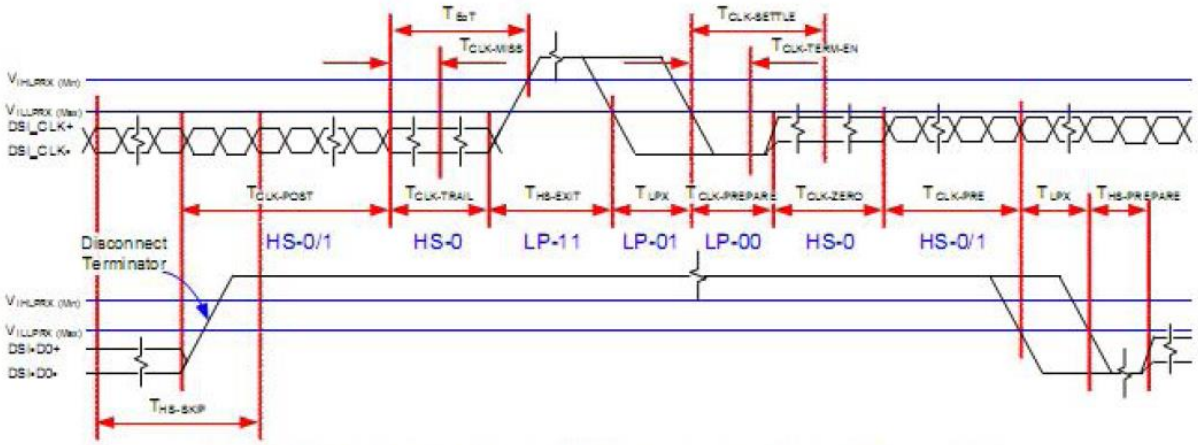


Fig. 7.3.6 Clock lanes- High Speed Mode to/from Low Power Mode Timing

7.2 Reset Input Timing

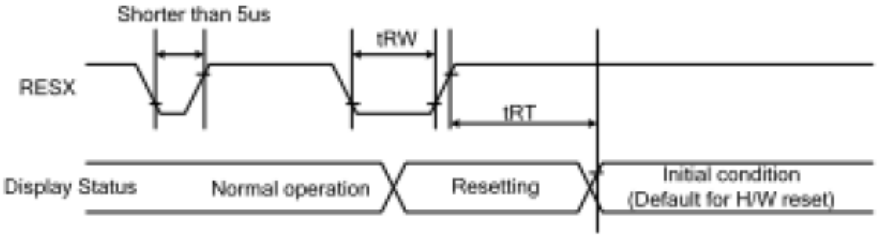


Figure 124: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

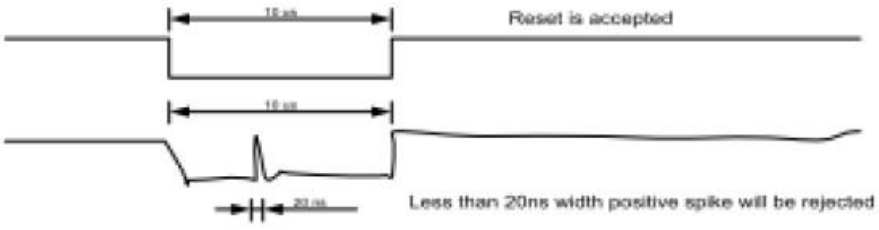


Figure 125: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.3 Deep Standby Mode Timing

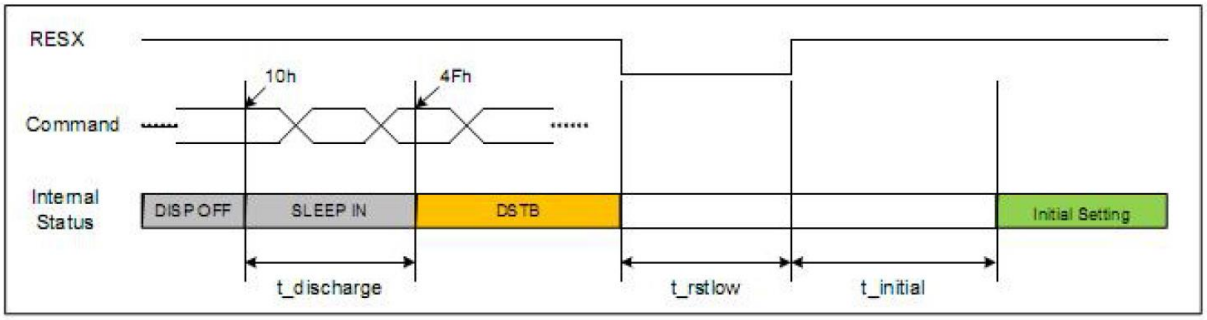


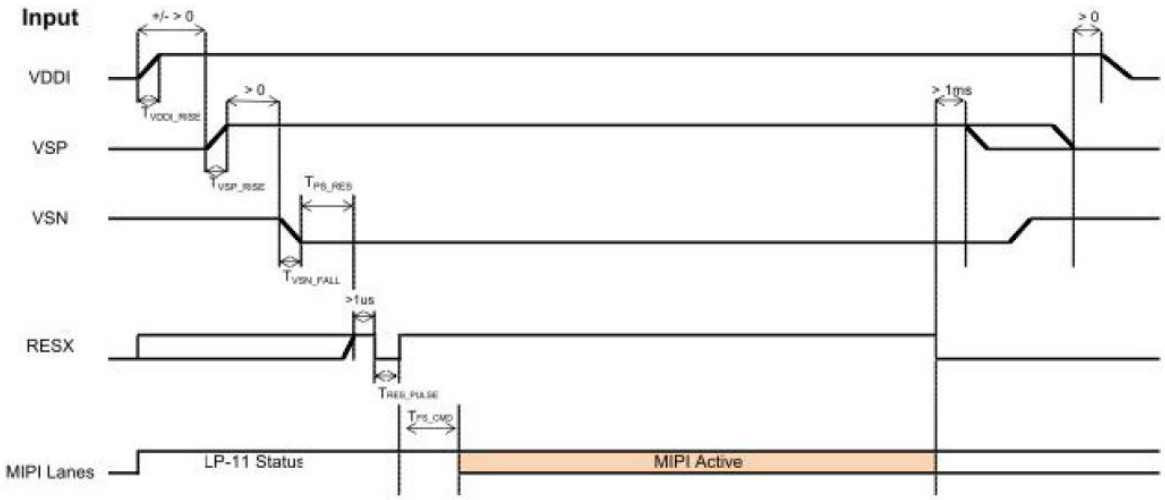
Fig. 7.3.8 Deep standby timing

(DVSS=VSSAM=AVSS=VSSB=VSSR=0V, VDDI=1.65V to 3.6V, Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	$t_{discharge}$	Sleep in into DSTB delay time	100	-	-	ms	
	t_{rstlow}	Reset low pulse	3	-	-	ms	
	$t_{initial}$	Reset high to initial setting delay time	120	-	-	ms	

Note 1) $t_{discharge}$ suggested delay time over 100ms.
Note 2) $t_{initial}$ suggested delay time over 120ms..

8. Power On/Off Sequence



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VSP_RISE}	VSP Rise time	130	-	-	us
T_{VSN_FALL}	VSN Fall time	200	-	-	us
T_{PS_RES}	VDDI/VSP on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Figure 104: Power on/off sequence with Power Mode 2A

9. Optical Characteristics

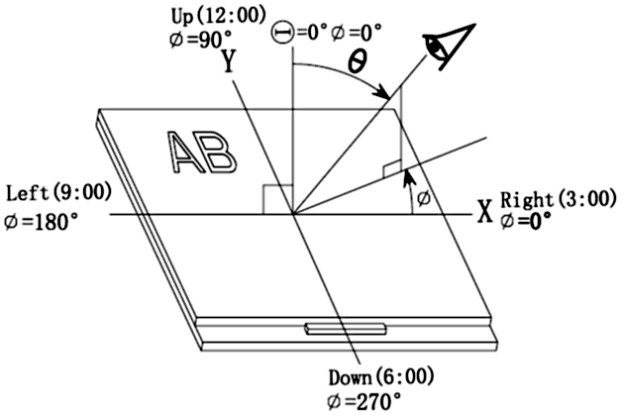
Ta=25℃

Item		Symbol	Condition	MIN.	TYP.	MAX.	UNIT	Note.
Viewing angle		θ_T	(CR≥10)	70	80	-	degree	Note 2
		θ_B		70	80	-		
		θ_L		70	80	-		
		θ_R		70	80	-		
Contrast ratio		CR	θ=0°	500	600	-	-	Note 1,3
Response Time		T_{on}	25℃	-	20	30	msec	Note 1,4
		T_{off}					msec	
Chromaticlty	White	X	Backlight is on	0.259	0.309	0.359		Note 1,5
		Y		0.271	0.321	0.371		
	Red	X		0.541	0.591	0.641		
		Y		0.302	0.352	0.402		
	Green	X		0.296	0.346	0.396		
		Y		0.529	0.579	0.629		
	Blue	X		0.101	0.151	0.201		
		Y		0.040	0.090	0.140		
Luminance		L		260	350	-	cd/m^2	Note 1,6
NTSC				-	50		%	Note 5
Luminance uniformity		U		75	80	-	%	Note 1,7
Gamma				-	2.2	-		

Test Conditions:
1. $I_{\_VLED}$= 60mA, VLED=9.0V, and the ambient temperature is 25. ℃
2. The test systems refer to Note 1 and Note 2.

Note 1:
The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment SR-3A (1°)
Measuring condition:
- Measuring surroundings: Dark room
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

Note 2:
The definition of viewing angle:
Refer to the graph below marked by θ and Φ

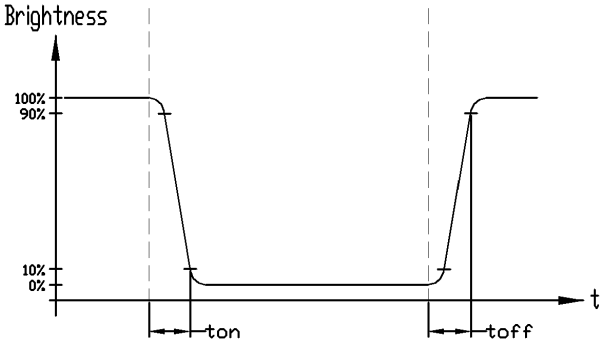


Note 3:
The definition of contrast ratio (Test LCM using SR-3A (1°)):

$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance When LCD is at "White" state}}{\text{Luminance When LCD is at "Black" state}}$$

(Contrast Ratio is measured in optimum common electrode voltage)

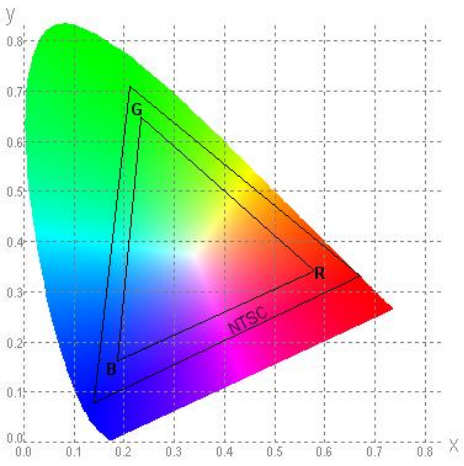
Note 4:
Definition of Response time. (Test LCD using BM-7A(2°)):
The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively.
The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



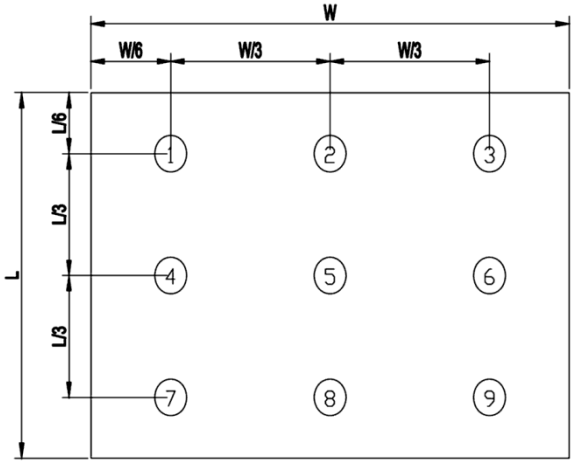
Note 5:
Definition of Color of CIE1931 Coordinate and NTSC Ratio.

Color gamut:

$$S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$



Note 6:
The luminance uniformity is calculated by using following formula.
△Bp = Bp (Min.) / Bp (Max.)×100 (%)
Bp (Max.) = Maximum brightness in 9 measured spots
Bp (Min.) = Minimum brightness in 9 measured spots.



Note 7:
Measured the luminance of white state at center point

Warranty

LCD Module Design and Handling Precaution

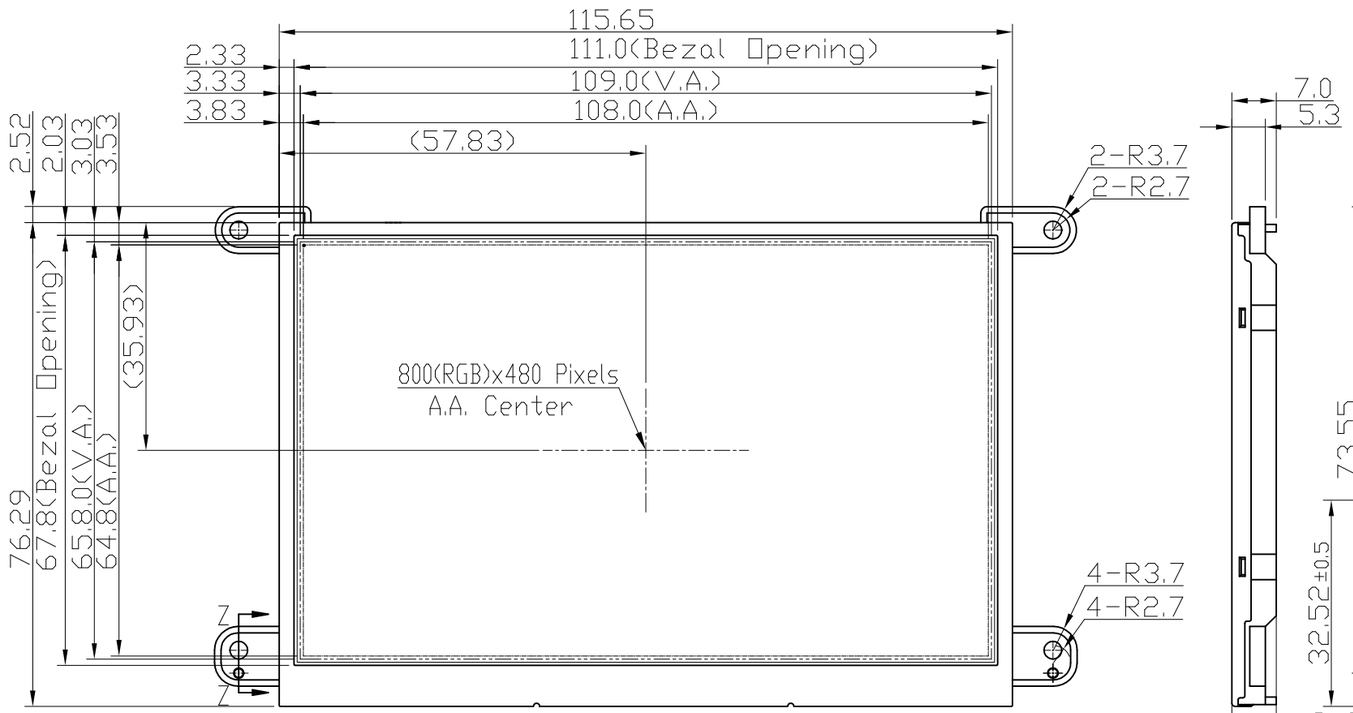
- Please ensure V0, VCOM is adjustable, to enable LCD module get the best contrast ratio under different temperatures, view angles and positions.
- Normally display quality should be judged under the best contrast ratio within viewable area. Unexpected display pattern may com out under abnormal contrast ratio.
- Never operate the LCD module exceed the absolute maximum ratings.
- Never apply signal to the LCD module without power supply. （No Hot-plugging）
- WARNING! Be aware of (if any) frame grounding of the LCD Module connection with the system which may cause safety issue(e.g. electric shock,etc).
- Keep signal line as short as possible to reduce external noise interference.
- IC chip (e.g. TAB or COG) is sensitive to light. Strong light might cause malfunction. Light sealing structure casing is recommended.
- Make sure there is enough space (with cushion) between case and LCD panel, to prevent external force passed on to the panel; otherwise that may cause damage to the LCD and degrade its display result.
- Avoid showing a display pattern on screen for a long time (continuous ON segment).
- LCD module reliability may be reduced by temperature shock.
- When storing and operating LCD module, avoids exposure to direct sunlight, high humidity, high or low temperature. They may damage or degrade the LCD module.
- Never leave LCD module in extreme condition (max./min storage/operate temperature) for more than 48hr.
- Recommend LCD module storage conditions is 0℃~40℃ <80%RH.
- LCD module should be stored in the room without acid, alkali and harmful gas.
- Avoid dropping & violent shocking during transportation, and no excessive pressure press, moisture and sunlight.
- LCD module can be easily damaged by static electricity. Please maintain an optimum anti-static working environment to protect the LCD module. (eg. ground the soldering irons properly)
- Be sure to ground the body when handling LCD module.
- Only hold LCD module by its sides. Never hold LCD module by applying force on the heat seal or TAB.
- When soldering, control the temperature and duration avoid damaging the backlight guide or diffuser which might degrade the display result such as uneven display.
- Never let LCD module contact with corrosive liquids, which might cause damage to the backlight guide or the electric circuit of LCD module.
- Only clean LCD with a soft dry cloth, Isopropyl Alcohol or Ethyl Alcohol. Other solvents (e.g. water) may damage the LCD.
- Never add force to components of LCD module. It may cause invisible damage or degrade the module's reliability.
- When mounting LCD module, please make sure it is free from twisting, warping and bending.
- Do not add excessive force on surface of LCD, which may cause the display color change abnormally.
- LCD panel is made with glass. Any mechanical shock (e.g.

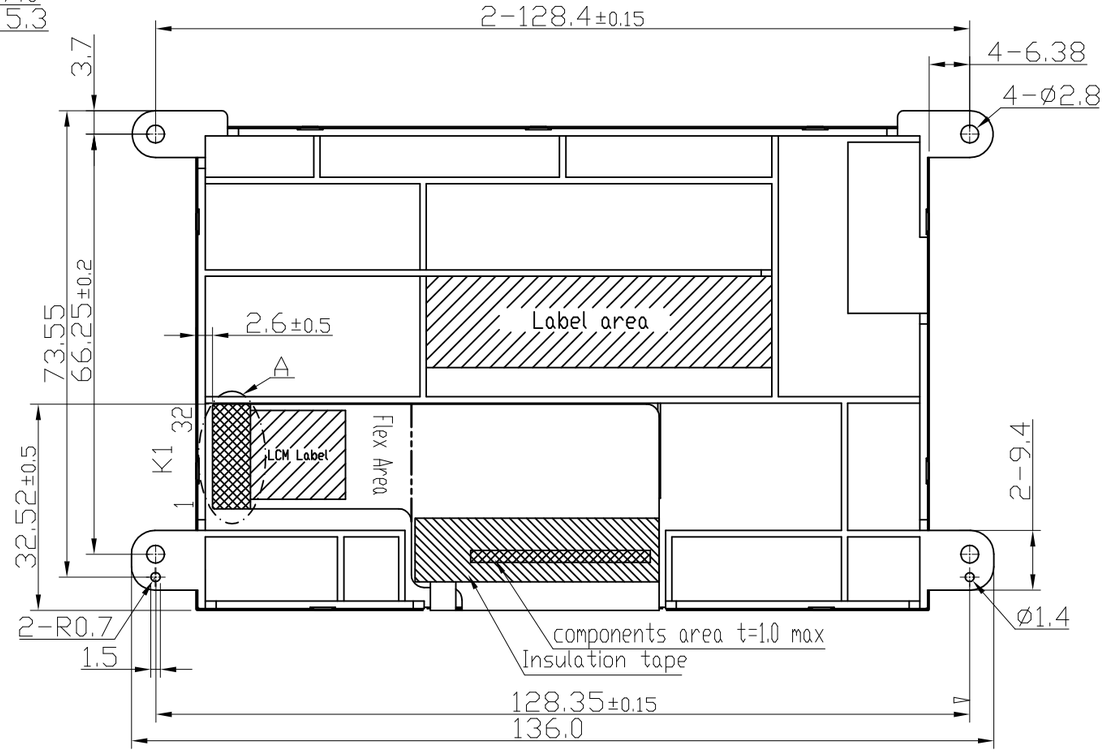
液晶显示模块设计和使用须知

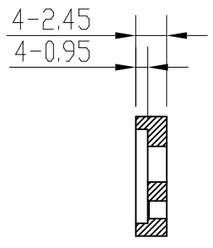
- 请注意 V0, VCOM 的设定，以确保液晶显示模块在不同的使用温度下以及在不同的视角和位置观察模块显示，均能达到最佳对比度，请务必将应用电路上设置为对比度可调。
- 请注意液晶显示模块的显示品质判定是指在正常对比度下以及视窗(V.A)范围内进行的，非正常对比度下液晶可能会出现非预期的显示不良，应注意区分。
- 请勿在最大额定值以外使用液晶显示模块。
- 请勿在没有接通电源的条件下，给液晶显示模块输送信号。（禁止热插拔）
- 警告！使用前需评估液晶显示模块的金属框架/壳体地(如有)与整机关系和安全性(如：漏电安全性，等)。
- 请尽可能缩短信号线的连接，以避免对液晶显示模块的信号干扰。
- 集成电路因 IC 芯片(如 TAB 或 COG)对紫外线极为敏感，强光环境下可能会引起液晶显示模块功能失效，故应采用不透光的外壳。
- 请在液晶显示模块与外壳之间保留足够的空间(可使用衬垫)，以缓冲外力对液晶显示模块的损坏或因受力不均而产生的显示不匀等异常现象。
- 避免液晶显示屏在某一画面下长时间点亮，否则有出现残影的风险；请通过软件每隔一段时间改变一次画面。
- 液晶显示模块的可靠性可能因温度冲击而降低。
- 请勿在阳光直射、高湿、高温或低温下储存和使用液晶显示模块，这将造成液晶显示模块的损坏或失效。
- 请勿在极限环境(最大/最小存储/工作温度)下使用或放置液晶显示模块超过 48 小时以上。
- 液晶显示模块建议存储条件为：0℃~40℃ <80%RH。
- 请勿让液晶显示模块存储于带有 酸性，碱性，有害气体环境之中。
- 在运输过程中，请勿让液晶显示模块跌落与猛烈震动，同时避免 异常挤压，高湿度，与 阳光照射
- 液晶显示模块极易受静电损坏，请务必保证液晶显示模块在防静电的工作环境中使用或保存。(如：烙铁正确接地,等)
- 拿取液晶显示模块时需注意操作人员的接地情况。
- 请手持液晶显示模块的边沿取放模块，防止热压纸或 TAB 部位受力。
- 焊接液晶模块时，请注意控制烙铁的温度、焊接时间，以免烫坏导光板或偏光片，导致显示不匀等不良现象发生。
- 请勿使用洗板水等腐蚀性液体接触液晶模块，以免腐蚀导光板或模块电路。
- 仅可使用柔软的干布，异丙醇或乙醇清洁液晶屏表面，其他任何溶剂(如:水)都有可能损坏液晶模块。
- 请勿挤压液晶显示模块上的元器件，以避免产生潜在的损坏或失效而影响产品可靠性。
- 装配液晶显示模块时，请务必注意避免液晶显示模块的扭曲或变形。
- 请勿挤压液晶显示屏表面，这将导致显示颜色的异常。
- 液晶屏由玻璃制作而成，任何机械碰撞(如从高处跌落)

dropping from high place) will damage the LCD module.
- Protective film is attached on LCD screen. Be careful when peeling off this protective film, since static electricity may be generated.
- Polarizer on LCD gets scratched easily. If possible, do not remove LCD protective film until the last step of installation.
- When peeling off protective film from LCD, static charge may cause abnormal display pattern. The symptom is normal, and it will turn back to normal in a short while.
- LCD panel has sharp edges, please handle with care.
- Never attempt to disassemble or rework LCD module.
- If display panel is damaged and liquid crystal substance leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes promptly wash it off using soap and water.

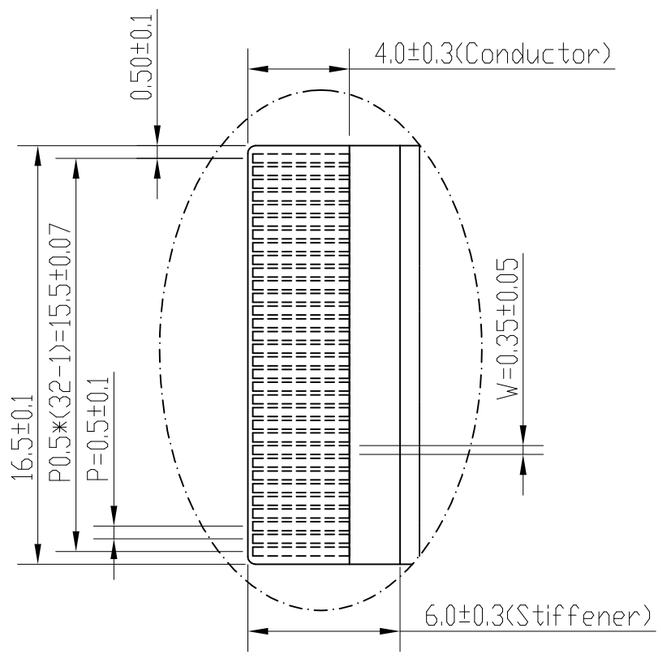
均有可能损坏液晶显示模块。
- 液晶屏表面带有保护膜，揭除保护膜时需要注意可能产生的静电。
- 因液晶显示屏表面的偏光片极易划伤，安装完成之前请尽量不要揭下保护膜。
- 请缓慢揭除保护膜，在此过程中液晶显示屏上可能会产生静电线，此为正常情况，可在短时间内消失。
- 请注意避免被液晶显示屏的边缘割伤。
- 请不要试图拆卸或改造液晶显示模块。
- 当液晶显示屏出现破裂，内部液晶液体可能流出；相关液体不可吞吃，绝对不可接触嘴巴，如接触到皮肤或衣服，请使用肥皂与清水彻底清洗.







Section Z-Z
Scale 2:1



Detail A
Scale=4:1

Note:
*1. LCD Display Type : TFT,Transmissive
*2. Pixel Arrangment : RGB-STRIPE
*3. Interface : MIPI
*4. Color Depth : 16.7M color
*5. Operating Voltage : 3.3V
*6. Backlight Supply : 60mA (Constant Current VF=9.0V typ.)
*7. Backlight : White LED
*8. Matched Connector: 62684-3211D0ALF Or Equivalent
*9. Operating Temperature : -20°C~70°C
*10. Storage Temperature : -30°C~80°C
*11. Unmarked Tolerace : ≤150,±0.3; >150,±0.5

	K1 Terminal		
No	Pin Name	No	Pin Name
17	D2P	1	GND
18	GND	2	GND
19	D3N	3	ID(GND)
20	D3P	4	LEDK
21	GND	5	LEDA
22	IOVCC	6	NC
23	IOVCC	7	DON
24	GND	8	DOP
25	VSP	9	GND
26	VSN	10	D1N
27	GND	11	D1P
28	CABC	12	GND
29	TE	13	CLKN
30	RESET	14	CLKP
31	GND	15	GND
32	GND	16	D2N

C		
B		
A		
Rev	Note	Date

Dwg Title: LMT050FNCFWA outline Dwg
Dwg No.: MK-008449-1-1
Date: 2024-04-24
Scale: 1/1 | Tol. | Unit: mm | Paper Size: A3
Approved | Checked | Drawn: Zhangwenbo

TOPWAY