



深圳市拓普微科技开发有限公司

SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LM12896HCW

LCD Module User Manual

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Rev.	Descriptions	Edit	Release Date
0.1	Preliminary release	Wangxiao	2025-04-18
0.2	Update 3.1DC Characteristics	Wangxiao	2025-06-30

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1. Basic Specifications

1.1 Display Specifications

- | | |
|---------------------|---|
| 1) LCD Display Mode | : FSTN, Positive, Transflective |
| 2) Display Color | : Display Data = "1" : Dark Gray (*1)
: Display Data = "0" : Light Gray (*2) |
| 3) Viewing Angle | : 6 H |
| 4) Driving Method | : 1/96 duty, 1/10bias |
| 5) Back Light | : White LED backlight |

Note:

*1. Color tone may slightly change by Temperature and Driving Condition.

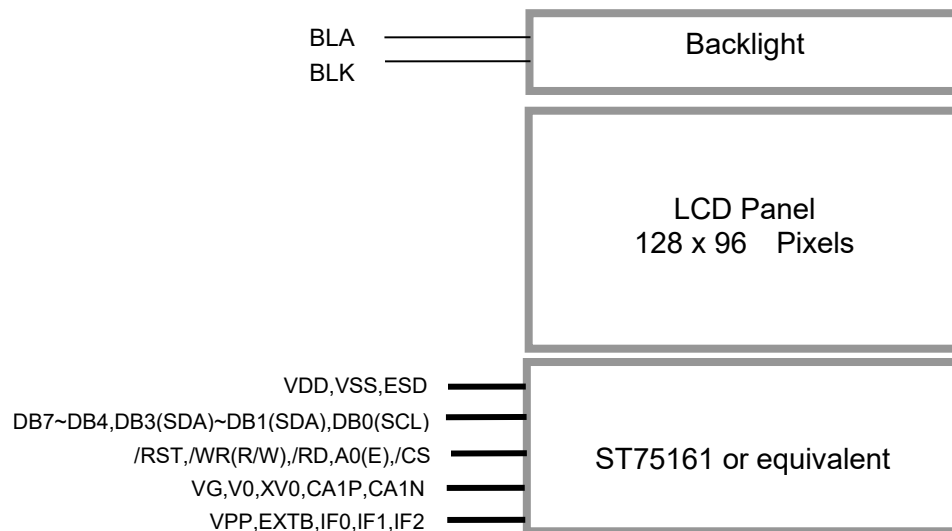
*2. The Color is defined as the inactive / background color.

*3. Fine Contrast adjustment function is necessary in application design for optimal display result.

1.2 Mechanical Specifications

- | | |
|----------------------|--|
| 1) Outline Dimension | : 63.2 x 43.5 x 6.25(mm)(exclude FPC terminal)
(see attached Outline Drawing for details) |
|----------------------|--|

1.3 Block Diagram



1.4 Terminal Functions

Pin No.	Pin Name	I/O	Descriptions			
			8080 mode	6800 mode	4-line SPI	3-line SPI
1	ESD	P	Connect to ground to boost ESD			
2	VPP	-	The programming power supply of the built-in OTP if no used,leave open			
3	NC	-	-			
4	EXTB	-	When programming OTP, connect EXTB to VSS externally if no used,leave open			
5	DB7	I/O	8 bit bi-directional data bus		No used,fix to H by VDD	
6	DB6	I/O				
7	DB5	I/O				
8	DB4	I/O				
9	DB3(SDA)	I/O			Serial input/output data, DB3(SDA)~DB1(SDA) must be connected together	
10	DB2(SDA)	I/O				
11	DB1(SDA)	I/O				
12	DB0(SCL)	I/O			Serial input clock	
13	/RST	I	Reset signal. /RST = L, internal Initialization is executed /RST = H, Normal running			
14	/WR(R/W)	I	WR=L→H, /RD=H; Data or Instruction latch into the LCD module	R/W = H, E=L; Data or Status read form the LCD module	No used,fix to H by VDD	
15	/RD(E)	I	WR=H, /RD=L; Data or Status read form the LCD module	R/W=L, E= H→L; Data or Instruction latch into the LCD module	No used,fix to H by VDD	
16	A0	I	Register Select A0 = H, Transferring the Display Data A0 = L, Transferring the Control Data			No used, fix to H by VDD
17	/CS	I	Chip select input pin /CS= “L” : This chip is selected and the MPU interface is active /CS= “H” : This chip is not selected and the MPU interface is disabled			
18	IF0	I	These pins select interface operation mode			
19	IF1	I	IF2	IF1	IF0	Interface Type
			L	H	H	8080 mode
20	IF2	I	L	H	L	6800 mode
			L	L	L	4-line SPI
			H	L	L	3-line SPI
21	VSS	P	Negative Power Supply, Ground (0V)			
22	VDD	P	Positive Power Supply			
23	CA1N	P	DC/DC voltage converter			
24	CA1P	P	Connect a capacitor between CA1P and CA1N			
25	XV0	P	Negative operating voltage of COM-drivers			
26	V0	P	Positive operating voltage of COM-drivers			
27	VG	P	VG is the power of SEG-drivers			
28	ESD	P	Connect to ground to boost ESD			
29	BLA	P	Positive Power for LED backlight			
30	BLK	P	Negative Power for LED backlight			

Note:

*1.I—Input, O—Output, P—Power/Ground.

2.Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	-0.3	4.0	V	$V_{SS} = 0V$
Operating Temperature	T_{OP}	-40	70	°C	No Condensation
Storage Temperature	T_{ST}	-40	80	°C	No Condensation

Cautions:

Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

3.Electrical Characteristics

3.1 DC Characteristics

$V_{SS} = 0V$, $V_{DD} = 3.3V$, $T_{OP} = 25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Operating Voltage	V_{DD}	3.0	3.3	3.6	V	VDD
Input High Voltage	V_{IH}	$0.7V_{DD}$	-	V_{DD}	V	DB7~DB4,DB3(SDA)~DB1(SDA),DB0(SCL),/RST,/WR(R/W),/RD(E),A0,/CS
Input Low Voltage	V_{IL}	V_{SS}	-	$0.3V_{DD}$	V	
Output High Voltage	V_{OH}	$0.8V_{DD}$	-	V_{DD}	V	
Output Low Voltage	V_{OL}	V_{SS}	-	$0.2V_{DD}$	V	
Operating Current	I_{DD}	-	1	-	mA	VDD

3.2 LED Backlight Circuit Characteristics

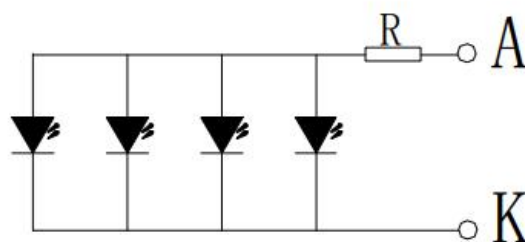
$V_{SS} = 0V$, $BLA = 3.3V$, $T_{OP} = 25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Forward Voltage	V_{BLA}	-	3.3	-	V	BLA
Forward Current	I_{BLA}	-	-	60	mA	BLA

Cautions:

Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.

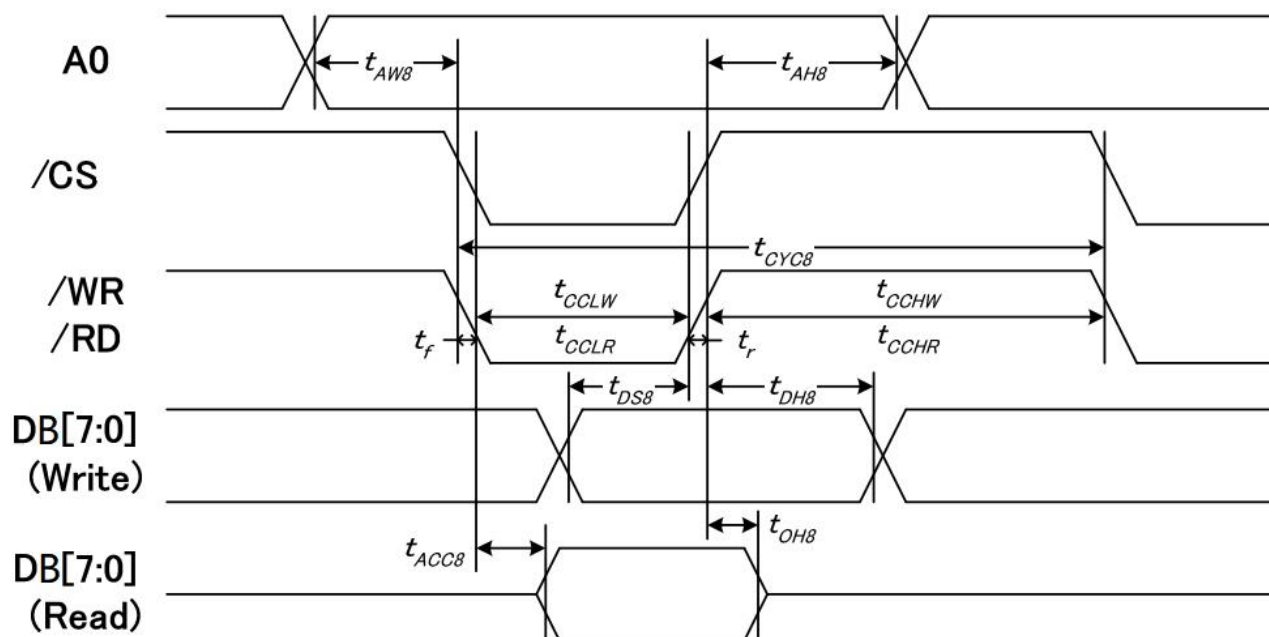
CIRCUIT DIAGRAM:



Backlight:WHITE LED(4)

3.3 AC Characteristics

3.3.1 8080 Interface Characteristics



8080 Interface Timing Diagram

$V_{SS} = 0V$, $V_{DD} = 3.3V$, $T_{OP} = 25^{\circ}C$

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address Setup Time	t_{AW8}		26	-	-	ns
Address Hold Time	t_{AH8}		0	-	-	ns
System cycle time(WRITE)	t_{CYC8}		208	-	-	ns
/WR L pulse width(WRITE)	t_{CCLW}		91	-	-	ns
/WR H pulsewidth(WRITE)	t_{CCHW}		91	-	-	ns
System cycle time (READ)	t_{CYC8}		520	-	-	ns
/RD L pulse width (READ)	t_{CCLR}		234	-	-	ns
/RD H pulse width (READ)	t_{CCHR}		234	-	-	ns
WRITE Data setup time	t_{DS8}		19.5	-	-	ns
WRITE Data hold time	t_{DH8}		19.5	-	-	ns
READ access time	t_{ACC8}	CL	-		130	ns
READ Output disable time	t_{OH8}	CL	13		77	ns

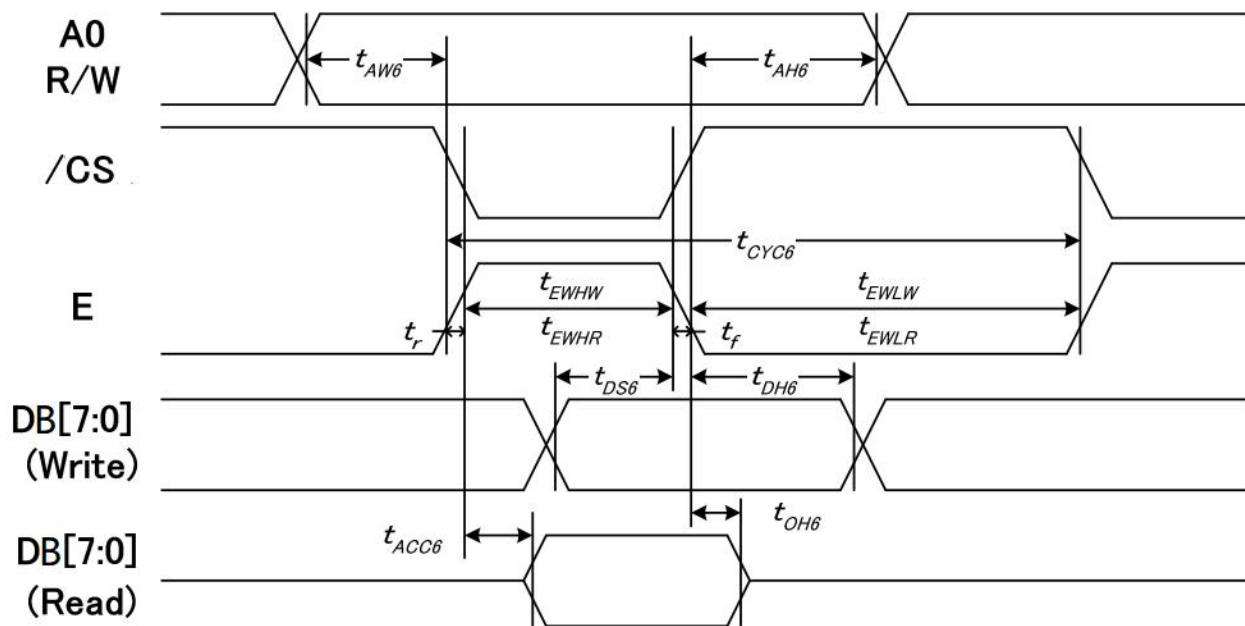
Note:

*1. Input signal rise/fall time should be less than 15ns.

*2. CL=30pF.

*3.All timing is using 20% and 80% of VDD as the reference.

3.3.2 6800 Interface Characteristics



6800 Interface Timing Diagram

 $V_{SS} = 0V, V_{DD} = 3.3V, T_{OP} = 25^{\circ}C$

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address Setup Time	t_{AW6}		26	-	-	ns
Address Hold Time	t_{AH6}		0	-	-	ns
System cycle time(WRITE)	t_{CYC6}		208	-	-	ns
Enable L pulse width(WRITE)	t_{EHLW}		91	-	-	ns
Enable H pulse width(WRITE)	t_{EHLR}		91	-	-	ns
System cycle time (READ)	t_{CYC6}		520	-	-	ns
Enable L pulse width (READ)	t_{EHLR}		234	-	-	ns
Enable H pulse width (READ)	t_{EHLR}		234	-	-	ns
Write data setup time	t_{DS6}		19.5	-	-	ns
Write data hold time	t_{DH6}		19.5	-	-	ns
Read data access time	t_{ACC6}	CL	-		130	ns
Read data output disable time	t_{OH6}	CL	13		77	ns

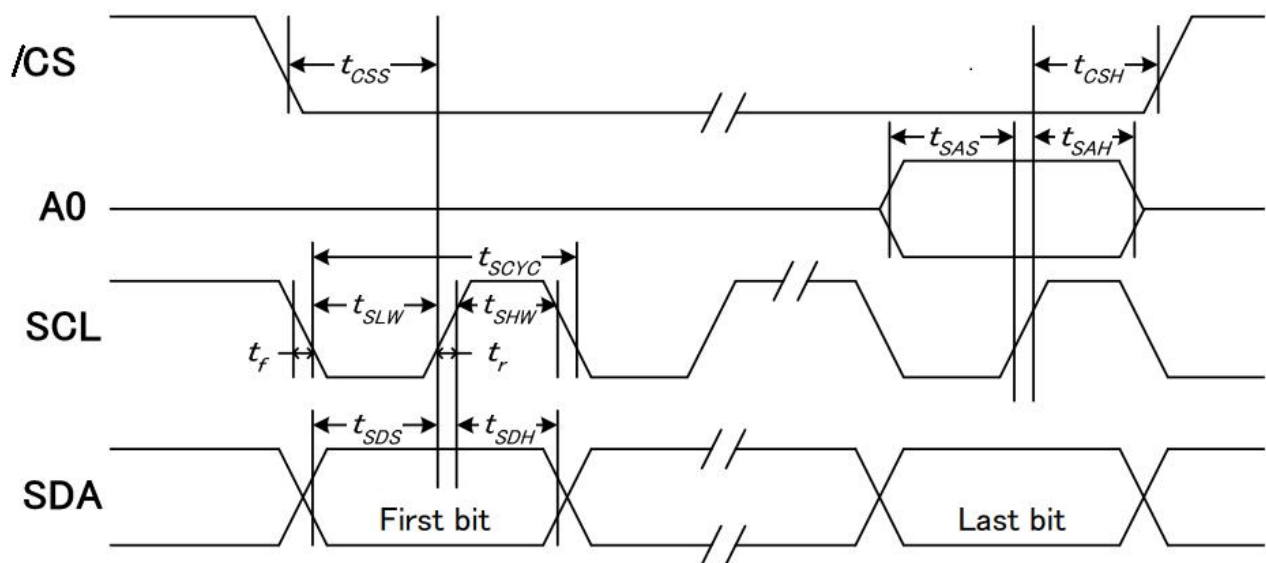
Note:

*1. Input signal rise/fall time should be less than 15ns.

*2. CL=30pF.

*3.All timing is using 20% and 80% of VDD as the reference.

3.3.3 4-Line SPI MCU Interface Characteristics



4-Line SPI Interface Timing Diagram

 $V_{SS} = 0V, V_{DD} = 3.3V, T_{OP} = 25^{\circ}C$

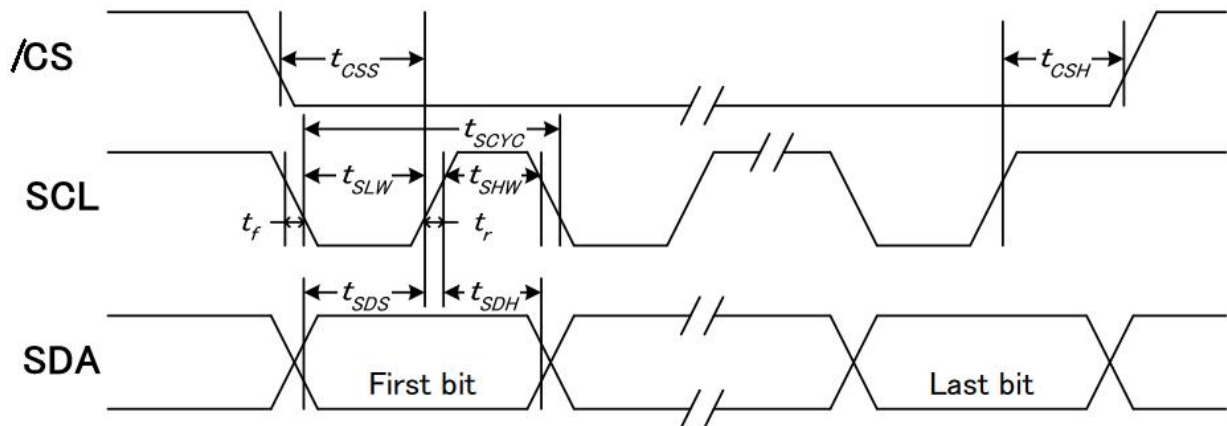
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Serial clock period	t_{SCYC}		104	-	-	ns
SCLK "H" pulse width	t_{SHW}		39	-	-	ns
SCLK "L" pulse width	t_{SLW}		39	-	-	ns
Address setup time	t_{SAS}		26	-	-	ns
Address hold time	t_{SAH}		26	-	-	ns
Data setup time	t_{SDS}		26	-	-	ns
Data hold time	t_{SDH}		26	-	-	ns
/CS-SCLK time	t_{CSS}		26	-	-	ns
/CS-SCLK time	t_{CSH}		26	-	-	ns
/CS "H" pulse width	t_{CHW}		0	-	-	ns

Note:

*1. Input signal rise/fall time should be less than 15ns.

*2. All timing is using 20% and 80% of VDD as the reference.

3.3.4 3-Line SPI MCU Interface Characteristics



3-Line SPI Interface Timing Diagram

$V_{SS} = 0V, V_{DD} = 3.3V, T_{OP} = 25^{\circ}C$

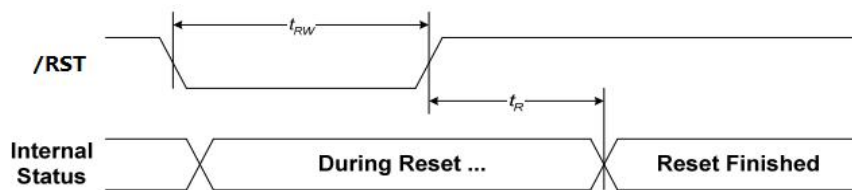
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Serial clock period	t_{SCYC}		104	-	-	ns
SCLK "H" pulse width	t_{SHW}		39	-	-	ns
SCLK "L" pulse width	t_{SLW}		39	-	-	ns
Data setup time	t_{SDS}		26	-	-	ns
Data hold time	t_{SDH}		26	-	-	ns
/CS-SCLK time	t_{CSS}		26	-	-	ns
/CS-SCLK time	t_{CSH}		26	-	-	ns

Note:

*1. Input signal rise/fall time should be less than 15ns.

*2. All timing is using 20% and 80% of V_{DD} as the reference.

3.3.5 Reset Timing



Reset Timing Diagram

$V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25^{\circ}C$

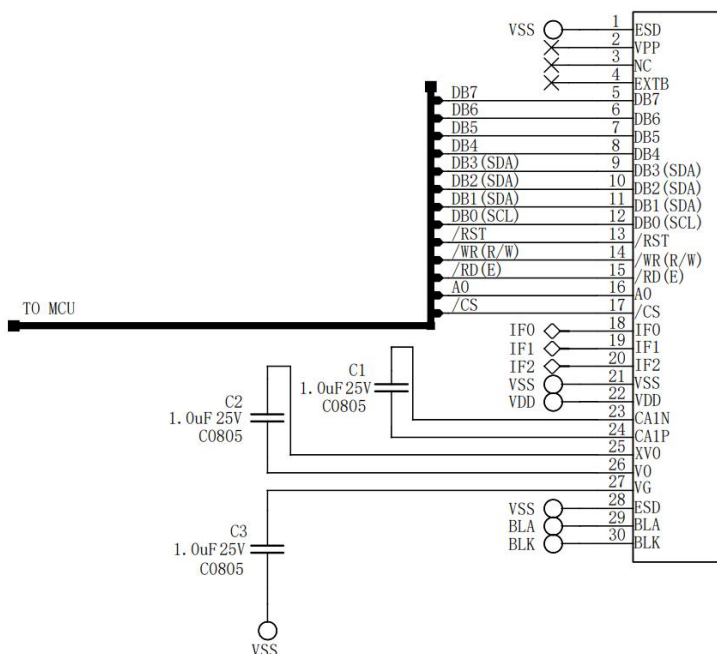
Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset time	t_R	-	-	1	ms
Reset "L" pulse width	t_{RW}	1	-	-	ms

4. Function Specifications

4.1 Adjusting the Display Contrast

- This LCD module equipped with latest digital contrast adjustment function.
- Its display contrast could be adjusted by MCU command. (please see the command tables for details)
- It is recommended to provide a contrast adjustment interface for end-user, where the best display result could meet the individual preference in mass production.

4.2 Application circuit(Example)



Note:

Please refer to the ST75161 data sheet for details

4.3 Resetting the LCD module

The LCD module should be initialized by using /RES terminal.

While turning on the VDD and VSS power supply, maintain /RES terminal at LOW level. After the power supply stabilized, release the reset terminal (/RES=HIGH)

4.4 Power off the LCD Module

It recommends that LCD module should enter sleep mode before power off.

4.5 Refreshing The LCD Module

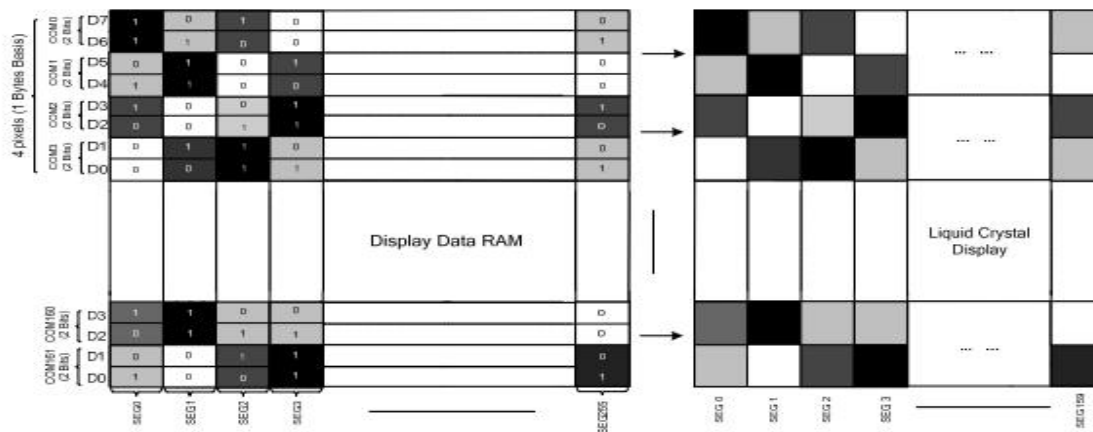
It recommends that the operating modes and display contents should be refreshed periodically to prevent the effect of unexpected noise.

4.6 Display Memory Map

Page Address	Data	LCD Module Top View							
0	D7 : D0								
1	D7 : D0								
:	:								
5	D7 : D0								
:	:								
8	D7 : D0								
:	:								
11	D7 : D0								
Column Address		00h							7Fh
Internal Display RAM Address									

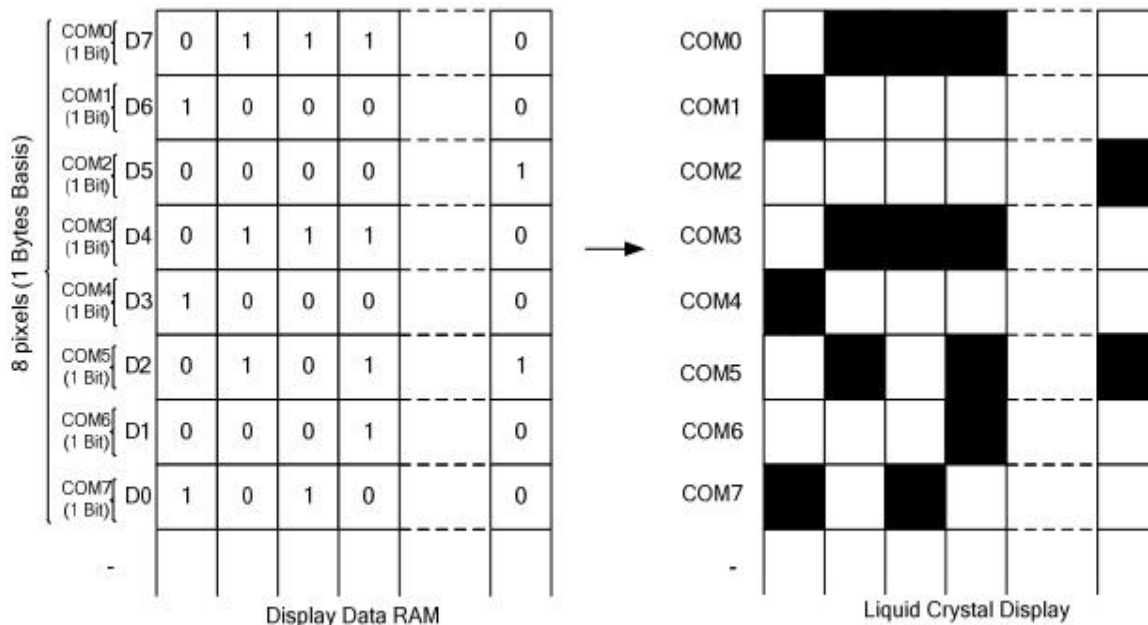
Note: Display start line = 0, INV = 0.

4.7 Display Data RAM (DDRAM)



2 Bits Data N=0~3		DDRAM		LCD
D2N+1	D2N			
1	1	1	1	
0	0	0	0	
1	0	1	0	
0	1	0	1	

DDRAM Mapping (4-Level Gray Scale Mode)



DDRAM Mapping (Monochrome Mode)

4.8 Display Commands

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
1.Extension Command	0	0	0	0	1	1	EXT1	0	0	EXT0	Set extension instruction
Ext[1:0]=0,0 (Extension Command 1)											
2.Display ON/OFF	0	0	1	0	1	0	1	1	1	DSP	Set LCD display DSP=0: Display off DSP=1: Display on
3.Inverse Display	0	0	1	0	1	0	0	1	1	INV	Set inverse display INV=0: Normal display INV=1: Inverse display
4.All Pixel ON/OFF	0	0	0	0	1	0	0	0	1	AP	Set all pixel on mode AP=0: All pixel off mode AP=1: All pixel on mode
5.Display Control	0	0	1	1	0	0	1	0	1	0	Set display control CLD :Set CL dividing ratio DT[7:0] : Set the number of duty LF[4:0] : Set N-line inversion counter FI : Set the inversion type of frame at the end of common scan cycle
	1	0	0	0	0	0	0	CLD	0	0	
	1	0	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	
	1	0	0	0	LF4	FI	LF3	LF2	LF1	LF0	
6.Power Save	0	0	1	0	0	1	0	1	0	SLP	Set power save mode SLP=0: Sleep out mode SLP=1: Sleep in mode
7.Set Page Address	0	0	0	1	1	1	0	1	0	1	Set page address Starting page address: 00h ≤ YS ≤ 27h Ending page address: YS ≤ YE ≤ 27h
	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
8.Set Column Address	0	0	0	0	0	1	0	1	0	1	Set column address Starting column address: 00h ≤ XS ≤ 9Fh Ending column address: XS ≤ XE ≤ 9Fh
	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
9.Data Scan Direction	0	0	1	0	1	1	1	1	0	0	Set normal/ inverse display of address and address scan direction
	1	0	0	0	0	0	0	MV	MX	0	
10.Write Data	0	0	0	1	0	1	1	1	0	0	Write data to DDRAM
	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
11.Read Data	0	0	0	1	0	1	1	1	0	1	Read data from DDRAM (Only for parallel interface and I ² C)
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
12.Partial In	0	0	1	0	1	0	1	0	0	0	Set partial area Starting partial display address: 00h ≤ PTS ≤ 9Fh Ending partial display address: 00h ≤ PTE ≤ 9Fh
	1	0	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0	
	1	0	PTE7	PTE6	PTE5	PTE4	PTE3	PTE2	PTE1	PTE0	

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
13.Partial Out	0	0	1	0	1	0	1	0	0	1	Exit the partial mode
14.Read/Modify/Write In	0	0	1	1	1	0	0	0	0	0	Enable read modify write
15.Read/Modify/Write Out	0	0	1	1	1	0	1	1	1	0	Disable read modify write
16.Scroll Area	0	0	1	0	1	0	1	0	1	0	Set scroll area TL[7:0] : Set top line address BL[7:0] : Set bottom line address NSL[7:0] : Number of specified line SCM[1:0] : Area scroll mode
	1	0	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	
	1	0	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0	
	1	0	NSL7	NSL6	NSL5	NSL4	NSL3	NSL2	NSL1	NSL0	
	1	0	0	0	0	0	0	0	SCM1	SCM0	
17.Set Start Line	0	0	1	0	1	0	1	0	1	1	Set scroll start address $00h \leq SL \leq 9Fh$
	1	0	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0	
18.OSC ON	0	0	1	1	0	1	0	0	0	1	Turn on the internal oscillator
19.OSC OFF	0	0	1	1	0	1	0	0	1	0	Turn off the internal oscillator
20.Power Control	0	0	0	0	1	0	0	0	0	0	Power circuit operation VB=0: OFF, VB=1: ON VF=0: OFF, VF=1: ON VR=0: OFF, VR=1: ON
	1	0	0	0	0	0	VB	0	VF	VR	
21.Set Vop	0	0	1	0	0	0	0	0	0	1	Set Vop
	1	0	0	0	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	
	1	0	0	0	0	0	0	Vop8	Vop7	Vop6	
22.Vop Control	0	0	1	1	0	1	0	1	1	VOL	Control Vop VOL=0: Vop increase one step VOL=1: Vop decrease one step
23.Read Register Mode	0	0	0	1	1	1	1	1	0	REG	Set read register mode REG=0: read the register value of Vop[5:0] REG=1: read the register value of Vop[8:6]
24.Nop	0	0	0	0	1	0	0	1	0	1	No operation
25.Read Status (Parallel and I ² C)	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Read status byte (Parallel and I ² C)
26.Read Status (4-Line and 3-Line SPI)	0	0	1	1	1	1	1	1	1	0	Read status byte (4-Line and 3-Line SPI)
	0	1	D7	D6	D5	D4	D3	D2	D1	D0	
27.Data Format Select	0	0	0	0	0	0	1	DO	0	0	DO=0; LSB on bottom (Default) DO=1; LSB on top
28. Display Mode	0	0	1	1	1	1	0	0	0	0	Set display mode DM=0 :Mono(Default) DM=1 :4Gray Scale Mode
	1	0	0	0	0	1	0	0	0	DM	

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
29.Set ICON	0	0	0	1	1	1	0	1	1	ICON	Enable/Disable ICON RAM ICON=1 ; Enable ICON RAM ICON=0 ; Disable ICON RAM
Ext[1:0]=0,1 (Extension Command 2)											
30. Set Gray Level	0	0	0	0	1	0	0	0	0	0	Set gray scale level GL[4:0]: Set Light Gray Level GD[4:0]: Set Dark Gray Level
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	GL4	GL3	GL2	GL1	GL0	
	1	0	0	0	0	GL4	GL3	GL2	GL1	GL0	
	1	0	0	0	0	GL4	GL3	GL2	GL1	GL0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
	1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
	1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
31.Analog Circuit Set	0	0	0	0	1	1	0	0	1	0	Set analog circuit BE[1:0]: Booster efficiency set BS[2:0]: Set bias ratio
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	BE1	BE0	
	1	0	0	0	0	0	0	BS2	BS1	BS0	
32.Booster Level	0	0	0	1	0	1	0	0	0	1	Set booster level BST=0 : X8 BST=1 : X10
	1	0	1	1	1	1	1	0	1	BST	
33. Driving Select	0	0	0	1	0	0	0	0	0	DS	Power type DS=0: Internal (Default) DS=1 :External
34.Auto Read Control	0	0	1	1	0	1	0	1	1	1	Set auto-read instruction XARD=0: Enable auto read XARD=1: Disable auto read
	1	0	1	0	0	XARD	1	1	1	1	
35.OTP WR/RD Control	0	0	1	1	1	0	0	0	0	0	OTP WR/RD control WR/RD=0: Enable OTP read WR/RD=1: Enable OTP write
	1	0	0	0	WR/RD	0	0	0	0	0	
36.OTP Control Out	0	0	1	1	1	0	0	0	0	1	OTP control out
37.OTP Write	0	0	1	1	1	0	0	0	1	0	OTP write
38.OTP Read	0	0	1	1	1	0	0	0	1	1	OTP read

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
39.OTP Selection Control	0	0	1	1	1	0	0	1	0	0	OTP selection control Ctrl=1: Disable OTP Selection Ctrl=0: Enable OTP Selection
	1	0	1	Ctrl	0	1	1	0	0	1	
40.OTP Programming Setting	0	0	1	1	1	0	0	1	0	1	OTP programming setting
	1	0	0	0	0	0	0	1	1	1	
41.Frame Rate	0	0	1	1	1	1	0	0	0	0	Frame rate setting in different temperature range
	1	0	0	0	0	FRA4	FRA3	FRA2	FRA1	FRA0	
	1	0	0	0	0	FRB4	FRB3	FRB2	FRB1	FRB0	
	1	0	0	0	0	FRC4	FRC3	FRC2	FRC1	FRC0	
	1	0	0	0	0	FRD4	FRD3	FRD2	FRD1	FRD0	
42.Temperature Range	0	0	1	1	1	1	0	0	1	0	Temperature range setting
	1	0	0	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
	1	0	0	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
	1	0	0	TC6	TC5	TC4	TC3	TC2	TC1	TC0	
43.Temperature Gradient Compensation	0	0	1	1	1	1	0	1	0	0	Set temperature gradient compensation coefficient
	1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00	
	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20	
	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40	
	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60	
	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80	
	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0	
	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0	
	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0	
Ext[1:0]=1,1(Extension Command 4)											
44.Enable OTP	0	0	1	1	0	1	0	1	1	0	Enable OTP EOTP =0 ; Disable (Default) EOTP =1 ; Enable
	1	0	0	0	0	EOTP	0	0	0	0	

Note: For Details please refer to ST75161 datasheet.

Design and Handling Precaution

1. The LCD panel is made by glass. Any mechanical shock (eg. dropping from high place) will damage the LCD module.
2. Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.
3. The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.
4. Never attempt to disassemble or rework the LCD module.
5. Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
6. When mounting the LCD module, make sure that it is free from twisting, warping and distortion.
7. Ensure to provide enough space (with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result.
8. Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
9. Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
10. LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
11. When peeling off the protective film from LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
12. Take care and prevent get hurt by the LCD panel sharp edge.
13. Never operate the LCD module exceed the absolute maximum ratings.
14. Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
15. Never apply signal to the LCD module without power supply.
16. IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
17. LCD module reliability may be reduced by temperature shock.
18. When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module.

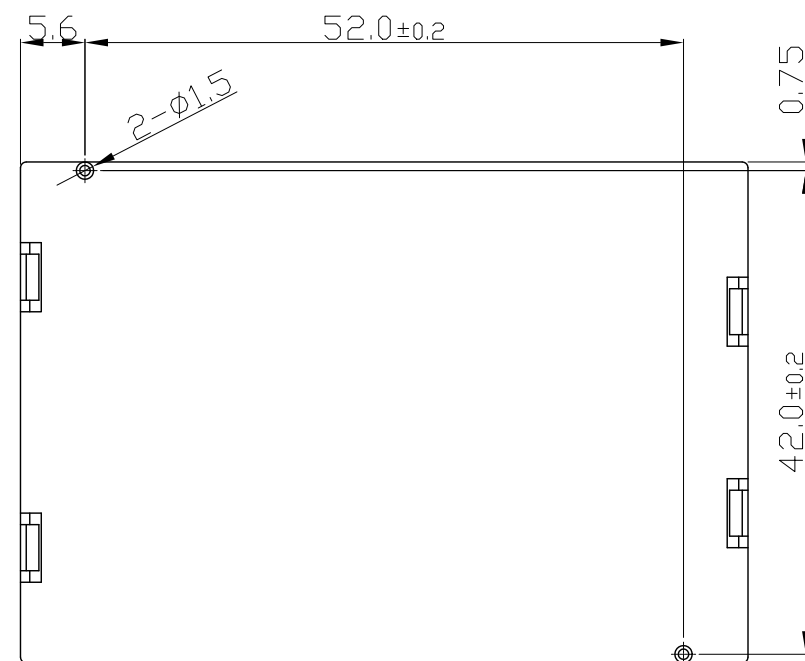
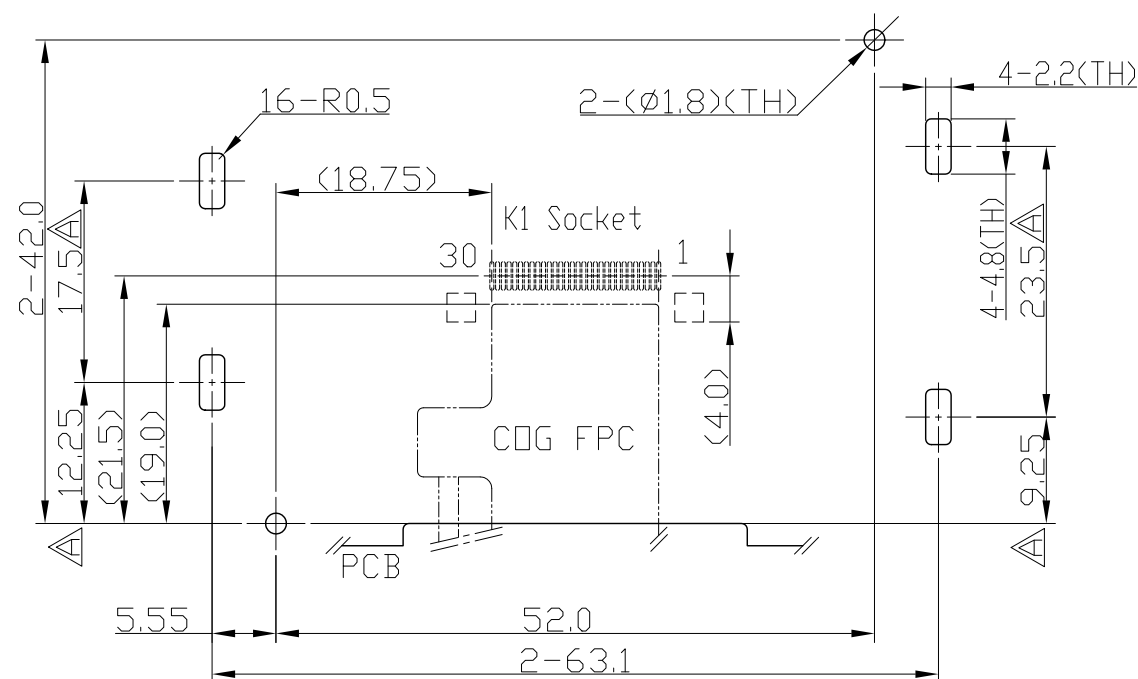


Diagram illustrating a multi-ported memory structure. The structure consists of a vertical stack of memory segments labeled COM94, COM0, SEGO, ..., SEGI27, COM1, ..., COM95. Horizontal lines connect these segments to a common vertical line on the right, representing a shared bus or output.



Application PCB Example
(PCB Thickness=1.6t, PCB Tol=±0.15mm)
Scale=3/2

TOPWAY

Note:

- *1. Display Type : FSTN, Positive, Transflective
- *2. Viewing Direction : 6H
- *3. Duty : 1/96, Bias : 1/10, Vop : 12.5V
- *4. Operating Voltage : 3.3V
- *5. Backlight Supply : 3.3V
- *6. Backlight Color : White
- *8. Recommended Connector : FH19SC-30S-0.5SH(HIROSE) Or Equivalent
- *9. Operating Temperature : -40°C~70°C
- *10. Storage Temperature : -40°C~80°C